

DESCRIPTION

The SM series of transient voltage suppressors are designed to protect components which are connected to data and transmission lines from over voltages caused by electrostatic discharge (ESD), electrical fast transients (EFT), and induced lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The dual junction common anode design allows the user to protect two separate lines with one package. The low cost SOT-23 package allows flexibility in the design of "crowded" PC boards. The SM series is suitable protection for sensitive TTL and CMOS ICs such as microprocessors, I/O transceivers, ASICs, transducers, and CMOS memory.

The SM series TVS diode will meet the surge requirements of IEC 1000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

APPLICATIONS:

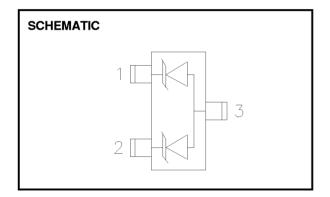
- RS-232, RS-423 data lines
- Cellular phone terminals
- Audio/Video inputs
- Portable electronics
- Networks

FEATURES:

- 300 watts Peak Pulse Power (tp = 8 x 20µs)
- Transient protection for data, signal, and Vcc bus to IEC 1000-4-2 (ESD) & IEC 1000-4-4 (EFT)
- Protects two unidirectional lines or one bidirectional line
- ESD protection >15kV
- Low Leakage Current
- Solid state silicon avalanche technology

MECHANICAL CHARACTERISTICS:

- JEDEC SOT-23 package
- Solder temperature : 265°C for 10 seconds
- Readily solderable terminals
- Marking: Marking Code
- Packaging : Tape & Reeled per EIA 481-1



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp = 8 x 20μs)	Ppk	300	Watts
Operating Temperature	Tj	-55 to +150	°C
Storage Temperature	Tstg	-55 to +150	°C

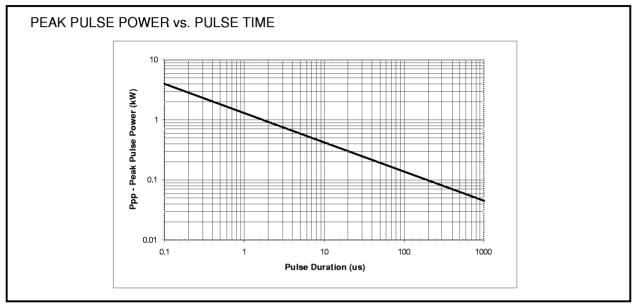
ELECTRICAL CHARACTERISTICS @ 25°C

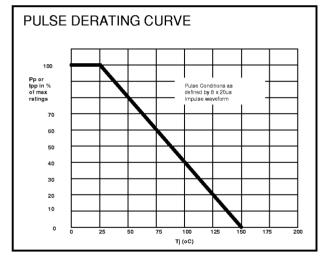
	Device	Reverse	Min	Max.	Max.	Leakage	Capacitance	Capacitance
Part	Marking	Stand-off	V _{BR}	Clamping	Peak Pulse	Current	@ 0v, 1MHz	@ 0v, 1MHz
Number	Code	Voltage	@ 1mA	@ lpp=1A ¹	Current ²	@ V _{RWM}	Pin 1- 2	Pin 1-3 & 2-3
		V _{RWM}	BV(min)	Vc	lpp	I _R	Cj	Cj
		Volts	Volts	Volts	Amps	μA	pf	pf
SM05	M05	5	6	9.8	17	20	350	400
SM12	M12	12	13.3	19	12	1	120	150
SM15	M15	15	16.7	24	10	1	75	100
SM24	M24	24	26.7	43	5	1	50	60
SM36	M36	36	40	60	4	1	40	45

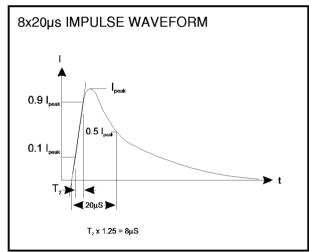
Notes :

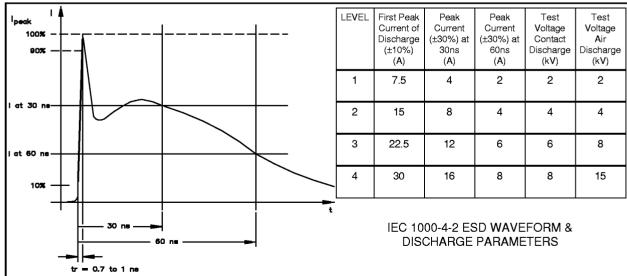
^{1.} Clamping voltage values are based upon an industry standard 8 x 20µs peak pulse current (lpp) waveform.

^{2.} $tp = 8/20 \mu s$

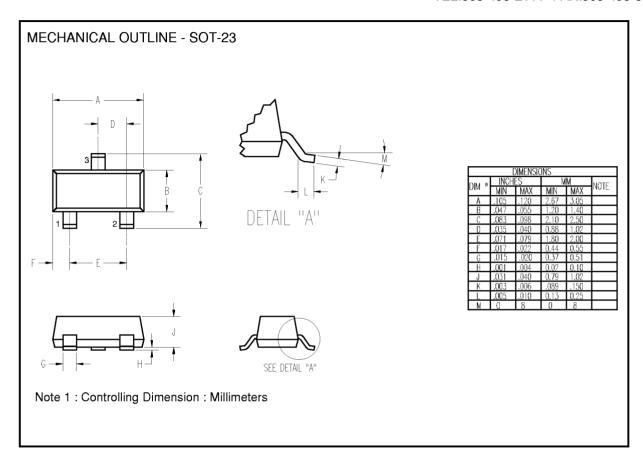








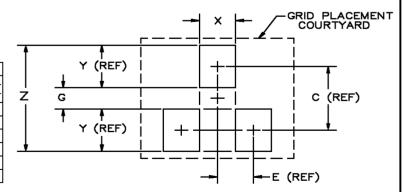




LAND PATTERN - SOT-23

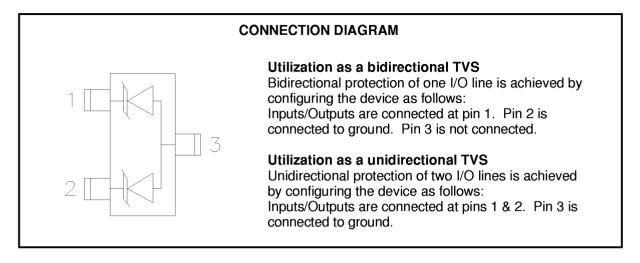
The layout of a surface mount board is a critical part of the design process. The footprint of the package must be the correct size to insure proper solder connection between the board and the device. Correct pad geometry will allow the devices to self align when subjected to the solder reflow process.

			DIMEN:	SIONS	ì	
	DIM	INCHES		М	NOTE	
ľ	ייואווט.	MIN	MAX	MIN	MAX	NOIE
	С	_	.09	_	2.20	_
	Ε	_	.04	-	.95	_
	G	.03	.04	.80	1.00	-
	Χ	.03	.04	.80	1.00	-
	Y	_	.06	_	1.40	_
	Z	.14	.15	3.40	3.60	_



Note 1 : Grid placement courtyard is 8 x 8 elements (4mm x 4mm) in accordance with the international grid detailed in IEC Publication 97.





TYPICAL APPLICATION

