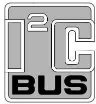

TDA10023HT

Single chip DVB-C/MCNS channel receiver

Rev. 01 — 12 April 2005 **Product data sheet**

1. General description

The TDA10023HT is a single chip DVB-C/MCNS channel receiver for 4, 16, 32, 64, 128 and 256-QAM modulated signals. The device interfaces directly to the IF signal, which is sampled by a 10-bit A/D converter.

The TDA10023HT performs the clock and the carrier recovery functions. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the current application.

After baseband conversion, equalization filters are used for echo cancellation in cable applications. These filters are configured as T-spaced transversal equalizer or DFE equalizer, so that the system performance can be optimized according to the network characteristics. A proprietary equalization algorithm, independent of carrier offset, is achieved in order to assist carrier recovery. Then a decision directed algorithm takes place, to achieve final equalization convergence.

The TDA10023HT chip implements two FEC decoders, one for each standard. In the DVB-C mode the TDA10023HT implements a Forney convolutional de-interleaver of depth 12 blocks and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The de-interleaver and the Reed-Solomon decoder are automatically synchronized thanks to the frame synchronization algorithm that uses the MPEG2 sync byte. Finally descrambling according to DVB-C standard is achieved at the Reed-Solomon output. In the MCNS mode the receiver error correction implements a soft decision trellis decoder to correct random channel errors, a randomizer, a convolutional de-interleaver of depth I = 128, 64, 32, 16, 8 and J = 1, 2, 3, 4, 8, 16 for burst protection, and a Reed-Solomon decoder which corrects up to 3 erroneous symbols. The de-interleaver and the Reed-Solomon decoder are automatically synchronized using the frame sync trailer.

This device is controlled via an I^{2}C-bus.

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2. Features

- 4,16, 32, 64, 128 and 256 QAM demodulator (*ITU-T J.83 annex A-B and C* compatible)
- High performance for 256 QAM especially for direct IF applications
- On-chip 10-bit ADC
- On-chip PLL for crystal frequency multiplication (typically 16 MHz crystal)
- Digital down conversion
- Programmable half Nyquist filter (roll off = 0.12, 0.13, 0.15 and 0.18)
- Two PWM AGC outputs with programmable take-over point (for tuner and down converter control)
- Clock timing recovery, with programmable second order loop filter
- Variable symbol rate capability from SACLK/64 to SACLK/4 (with low sampling clock: SACLK = 36 MHz maximum) or from SACLK/128 to SACLK/8 (with high sampling clock: SACLK = 72 MHz maximum)
- Programmable anti-aliasing filters
- Full digital carrier recovery loop
- Carrier acquisition range up to 9 % of symbol rate
- Integrated adaptive equalizer (linear transversal equalizer or decision feedback equalizer)
- DVB compatible differential decoding and mapping
- On chip DVB-C full compliant FEC decoder (de-interleaver, Reed-Solomon decoder and de-scrambler)
- On chip MCNS full compliant FEC decoder (trellis demodulator, de-randomizer, de-interleaver and Reed-Solomon decoder)
- Multiple TS JQAM filter
- Parallel and serial transport stream interface simultaneously
- I^2C-bus interface, for easy control

3. Applications

- Cable set-top boxes
- Cable modems
- Cable Network Interface Modules (NIMs)
- Multichannel Multipoint Distribution Service (MMDS) (ETS 300-749) set-top boxes

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4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Recommended operating conditions						
V_{DDD3}	digital core supply voltage		1.65	1.8	1.95	V
V_{DDD2}	digital pad supply voltage		3	3.3	3.6	V
T_{amb}	ambient temperature		0	-	70	°C
V_{IH}	HIGH-level input voltage (including voltage on outputs in 3-state mode)	all digital inputs are 5 V tolerant except XIN which is 2 V tolerant	$0.8V_{DDD3}$	-	V_{DDD3}	V
			1.8	-	5.5	V
V_{IL}	LOW-level input voltage (including voltage on outputs in 3-state mode)	all digital inputs are 5 V tolerant except XIN which is 2 V tolerant	0	-	$0.2V_{DDD3}$	V
			0	-	1	V
V_{OH}	HIGH-level output voltage		2.6	2.9	3.2	V
V_{OL}	LOW-level output voltage		0	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDD2} - 0.4$ V	−4.8	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V	4.2	-	-	mA
P	power dissipation	QAM 256 / symbol rate 6.9 MBd; $f_s = 29.33$ MHz; cs = 150 %	-	500	620	mW
$I_{tot(3V3)}$	total current consumption for the digital and analog 3.3 V supply voltages (V_{DDD2}, V_{DDD4}, V_{DDA3})	QAM 256 / symbol rate 6.9 MBd; $f_s = 29.33$ MHz; cs = 150 %	-	94	100	mA
$I_{tot(1V8)}$	total current consumption for the digital and analog 1.8 V supply voltages (V_{DDD1}, V_{DDD3}, V_{DDA2})	QAM 256 / symbol rate 6.9 MBd; $f_s = 29.33$ MHz; cs = 150 %	-	105	130	mA
C_i	input capacitance		-	-	6	pF
Crystal oscillator characteristics						
V_{DDA1}	crystal analog supply voltage		1.65	1.8	1.95	V
I_{DDA1}	supply current in Slave mode	at maximum f_c	-	-	1.12	mA
$f_{i(slave)}$	input frequency in Slave mode		1	-	50	MHz
f_c	output frequency		1	-	50	MHz
V_{XIN}	XIN input level in Slave mode	AC coupled	400	900	-	mV
t_{start}	average start-up time		-	500	-	µs
Slope	XIN clock signal slope		25	-	-	V/µs
PLL characteristics						
V_{DDA2}	analog PLL supply voltage		1.6	1.8	2.0	V
V_{DDD1}	digital PLL supply voltage		1.65	1.8	1.95	V
I_{DDA2}	analog supply current		-	1	-	mA
I_{DDD1}	digital supply current		-	1	-	mA
f_{ref}	input frequency		0.1	-	150	MHz
f_{out}	output frequency		4.3	-	550	MHz
t_{PU}	start-up time to power-up		-	-	500	µs

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Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
10-bit ADC characteristics							
V_{DDA3}	analog ADC supply voltage			3.0	3.3	3.6	V
V_{DDD4}	digital ADC supply voltage			3.0	3.3	3.6	V
V_{DDD1}	digital ADC supply voltage			1.65	1.8	1.95	V
V_{dif}	differential input range $V_{VIP} - V_{VIM}$	gainset = 0	[1]	–1	-	+1	V
		gainset = 1	[1]	–0.5	-	+0.5	V
V_{range}	single-ended peak-to-peak input range (on VIP)	gainset = 0	[1]	-	2	-	V
		gainset = 1	[1]	-	1	-	V
V_{DC}	DC reference level (common mode)	differential input		0.5	$0.5V_{DDA3}$	1.8	V
		single-ended input		0.9	-	1.3	V
R_i	input resistance	single-ended or differential input		-	7.5	-	kΩ
C_i	input capacitance	VIP or VIM		-	1.5	-	pF
$f_{i(max)}$	maximum input frequency	CS = 11 (differential input)	[1]	-	-	100	MHz
		CS = 10 (differential input)	[1]	-	-	80	MHz
		CS = 01 (differential input)	[1]	-	-	60	MHz
		CS = 00 (differential input)	[1]	-	-	35	MHz
		CS = 10 (single-ended input)	[1]	-	-	60	MHz
$f_{s(max)}$	maximum sampling frequency	CS = 11	[1]	-	-	90	MHz
		CS = 10	[1]	-	-	80	MHz
		CS = 01	[1]	-	-	60	MHz
		CS = 00	[1]	-	-	35	MHz

[1] ‘Gainset’ and ‘CS’ are programmed by registers. CS must be selected as small as possible because it reduces the power consumption.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA10023HT	TQFP64	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm	SOT357-1

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6. Block diagram

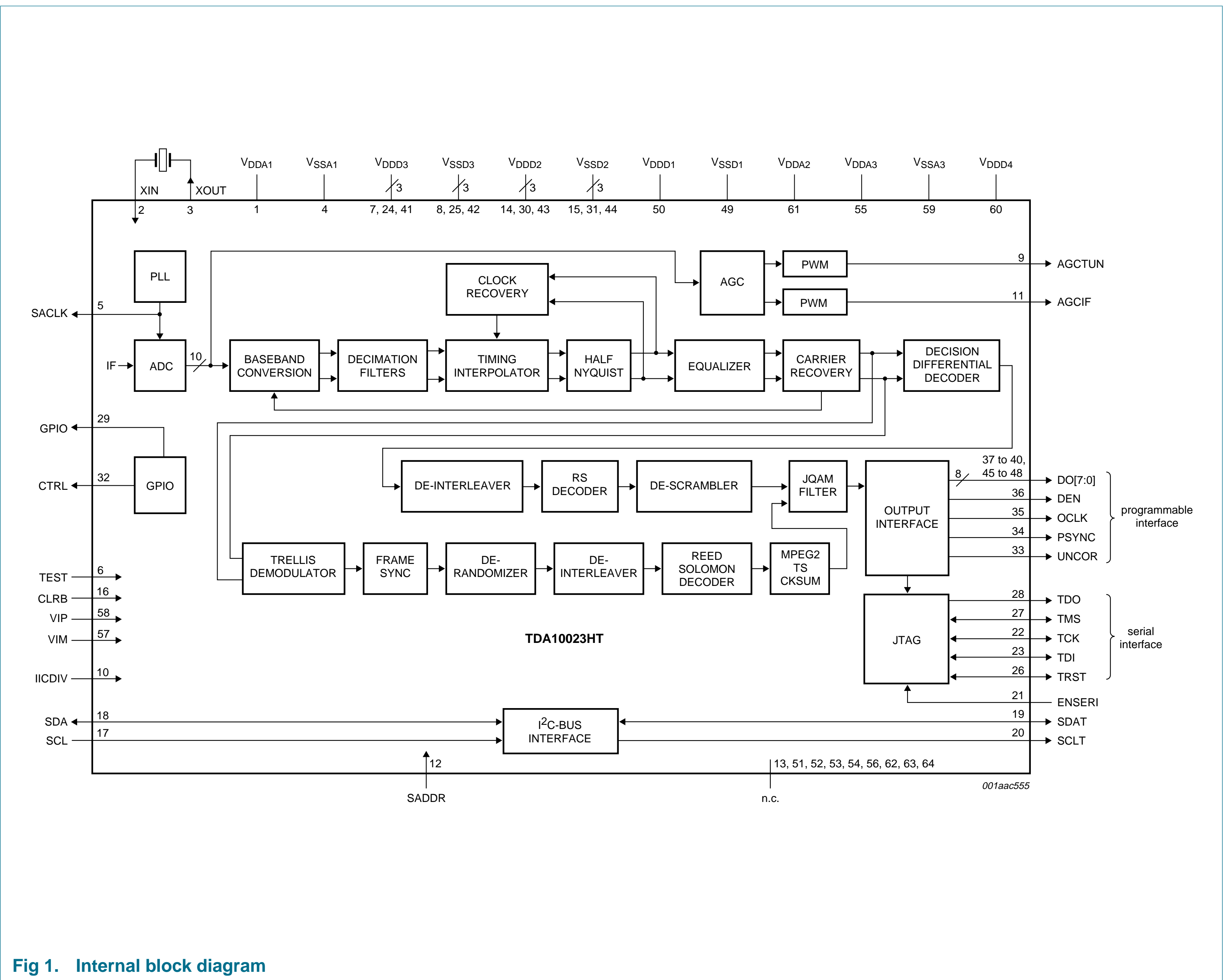

Fig 1. Internal block diagram

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7. Pinning information

7.1 Pinning

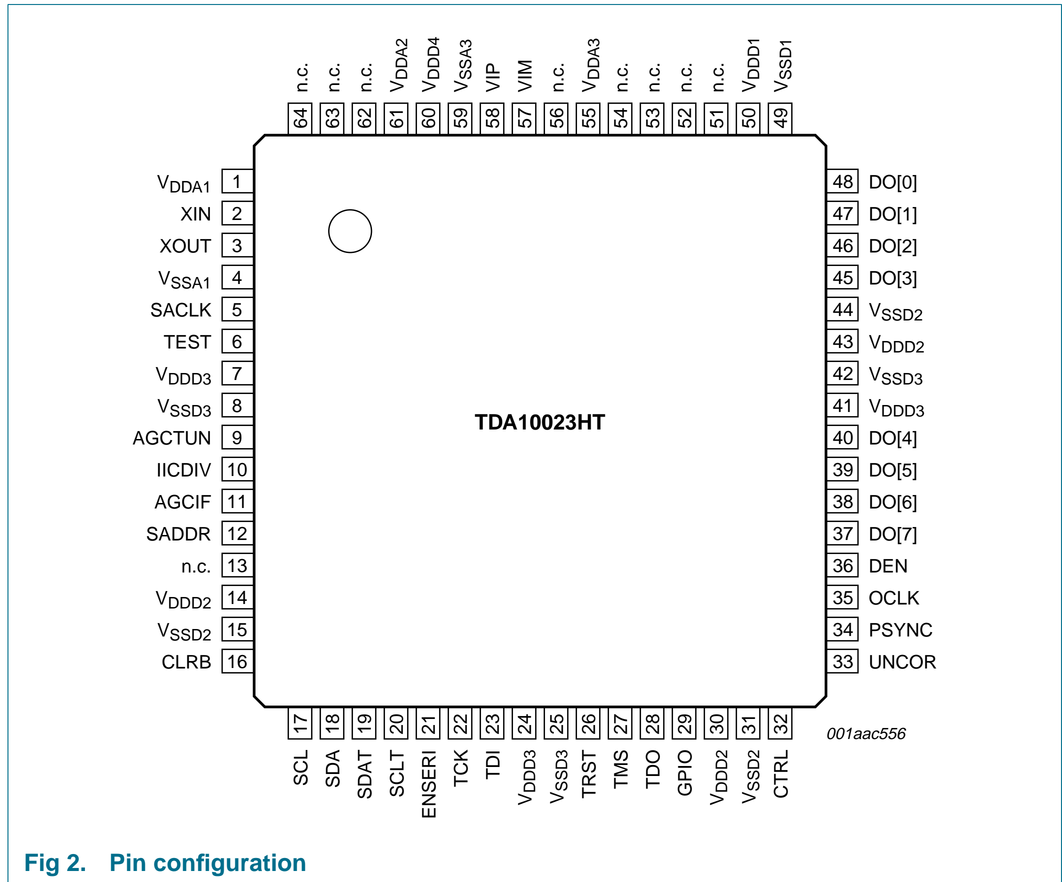

Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Type [1]	Description
V_{DDA1}	1	S	crystal analog supply voltage 1.8 V
XIN	2	I	Crystal oscillator input. Typically a fundamental crystal oscillator is connected between the XIN and XOUT pins. The crystal frequency **must** be chosen so that the system frequency SYSCLK (= XIN × multiplying factor of the PLL) equals 1.6 times the tuner output intermediate frequency: SYSCLK = 1.6 × IF.
XOUT	3	O	crystal oscillator output; typically a fundamental crystal oscillator is connected between the XIN and XOUT pins
V_{SSA1}	4	G	crystal analog ground
SACLK	5	O	Sampling clock. This output clock can be fed to an external 10-bit ADC as the sampling clock. SACLK can be either equal to SYSCLK/2 in simple sampling mode or equal to SYSCLK in double sampling mode.
TEST	6	I	test input pin; in normal mode, TEST must be grounded

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Table 3: Pin description *…continued*

Symbol	Pin	Type [1]	Description
V_{DDD3}	7	S	digital core supply voltage 1.8 V
V_{SSD3}	8	G	digital core ground
AGCTUN	9	O/OD	First PWM encoded output signal for AGC tuner. This signal is typically fed to the AGC amplifier through a single RC network. The maximum signal frequency on VAGC output is XIN/16. AGC information can be refreshed every 512 ADC samples.
IICDIV	10	I	IICDIV allows to select the frequency of the I^2C-bus internal system clock, depending on the crystal frequency. Internal I^2C-bus clock is a division of XIN by 4^{IICDIV}.
AGCIF	11	O/OD	Second PWM encoded output signal for AGC IF. This signal is typically fed to the AGC amplifier through a single RC network. The maximum signal frequency on VAGC output is XIN/16. AGC information can be refreshed every 512 ADC samples. But AGCIF can also be configured to output a PWM signal, which value can be programmed through the I^2C-bus interface (see register PWMREF, index 34h).
SADDR	12	I	Two I^2C-bus addresses are implemented in the TDA10023HT chip. One address regarding all the TDA10023HT registers except JQAM registers, and a second one dedicated to the JQAM filter registers only. SADDR is the LSB of the 2 I^2C-bus addresses. The MSBs are internally set to 000110 (all registers except JQAM) and 000111 (only JQAM). Therefore the 2 complete I^2C-bus addresses are (MSB to LSB): 0, 0, 0, 1, 1, 0, SADDR (core registers) 0, 0, 0, 1, 1, 1, SADDR (JQAM registers)
n.c.	13		not connected
V_{DDD2}	14	S	digital pad supply voltage 3.3 V
V_{SSD2}	15	G	digital pad ground
CLRB	16	I	The CLRB input is asynchronous and active LOW, and clears the TDA10023HT. When CLRB goes LOW, the circuit immediately enters its RESET mode and normal operation will resume 4 XIN falling edges later after CLRB returned HIGH. The I^2C-bus register contents are all initialized to their default values. The minimum width of CLRB at LOW level is 4 XIN clock periods.
SCL	17	I	I^2C-bus clock input. SCL should nominally be a square wave with a maximum frequency of 400 kHz. SCL is generated by the system I^2C-bus master.
SDA	18	I/OD	SDA is a bidirectional signal. It is the serial input/output of the I^2C-bus internal block. A pull-up resistor (typically 4.7 kΩ) must be connected between SDA and V_{DDD2} (or 5 V) for proper operation (open-drain output).
SDAT	19	I/OD	SDAT is equivalent to SDA I/O of TDA10023HT but can be 3-stated by I^2C-bus programming. It is actually the output of a switch controlled by parameter BYPIIC of register TEST (index 0Fh). SDAT is an open-drain output and therefore requires an external pull-up resistor.

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Table 3: Pin description *...continued*

Symbol	Pin	Type [1]	Description
SCLT	20	OD	SCLT can be configured to be a control line output or to output SCL input. This is controlled by parameter BYPIIC and CTRL_SCLT of register TEST (index 0Fh). SCLT is an open-drain output and therefore requires an external pull-up resistor.
ENSERI	21	I	When HIGH this pin enables the serial output transport stream through the boundary scan pins: TRST, TDO, TCK, TDI and TMS (serial interface). Must be set LOW in Built-In Self-Test (BIST) and boundary scan mode.
TCK	22	I/O	Test clock: an independant clock used to drive the TAP controller in boundary scan mode. In normal mode of operation, TCK must be set LOW. *In serial stream mode, TCK is the OCLK output.*
TDI	23	I/O	Test data in. The serial input for test data and instruction in boundary scan mode. In normal mode of operation, TDI must be set to LOW. *In serial stream mode, TDI is the PSYNC output.*
V_{DDD3}	24	S	digital core supply voltage 1.8 V
V_{SSD3}	25	G	digital core ground
TRST	26	I/O	Test reset. This active LOW input signal is used to reset the TAP controller in boundary scan mode. In normal mode of operation, TRST must be set LOW. *In serial stream mode, TRST is the uncorrectable output (UNCOR) and has to be connected to a pull-down resistor.*
TMS	27	I/O	Test mode select. This input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set LOW. *In serial stream mode, TMS is the DEN output.*
TDO	28	O	Test data out. This is the serial test output pin used in boundary scan mode. Serial data are provided on the falling edge of TCK. *In serial stream mode, TDO is the data output (DO).*
GPIO	29	OD	GPIO can be configured by I^2C-bus (parameter SELGPIO[1:0], index 0Fh) either as: A Front-End Lock indicator (FEL) (default mode), or An active LOW output interrupt line (IT) which can be configured by the I^2C-bus interface. See registers ITsel (index 32h/33h) and ITstat (index 3Eh/3Fh), or A control output pin programmable by I^2C-bus (parameter CTRL_GPIO, index 1Eh) GPIO is an open-drain output and therefore requires an external pull-up resistor.
V_{DDD2}	30	S	digital pad supply voltage 3.3 V
V_{SSD2}	31	G	digital pad ground
CTRL	32	OD	CTRL is a control output pin programmable by I^2C-bus parameter CTRL of register CONTROL (index 1Eh). CTRL is open-drain output, and therefore requires an external pull-up resistor.

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Table 3: Pin description *...continued*

Symbol	Pin	Type [1]	Description
UNCOR	33	O	In DVB mode, uncorrectable transport stream packet. This output signal is HIGH when the provided packet is uncorrectable (during the 188 bytes of the packet). The uncorrectable packet is not affected by the Reed-Solomon decoder, but the MSB of the byte following the sync byte is forced ‘1’ for the MPEG2 process: error flag indicator (if RSI and IEI are set LOW in the I^2C-bus table). In MCNS mode, uncorrectable Reed-Solomon blocks. This output signal is HIGH when the provided block is uncorrectable (during the entire block). The uncorrectable block is not affected by the Reed-Solomon decoder.
PSYNC	34	O	Pulse synchro output. This output signal goes HIGH when the sync byte (47h) is provided (in DVB or MCNS modes), then it goes LOW until the next sync byte. Also by default (register TSOUT, index 1Eh), PSYNC is forced LOW when UNCOR pin goes HIGH.
OCLK	35	O	Output clock output. OCLK is the output clock for the DO[7:0] data outputs. OCLK is internally generated depending on which interface is selected.
DEN	36	O	Data enable (in DVB/MCNS modes). This output signal is HIGH when there is a valid data on output bus DO[7:0]. Also by default (register TSOUT, index 1Eh), DEN is forced LOW when UNCOR pin goes HIGH.
DO[7:0]	37,38, 39,40, 45,46, 47,48	O	Data output bus. These 8-bit parallel data are the outputs of the TDA10023HT after demodulation and FEC (DVB or MCNS) decoder. When one of the 3 possible parallel interfaces (A/B/C) is selected (parameter INTPSEL = 00/01/10, index 20h) then DO[7:0] is the transport stream output. When the serial interface is selected (parameter INTPSEL = 11, index 20h) then the serial output is on pin DO[0]. Also by default (register TSOUT, index 1Eh), in DVB or MCNS mode, the TS data is forced to the null TS FFh when the UNCOR pin goes HIGH.
V_{DDD3}	41	S	digital core supply voltage 1.8 V
V_{SSD3}	42	G	digital core ground
V_{DDD2}	43	S	digital pad supply voltage 3.3 V
V_{SSD2}	44	G	digital pad ground
V_{SSD1}	49	G	ground return for the digital switching circuitry (ADC and PLL)
V_{DDD1}	50	S	supply voltage for the digital switching circuitry 1.8 V (ADC and PLL)
n.c.	51		not connected
n.c.	52		not connected
n.c.	53		not connected
n.c.	54		not connected
V_{DDA3}	55	S	supply voltage for the analog circuits 3.3 V (ADC)
n.c.	56		not connected

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Table 3: Pin description *…continued*

Symbol	Pin	Type [1]	Description
VIM	57	I	Negative input to the A/D converter. This pin is DC biased to half-supply voltage through an internal resistor divider (2 × 20 kΩ resistors). In order to stay in the range of the ADC, $\|V_{VIP} - V_{VIM}\|$ should remain between the input range corresponding to the GAINADC register (index 1Bh - default value = 2 V).
VIP	58	I	Positive input to the A/D converter. This pin is DC biased to half-supply voltage through an internal resistor divider (2 × 20 kΩ resistors). In order to stay in the range of the ADC, $\|V_{VIP} - V_{VIM}\|$ should remain between the input range corresponding to the GAINADC register (index 1Bh - default value = 2 V).
V_{SSA3}	59	G	ground return for analog circuits (ADC)
V_{DDD4}	60	S	digital supply voltage for the switching circuitry 3.3 V (ADC)
V_{DDA2}	61	S	analog supply voltage 1.8 V (PLL)
n.c.	62		not connected
n.c.	63		not connected
n.c.	64		not connected

[1] All inputs (I) are TTL, 5 V tolerant (except XIN, VIP and VIM).
OD are open-drain outputs, so they must be connected to a pull-up resistor to V_{DDD2} (3.3 V) or 5 V.
All outputs are 4 mA drive, 5 V tolerant.

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDD3}	digital core supply voltage		–0.5	+1.98	V
V_{DDD2}	digital pad supply voltage		–0.5	+3.6	V
XIN	XIN input signal		–0.5	+2.0	V
V_i	DC analog input voltage		–0.5	$V_{DD} + 0.5$	V
V_I	DC input voltage		–0.5	+5.5	V
I_I	DC input current		-	±20	mA
T_{lead}	lead temperature		-	300	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	150	°C

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9. Application information

9.1 General block diagram

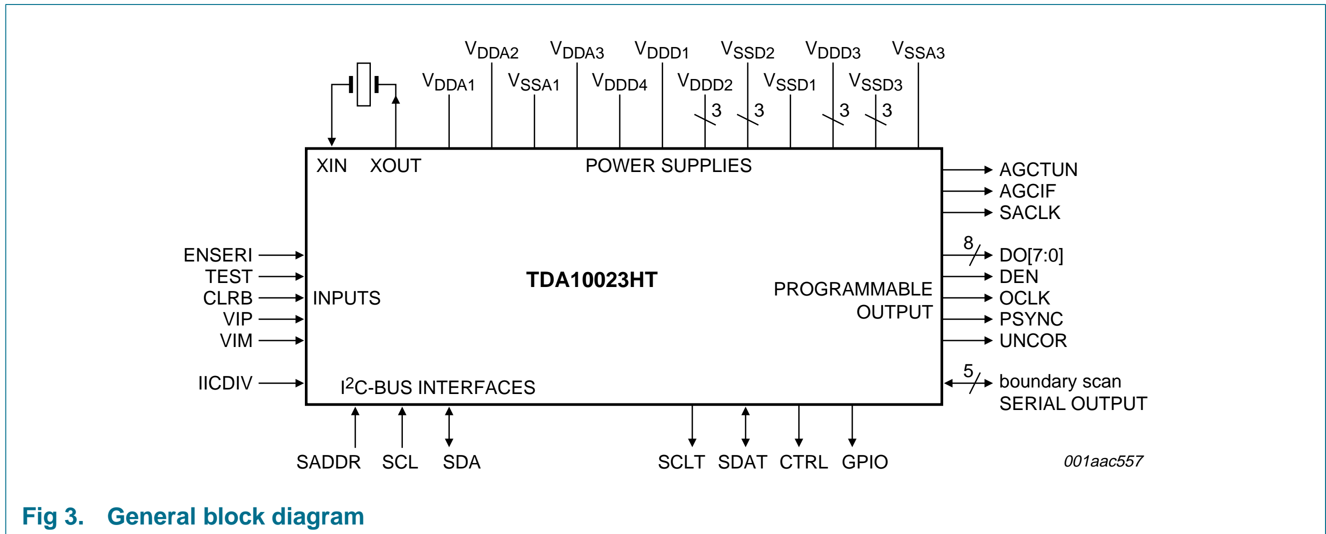
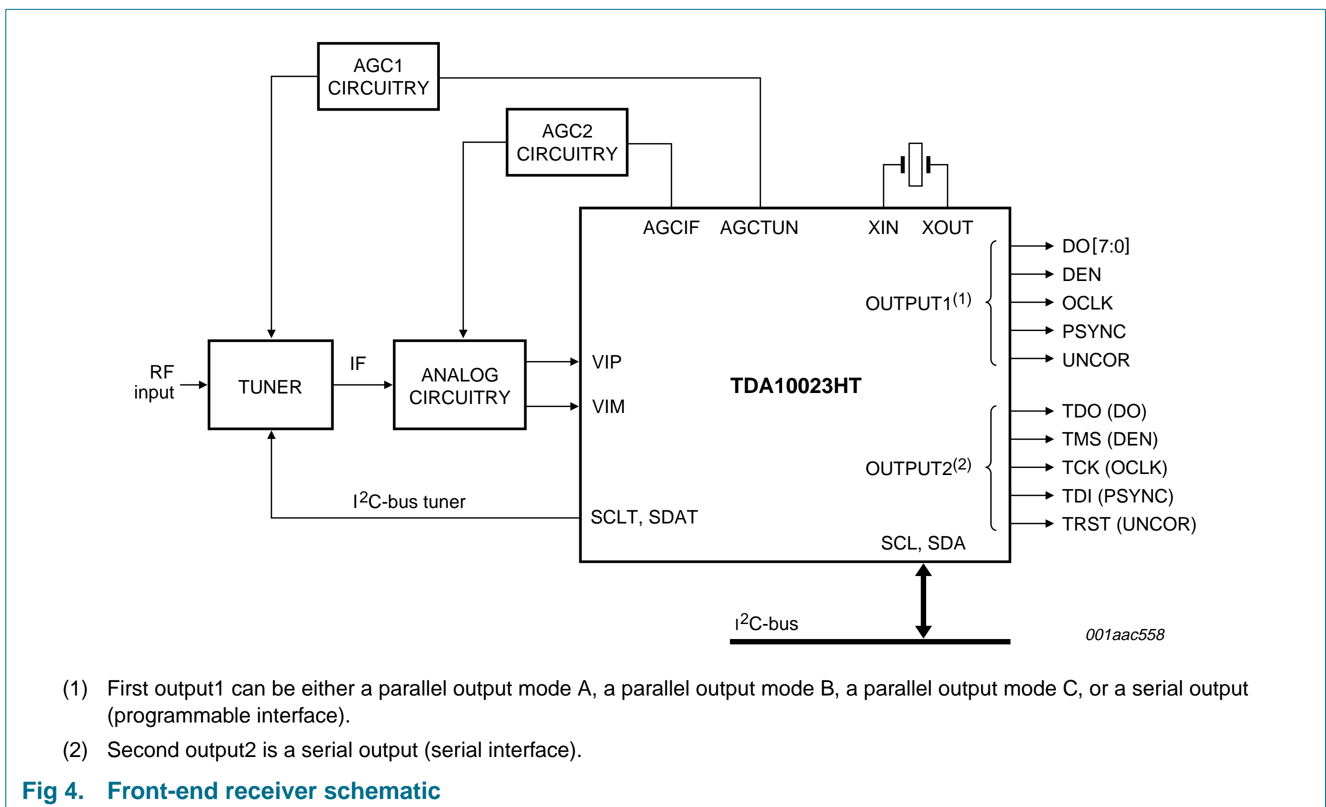


Fig 3. General block diagram

9.2 Typical application



(1) First output1 can be either a parallel output mode A, a parallel output mode B, a parallel output mode C, or a serial output (programmable interface).

(2) Second output2 is a serial output (serial interface).

Fig 4. Front-end receiver schematic

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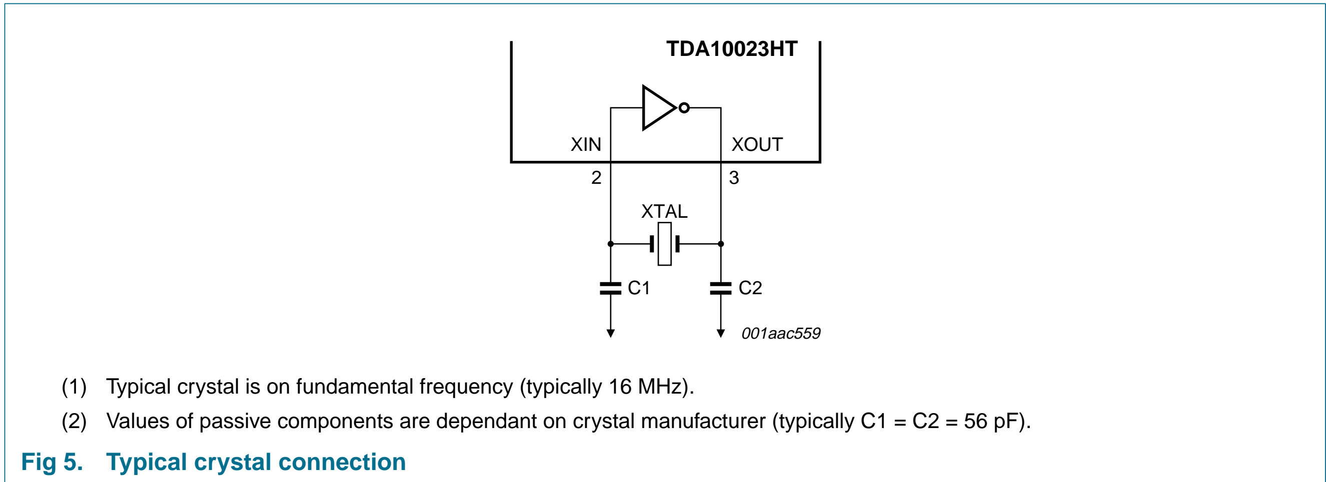
9.3 Crystal oscillator

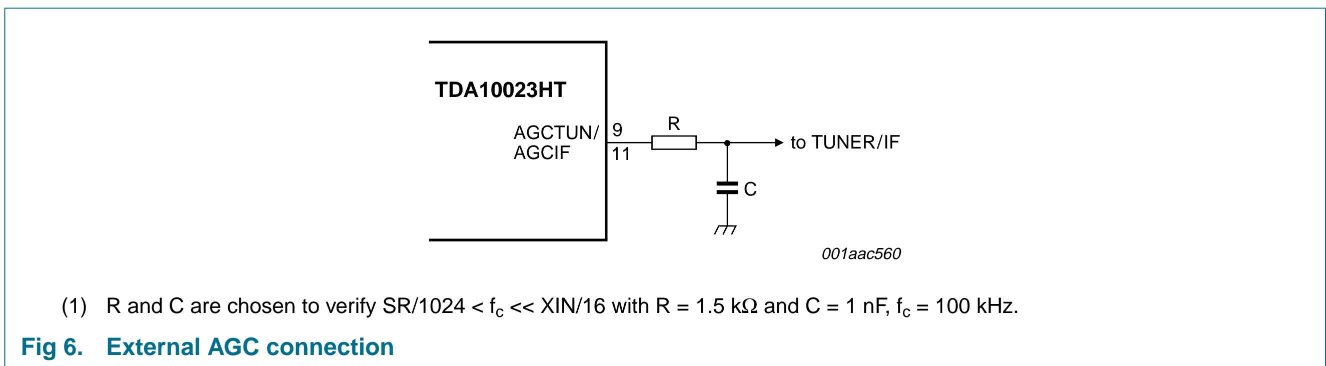


(1) Typical crystal is on fundamental frequency (typically 16 MHz).

(2) Values of passive components are dependant on crystal manufacturer (typically C1 = C2 = 56 pF).

Fig 5. Typical crystal connection

9.4 External AGC circuitry



(1) R and C are chosen to verify SR/1024 < f_c << XIN/16 with R = 1.5 kΩ and C = 1 nF, f_c = 100 kHz.

Fig 6. External AGC connection

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9.5 External PLL and ADC connections

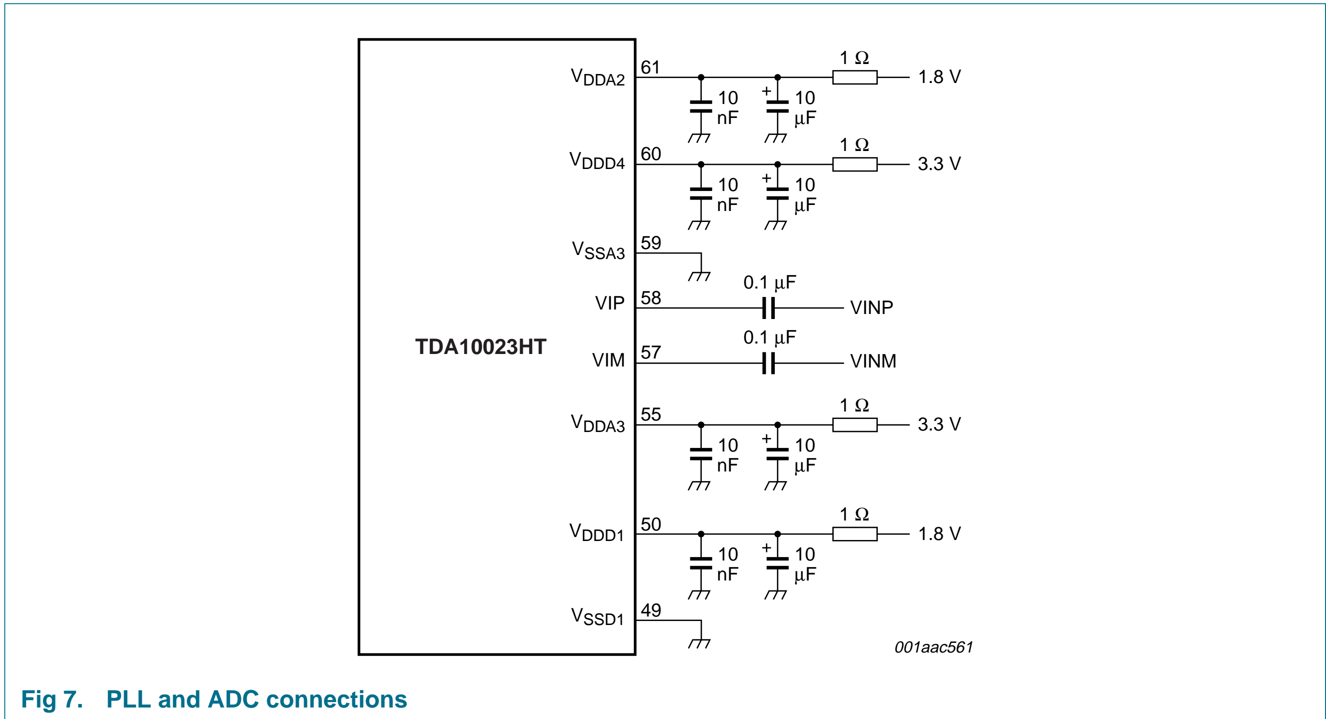

Fig 7. PLL and ADC connections

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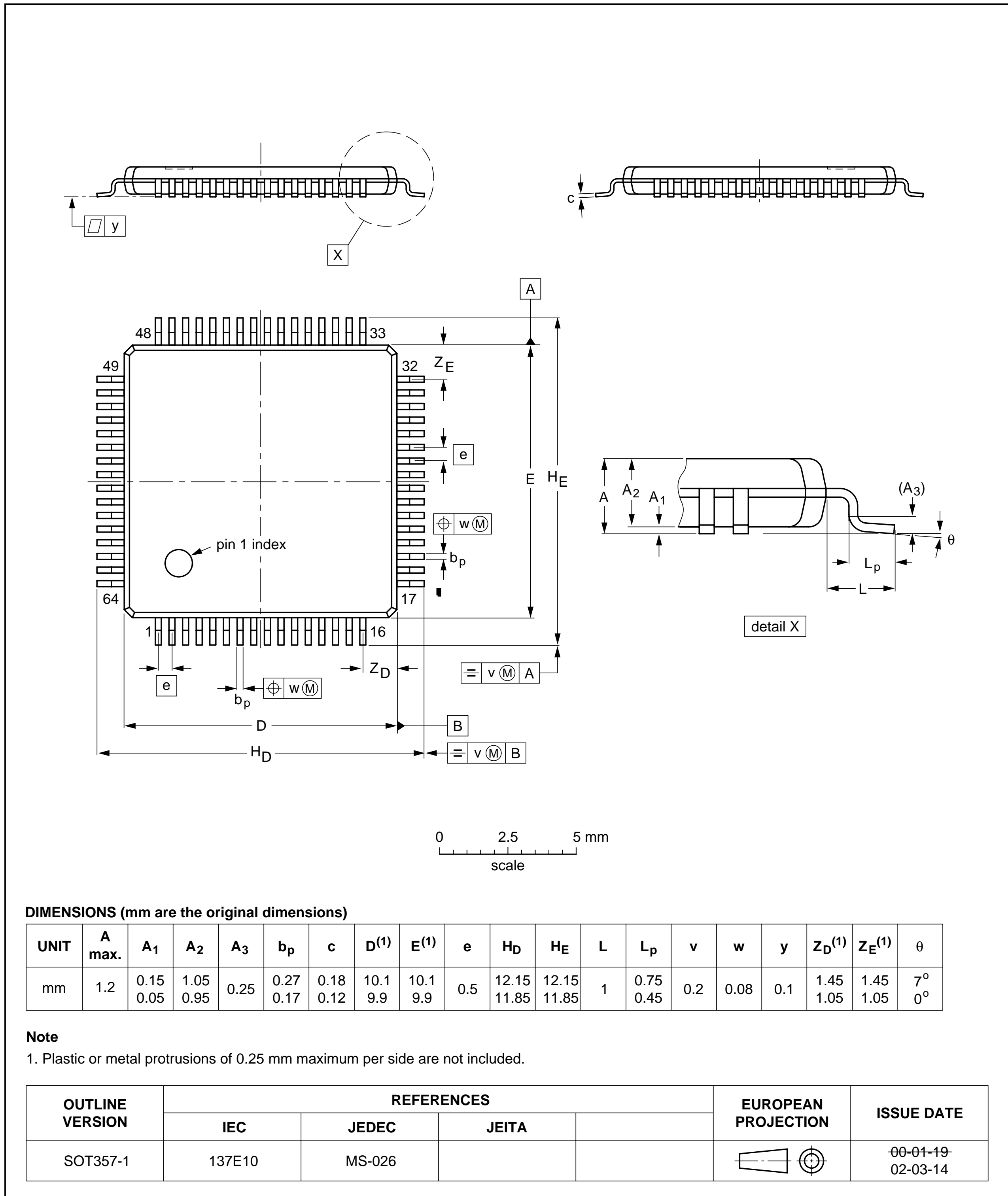
10. Package outline

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm **SOT357-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT357-1	137E10	MS-026				~~00-01-19~~ 02-03-14

Fig 8. Package outline SOT357-1 (TQFP64)

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11. Soldering

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

11.5 Package related soldering information

Table 5: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

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12. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA10023HT_SDS_1	20050412	Product data sheet	-	9397 750 14559	-

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13. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Date of release: 12 April 2005
Document number: 9397 750 14559

Published in The Netherlands