# 8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible

## 54/74ACT651 54/74ACT652

### Features/Benefits

- **Bidirectional bus transceiver and register**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low quiescent supply current of <10 μA (typical)**
- **Active supply current at about 20% LS equivalent**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C**

### Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | OUTPUT | TECH |
|---|---|---|---|---|---|
| 54ACT651 | JS,W, L28 | Mil | Invert | 3-state | CMOS |
| 74ACT651 | NS,JS | Com | | | |
| 54ACT652 | JS,W, L28 | Mil | Non-invert | | |
| 74ACT652 | NS,JS | Com | | | |

### Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT651/652 are given in the Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

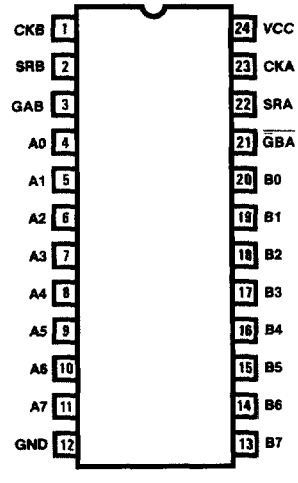
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{GBA}$.

When GAB is low and $\overline{GBA}$ is high, data from the buses can be loaded into registers A and B. When $\overline{GBA}$ is low, the A bus is configured for output. When GAB is high, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

### Pin Configuration

'ACT651/652
8-Bit Bus Front-Loading Latch Transceiver

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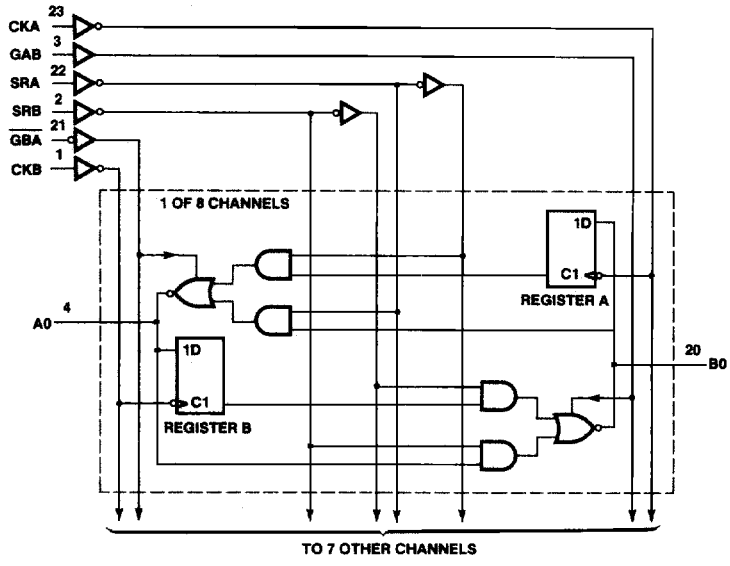
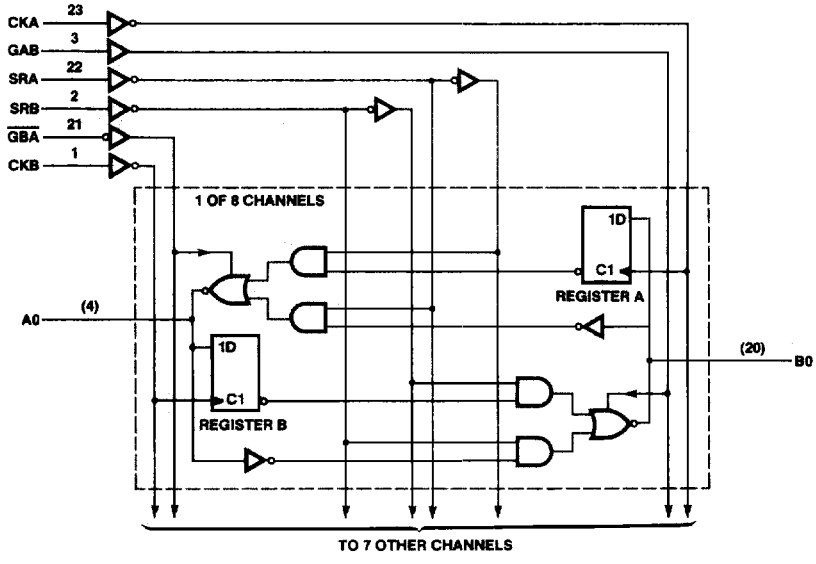
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

## Logic Diagrams

'ACT651 (Inverting)




'ACT652 (Non-Inverting)

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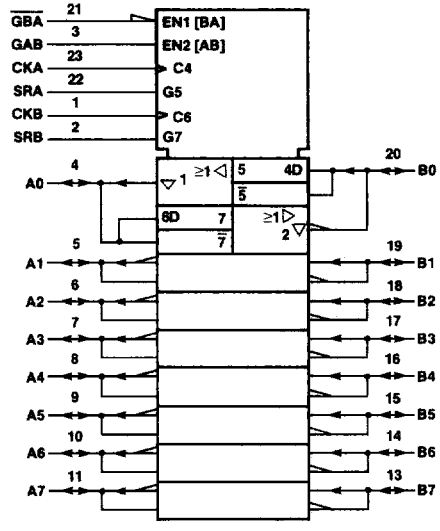
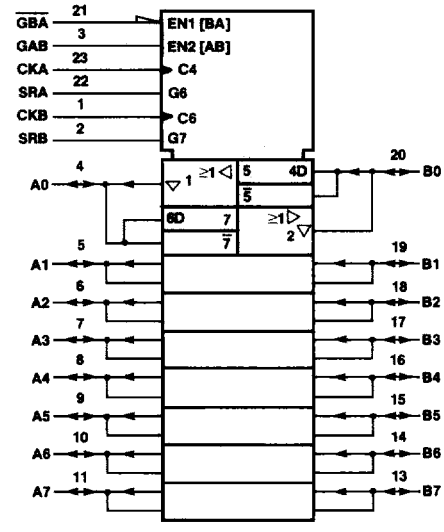
## IEEE Symbols

'ACT651

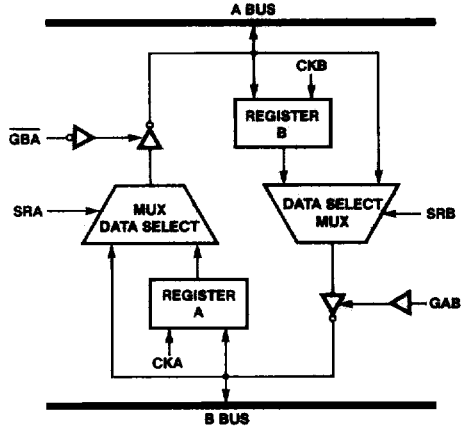



'ACT652

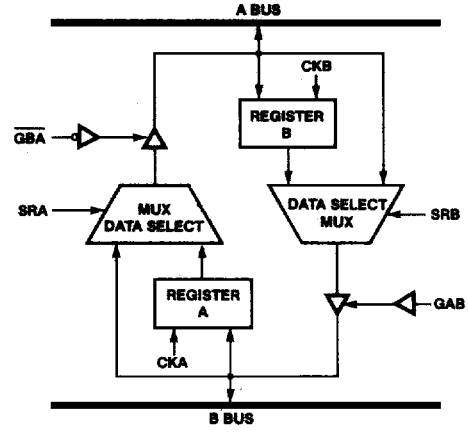



## Block Diagrams

'ACT651 (Inverting)




'ACT652 (Non-Inverting)



## Function Table
## Nomenclature Description

**GAB:** To enable A-to-B operation.

**$\overline{GBA}$:** To enable B-to-A operation.

| GAB | $\overline{GBA}$ | OPERATION DIRECTION |
|---|---|---|
| L | L | B-to-A |
| L | H | A and B buses both are inputs (Storage) |
| H | L | A and B buses both are outputs (Transfer stored data to bus) |
| H | H | A-to-B |

**SRA/SRB:** To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

**A0-A7:** Eight input/output pins on the A side.

**B0-B7:** Eight input/output pins on the B side.

**CKA/CKB:** Clock for register A/B.

**X:** H or L state irrelevant ("Don't Care" condition).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

**UC:** H or L or ↓ case (nonclocked operation).

**RGTR:** Register.

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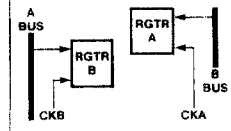
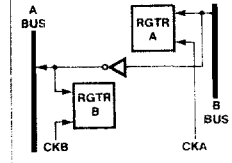
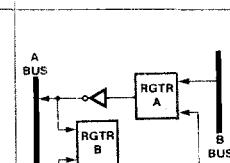
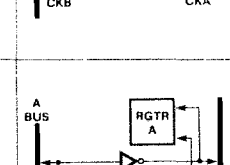
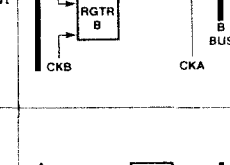
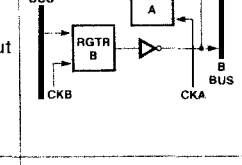
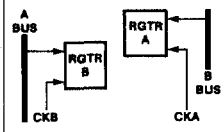
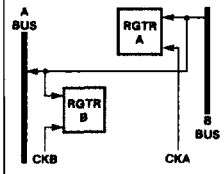
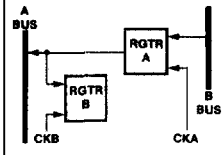
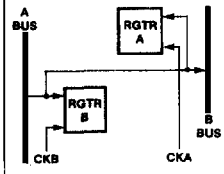
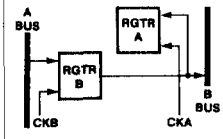
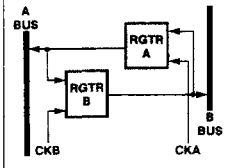
## Bus Operation for 'ACT651

| OPERATION | CONTROL | | | | DATA I/O | | BLOCK DIAGRAM | CLOCK ENABLE | | 'ACT651 |
|---|---|---|---|---|---|---|---|---|---|---|
| | GAB | $\overline{GBA}$ | SRA | SRB | A0-A7 | B0-B7 | | CKA | CKB | |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
| | | | | | | | | UC | ↑ | Real time A bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time B bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time A bus data → RGTR B<br>Real time B bus data → RGTR A |
| Real time B-to-A Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $\overline{B}$ bus data → A bus |
| | | | | | | | | UC | ↑ | Real time $\overline{B}$ bus data → A bus<br>Real time $\overline{B}$ bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time $\overline{B}$ bus data → A bus<br>Real time B bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time $\overline{B}$ bus data → A bus<br>Real time B bus data → RGTR A<br>Real time $\overline{B}$ bus data → RGTR B |
| Stored data B-to-A Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $\overline{A}$ data → A bus |
| | | | | | | | | UC | ↑ | RGTR $\overline{A}$ data → A bus<br>RGTR $\overline{A}$ data → RGTR B |
| | | | | | | | | ↑ | UC | Real time B bus data → RGTR A<br>RGTR $\overline{A}$ data → A bus |
| | | | | | | | | ↑ | ↑ | Real time B bus data → RGTR A<br>RGTR $\overline{A}$ data → A bus<br>RGTR $\overline{A}$ data → RGTR B |
| Real time A-to-B Operation | H | H | X | L | Input | Output |  | UC | UC | Real time $\overline{A}$ bus data → B bus |
| | | | | | | | | UC | ↑ | Real time $\overline{A}$ bus data → B bus<br>Real time A bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time $\overline{A}$ bus data → B bus<br>Real time $\overline{A}$ bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time $\overline{A}$ bus data → B bus<br>Real time $\overline{A}$ bus data → RGTR A<br>Real time A bus data → RGTR B |
| Stored data A-to-B Operation | H | H | X | H | Input | Output |  | UC | UC | RGTR $\overline{B}$ data → B bus |
| | | | | | | | | UC | ↑ | Real time A bus data → RGTR B<br>RGTR $\overline{B}$ data → B bus |
| | | | | | | | | ↑ | UC | RGTR $\overline{B}$ data → B bus<br>RGTR $\overline{B}$ data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time A bus data → RGTR B<br>RGTR $\overline{B}$ data → B bus<br>RGTR $\overline{B}$ data → RGTR A |
| Transfer Stored Data | H | L | H | H | Output | Output |  | UC | UC | RGTR $\overline{A}$/$\overline{B}$ data → A/B bus |
| | | | | | | | | UC | ↑ | RGTR $\overline{A}$/$\overline{B}$ data → A/B bus<br>RGTR $\overline{A}$ data → RGTR B |
| | | | | | | | | ↑ | UC | RGTR $\overline{A}$/$\overline{B}$ data → A/B bus<br>RGTR $\overline{B}$ data → RGTR A |
| | | | | | | | | ↑ | ↑ | RGTR $\overline{A}$/$\overline{B}$ data → A/B bus<br>RGTR $\overline{A}$ data → RGTR B<br>RGTR $\overline{B}$ data → RGTR A |

## Bus Operation for 'ACT652

| OPERATION | CONTROL | | | | DATA I/O | | BLOCK DIAGRAM | CLOCK ENABLE | | 'ACT652 |
|---|---|---|---|---|---|---|---|---|---|---|
| | GAB | $\overline{GBA}$ | SRA | SRB | A0-A7 | B0-B7 | | CKA | CKB | |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
| | | | | | | | | UC | ↑ | Real time A bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time B bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time A bus data → RGTR B<br>Real time B bus data → RGTR A |
| Real time B-to-A Operation | L | L | L | X | Output | Input |  | UC | UC | Real time B bus data → A bus |
| | | | | | | | | UC | ↑ | Real time B bus data → A bus<br>Real time B bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time B bus data → A bus<br>Real time B bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time B bus data → A bus<br>Real time B bus data → RGTR A<br>Real time B bus data → RGTR B |
| Stored data B-to-A Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR A data → A bus |
| | | | | | | | | UC | ↑ | RGTR A data → A bus<br>RGTR A data → RGTR B |
| | | | | | | | | ↑ | UC | Real time B bus data → RGTR A<br>RGTR A data → A bus |
| | | | | | | | | ↑ | ↑ | Real time B bus data → RGTR A<br>RGTR A data → A bus<br>RGTR A data → RGTR B |
| Real time A-to-B Operation | H | H | X | L | Input | Output |  | UC | UC | Real time A bus data → B bus |
| | | | | | | | | UC | ↑ | Real time A bus data → B bus<br>Real time A bus data → RGTR B |
| | | | | | | | | ↑ | UC | Real time A bus data → B bus<br>Real time A bus data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time A bus data → B bus<br>Real time A bus data → RGTR A<br>Real time A bus data → RGTR B |
| Stored data A-to-B Operation | H | H | X | H | Input | Output |  | UC | UC | RGTR B data → B bus |
| | | | | | | | | UC | ↑ | Real time A bus data → RGTR B<br>RGTR B data → B bus |
| | | | | | | | | ↑ | UC | RGTR B data → B bus<br>RGTR B data → RGTR A |
| | | | | | | | | ↑ | ↑ | Real time A bus data → RGTR B<br>RGTR B data → B bus<br>RGTR B data → RGTR A |
| Transfer Stored Data | H | L | H | H | Output | Output |  | UC | UC | RGTR A/B data → A/B bus |
| | | | | | | | | UC | ↑ | RGTR A/B data → A/B bus<br>RGTR A data → RGTR B |
| | | | | | | | | ↑ | UC | RGTR A/B data → A/B bus<br>RGTR B data → RGTR A |
| | | | | | | | | ↑ | ↑ | RGTR A/B data → A/B bus<br>RGTR A data → RGTR B<br>RGTR B data → RGTR A |

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## Absolute Maximum Ratings

Supply voltage, $V_{CC}$ ..... −0.5 V to 7.0 V
DC input voltage, $V_I$ ..... −0.5 V to $V_{CC}$ +0.5 V
DC output voltage, $V_O$ ..... −0.5 V to $V_{CC}$+0.5 V
DC output source/sink current per output pin, $I_O$ ..... ±35 mA
DC $V_{CC}$ or ground current, $I_{CC}$ or $I_{GND}$ ..... ±100 mA
Input diode current, $I_{IK}$:
$V_I$ <0 ..... −20 mA
$V_I$ >$V_{CC}$ ..... +20 mA
Output diode current, $I_{OK}$:
$V_O$ <0 ..... −20 mA
$V_O$ >$V_{CC}$ ..... +20 mA
Storage temperature ..... −65 to +150°C

## Operating Conditions

| SYMBOL | PARAMETER | | MILITARY MIN | MILITARY TYP | MILITARY MAX | COMMERCIAL MIN | COMMERCIAL TYP | COMMERCIAL MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |
| $t_w$ | Width of clock | High | 20 | | | 20 | | | ns |
| | | Low | 20 | | | 20 | | | |
| $t_{su}$ | Set up time | | 30↑ | | | 25↑ | | | ns |
| $t_h$ | Hold time | | 0↑ | | | 0↑ | | | ns |
| $t_r$ | Input rise time at $V_I$ = 4.5 V | | 0 | | 500 | 0 | | 500 | ns |
| $t_f$ | Input fall time at $V_I$ = 4.5 V | | 0 | | 500 | 0 | | 500 | ns |
| $I_{OH}$ | High-level output current | | | | −6 | | | −6 | mA |
| $I_{OL}$ | Low-level output current | | | | 12 | | | 12 | mA |

↑ The arrow indicates the Low-to-High transition of the clock input used as reference.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | | 25°C MIN | 25°C TYP | 25°C MAX | MILITARY MIN | MILITARY TYP | MILITARY MAX | COMMERCIAL MIN | COMMERCIAL TYP | COMMERCIAL MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.7 | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | 2 | | | V |
| $I_{IN}$ | Input Current | $V_{CC}$ = MAX | $V_I$ = $V_{CC}$ or GND | | | ±1.0 | | | ±1.0 | | | ±1.0 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = 20 μA | | | 0.1 | | | 0.1 | | | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | | | 0.32 | | | 0.4 | | | 0.37 | |
| | | | $I_{OL}$ = 12 mA | | | 0.4 | | | 0.4 | | | 0.4 | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = -20 μA | 3.4 | | | 3.4 | | | 3.4 | | | V |
| | | | $I_{OH}$ = -6 mA | 2.4 | | | 2.4 | | | 2.4 | | | |
| $I_{OZ}$ | Off-state output current | $V_{CC}$ = MAX | $V_O$ = $V_{CC}$ or GND | | | ±10 | | | ±50 | | | ±30 | μA |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = MAX | $V_I$ = $V_{CC}$ or GND | | | 10 | | | 80 | | | 40 | μA |
| $I_C$ | Maximum quiescent supply current | $V_{CC}$ = MAX | Only one input at 2.4 V | | | 1.5 | | | 2.0 | | | 1.9 | mA |
| | | $V_I$ = 2.4 V or 0.5 V | All inputs at 2.4 V | | | 25 | | | 35 | | | 33 | |

## Switching Characteristics

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveform) | COM/MIL $T_A$ = 25°C MIN | COM/MIL $T_A$ = 25°C MAX | MILITARY MIN | MILITARY MAX | COMMERCIAL MIN | COMMERCIAL MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to output delay | $C_L$ = 50 pF | | 39 | | 53 | | 48 | ns |
| $t_{PHL}$ | | | | 30 | | 48 | | 42 | |
| $t_{PLH}$ | Clock to output delay | | | 35 | | 50 | | 44 | ns |
| $t_{PHL}$ | | | | 30 | | 44 | | 40 | |
| $t_{PLH}$ | Select to output delay* (data input high) | | | 32 | | 44 | | 40 | ns |
| $t_{PHL}$ | | | | 32 | | 44 | | 40 | |
| $t_{PLH}$ | Select to output delay* (data input low) | | | 35 | | 50 | | 44 | ns |
| $t_{PHL}$ | | | | 30 | | 40 | | 36 | |
| $t_{PZL}$ | $\overline{GBA}$ to A bus output enable delay | $R_L$ = 1KΩ, $C_L$ = 50 pF | | 25 | | 35 | | 32 | ns |
| $t_{PZH}$ | | | | 25 | | 35 | | 32 | |
| $t_{PLZ}$ | $\overline{GBA}$ to A bus output disable delay | | | 25 | | 35 | | 32 | ns |
| $t_{PHZ}$ | | | | 35 | | 40 | | 38 | |
| $t_{PZL}$ | GAB to B bus output enable delay | | | 30 | | 35 | | 33 | ns |
| $t_{PZH}$ | | | | 25 | | 35 | | 32 | |
| $t_{PLZ}$ | GAB to B bus output disable delay | | | 25 | | 35 | | 32 | ns |
| $t_{PHZ}$ | | | | 35 | | 40 | | 38 | |

* See Figure 4.

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## Test Waveforms

**Setup Time/Hold Time**

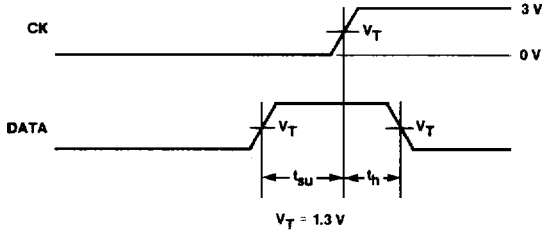



Figure 1

**Bus Data To Bus Output Delay**

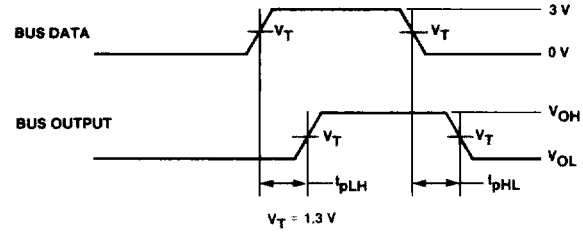



Figure 2

**CK To Bus Output Propagation Delay Time**

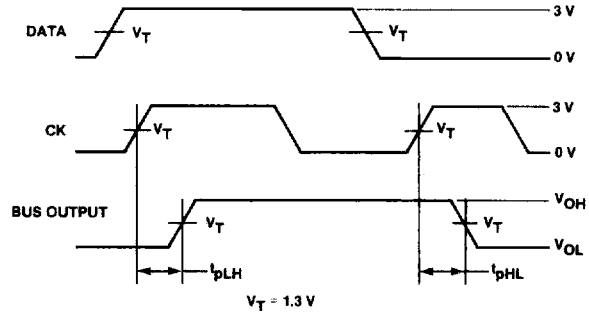
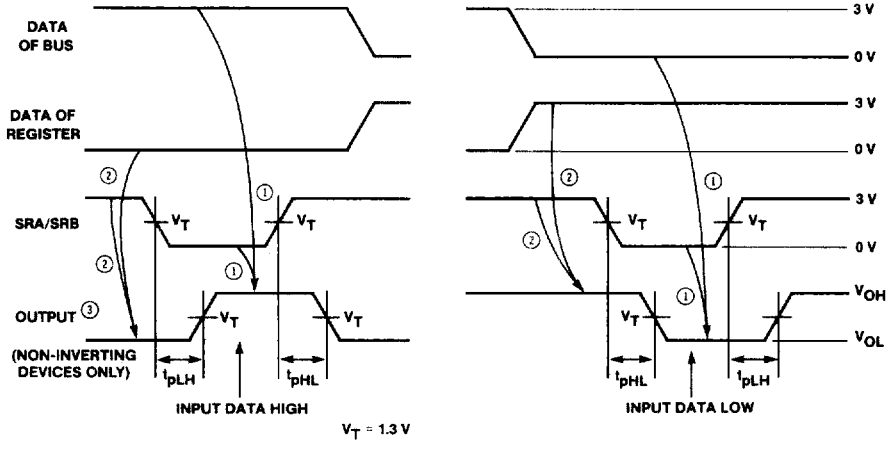



Figure 3

**Select To Output Delay**




NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4

## Enable/Disable/Direction-Change Delay

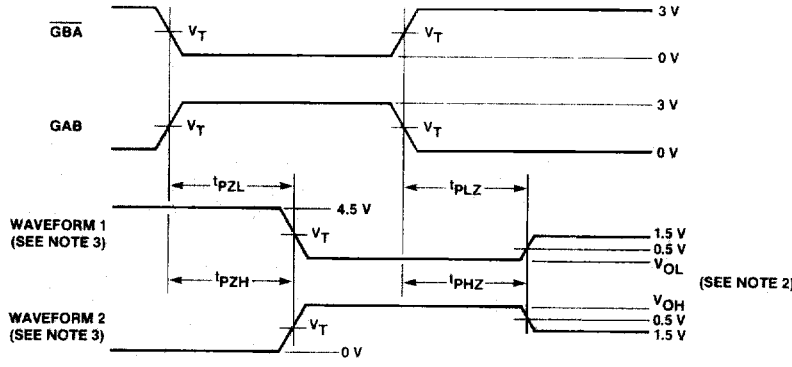



Figure 5

## Test Load

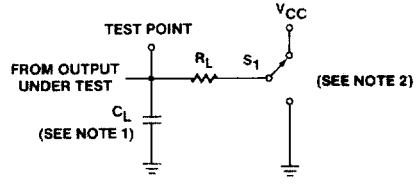



Figure 6

NOTES 1. $C_L$ includes probe and jig capacitance.

2. When measuring $t_{PLZ}$ and $t_{PZL}$, $S_1$ is tied to $V_{CC}$. When measuring $t_{PHZ}$ and $t_{PZH}$, $S_1$ is tied to ground.

   When measuring propagation delay times of three-state outputs, $S_1$ is open, i.e., not connected to $V_{CC}$ or ground.

3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

5. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_{out}$ = 50 Ω.

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## Die Configurations

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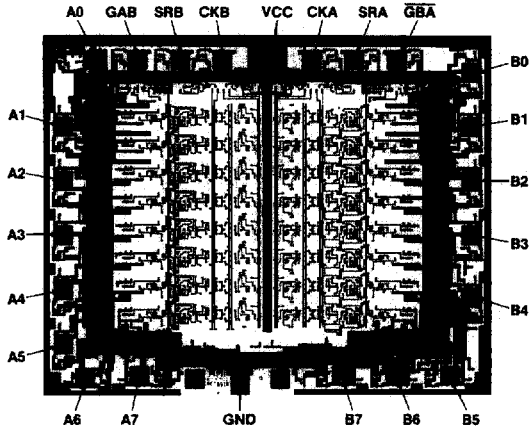
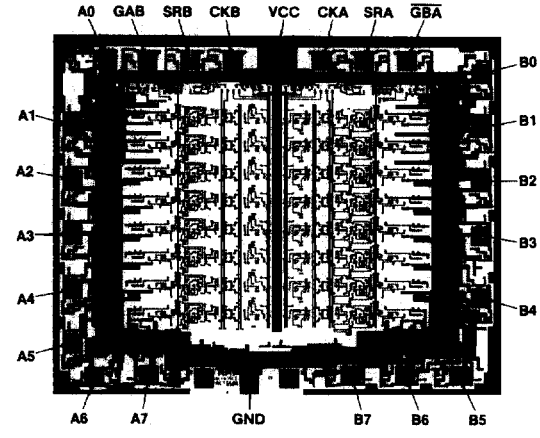



54/74ACT652




Die Size: 87x107 mil$^2$