



4-Pin μ P Voltage Supervisor with Manual Reset

General Description

The ASM811/ASM812 are cost effective low power supervisors designed to monitor voltage levels of 3.0V, 3.3V and 5.0V power supplies in low-power microprocessor (μ P), microcontroller (μ C) and digital systems. They provide excellent reliability by eliminating external components and adjustments.

A reset signal is issued if the power supply voltage drops below a preset reset threshold and is asserted for at least 140ms after the supply has risen above the reset threshold. The ASM811 has an active-low output $\overline{\text{RESET}}$ that is guaranteed to be in the correct state for V_{CC} down to 1.1V. The ASM812 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC} . A debounced manual reset input allows the user to manually reset the systems to bring them out of locked state.

Low power consumption makes the ASM811/ASM812 ideal for use in portable and battery operated equipment. The ASM811/ASM812 are available in a compact 4-pin SOT-143 package and thus use minimal board space.

Applications

- Computers and Controllers
- Embedded controllers
- Portable/Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipments
- Automotive systems
- Safety Systems

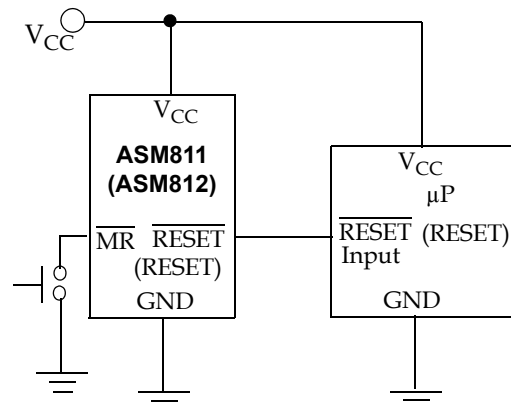
Six voltage thresholds are available to support 3V to 5V systems:

RESET THRESHOLD	
Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

Features

- New 4.0V threshold option
- 6 μ A supply current
- Monitor 5V, 3.3V and 3V supplies
- Manual reset input
- 140ms min. reset pulse width
- Guaranteed over temperature
- Active-low reset valid with 1.1V supply (ASM811)
- Small 4-pin SOT-143 package
- No external components
- Power-supply transient-immune design

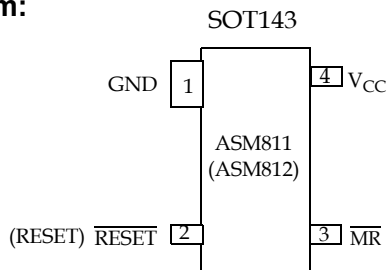
Typical Operating Circuit



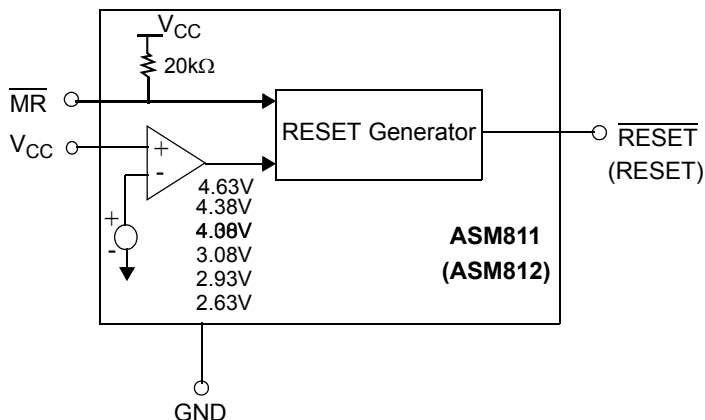


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Pin Diagram:



Block Diagram



Pin Description

Pin #		Pin Name	Function
ASM811	ASM812		
1	1	GND	Ground.
2	-	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is asserted LOW if V_{CC} falls below V_{TH} . $\overline{\text{RESET}}$ remains LOW for atleast 140ms (T_{RST}) once V_{CC} exceeds the Threshold. In addition, $\overline{\text{RESET}}$ is active LOW as long as the manual reset ($\overline{\text{MR}}$) is low.
-	2	RESET	RESET is asserted HIGH if V_{CC} falls below V_{TH} . RESET remains HIGH for atleast 140ms (T_{RST}) once V_{CC} exceeds the threshold. In addition, RESET is active HIGH as long as the manual reset ($\overline{\text{MR}}$) is low.
3	3	$\overline{\text{MR}}$	Manual Reset Input. A logic LOW on $\overline{\text{MR}}$ asserts reset. Reset remains active as long as $\overline{\text{MR}}$ is LOW and for atleast 180ms (T_{MRST}) once $\overline{\text{MR}}$ returns HIGH. The active low input has an internal 20kΩ pull-up resistor. The input should be left open if not used. It can be driven by TTL or CMOS logic or shorted to ground by a switch.
4	4	V_{CC}	Power supply input voltage (3.0V, 3.3V, 5.0V)

Detailed Description

A proper reset input enables a microprocessor / microcontroller to start in a known state. ASM811/812 assert reset to prevent code execution errors during power-up, power-down and brown-out conditions.

Reset Timing

The reset signal is asserted- LOW for the ASM811 and HIGH for the ASM812- when the V_{CC} supply voltage falls below the threshold trip voltage and remains asserted for 140ms minimum after the V_{CC} has risen above the threshold.

Manual Reset ($\overline{\text{MR}}$) Input

A logic low on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$ LOW on the ASM811 and RESET HIGH on the ASM812. $\overline{\text{MR}}$ is internally pulled high through a 20kΩ resistor and can be driven by TTL/CMOS gates or with open collector/drain outputs. $\overline{\text{MR}}$ can be left open if not used. $\overline{\text{MR}}$ may be connected to ground through a normally-open momentary switch without an external debounce circuit.

A 0.1μF capacitor from $\overline{\text{MR}}$ to ground can be added for additional noise immunity.



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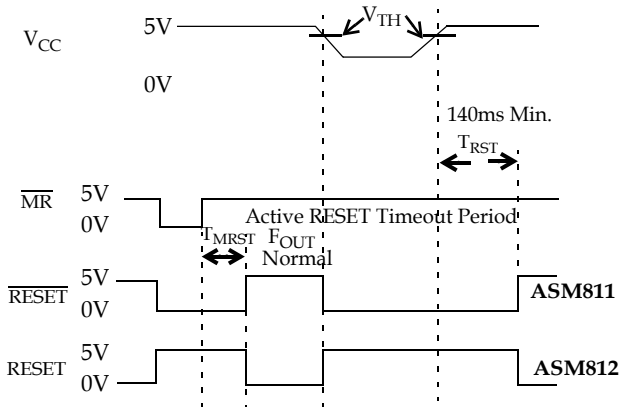


Figure 1: Reset Timing and Manual Reset (\overline{MR})

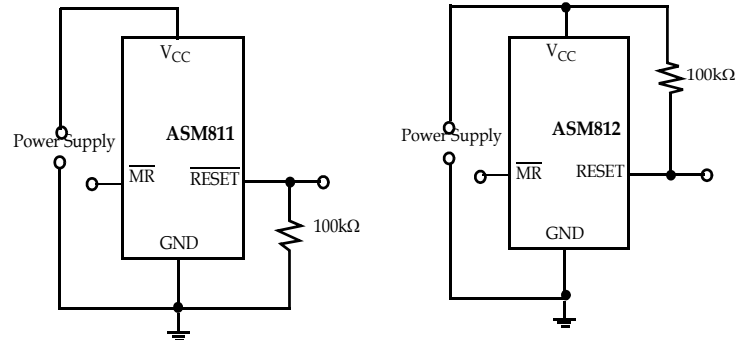
Reset Output Operation

In $\mu P / \mu C$ systems it is important to have the processor and the system begin operation from a known state. A reset output to a processor is provided to prevent improper operation during power supply sequencing or low voltage brown-out conditions.

The ASM811/812 are designed to monitor the system power supply voltages and issue a reset signal when the levels are out of range. RESET outputs are guaranteed to be active for V_{CC} above 1.1V. When V_{CC} exceeds the reset threshold, an internal timer keeps RESET active for the reset timeout period, after which RESET becomes inactive (HIGH for the ASM811 and LOW for the ASM812). If V_{CC} drops below the reset threshold, RESET automatically becomes active. Alternatively, external circuitry or an operator can initiate this condition using the Manual Reset (\overline{MR}) pin. \overline{MR} can be left open if it is not used. \overline{MR} can be driven by TTL/CMOS logic or even an external switch.

Valid Reset with V_{CC} under 1.1V

To ensure logic inputs connected to the ASM811 \overline{RESET} pin are in a known state when V_{CC} is under 1.1V, a 100k Ω pull-down resistor at \overline{RESET} is needed. The value is not critical. A 100k Ω pull-up resistor to V_{CC} at \overline{RESET} is needed with the ASM812.



Figures 2 & 3: RESET valid with V_{CC} under 1.1V

Application Information

Negative VCC Transients

Typically short duration transients of 100mV amplitude and 60 μs duration do not cause a false RESET. A 0.1 μF capacitor at V_{CC} increases transient immunity.

Bidirectional Reset Pin Interfacing

The ASM811/812 can interface with $\mu P / \mu C$ bi-directional reset pins by connecting a 4.7k Ω resistor in series with the ASM811/812 reset output and the $\mu P / \mu C$ bi-directional reset input pin.

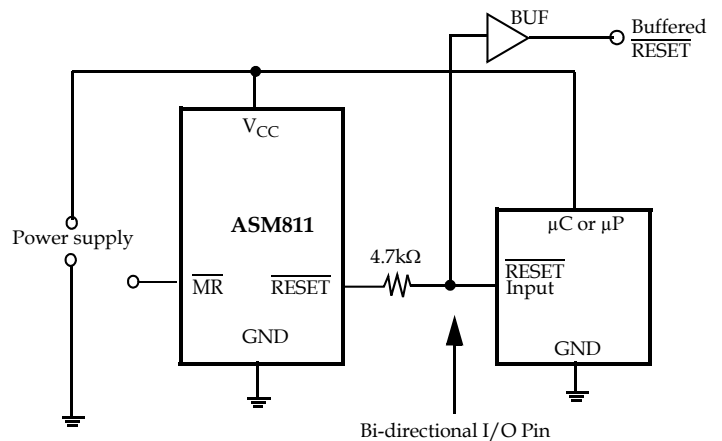


Figure 4: Bi-directional Reset Pin Interface



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Absolute Maximum Ratings, Table 1:

Parameter	Min	Max	Units
Pin Terminal Voltage With Respect To Ground			
V_{CC}	-0.3	6.0	V
RESET, $\overline{\text{RESET}}$ and $\overline{\text{MR}}$	-0.3	$V_{CC} + 0.3$	V
Input current at V_{CC} and $\overline{\text{MR}}$		20	mA
Output current: RESET, $\overline{\text{RESET}}$		20	mA
Rate of Rise at V_{CC}		100	V/ μ s
ESD rating		2	KV
HBM		200	V
MM			
Note: These are stress ratings only and the functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.			

Absolute Maximum Ratings, Table 2:

Parameter	Min	Max	Units
Power Dissipation ($T_A = 70^\circ\text{C}$) Derate SOT-143 4mW/ $^\circ\text{C}$ above 70°C		320	mW
Operating temperature range	-40	105	$^\circ\text{C}$
Storage temperature range	-65	160	$^\circ\text{C}$
Lead temperature (Soldering, 10 sec)		300	$^\circ\text{C}$
Note: These are stress ratings only and the functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.			



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Electrical Characteristics:

Unless otherwise noted, V_{CC} is over the full voltage range, $T_A = -40^{\circ}\text{C}$ to 105°C .
 Typical values at $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5\text{V}$ for L/M/J devices, $V_{CC} = 3.3\text{V}$ for T/S devices and $V_{CC} = 3\text{V}$ for R devices.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{CC}	Input Voltage Range	$T_A = 0^{\circ}\text{C}$ to 70°C	1.1		5.5	V	
		$T_A = -40^{\circ}\text{C}$ to 105°C	1.2		5.5	V	
I_{CC}	Supply Current (Unloaded)	$T_A = -40^{\circ}\text{C}$ to 85°C $V_{CC} < 5.5\text{V}$, L/M/J		6	15	μA	
		$T_A = -40^{\circ}\text{C}$ to 85°C $V_{CC} < 3.6\text{V}$, R/S/T		5	10		
		$T_A = 85^{\circ}\text{C}$ to 105°C $V_{CC} < 5.5\text{V}$, L/M/J			25		
		$T_A = 85^{\circ}\text{C}$ to 105°C $V_{CC} < 3.6\text{V}$, R/S/T			20		
V_{TH}	Reset Threshold	L devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	4.56 4.50 4.40	4.63	4.70 4.75 4.86	V
		M devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	4.31 4.25 4.16	4.38	4.45 4.50 4.56	
		J devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	3.93 3.89 3.80	4.00	4.06 4.10 4.20	
		T devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	3.04 3.00 2.92	3.08	3.11 3.15 3.23	
		S devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	2.89 2.85 2.78	2.93	2.96 3.00 3.08	
		R devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C}$ to 85°C $T_A = 85^{\circ}\text{C}$ to 105°C	2.59 2.55 2.50	2.63	2.66 2.70 2.76	
TC_{VTH}	Reset Threshold Temp. Coefficient			30		ppm/ $^{\circ}\text{C}$	
	V_{CC} to Reset Delay	$V_{CC} = V_{TH}$ to $(V_{TH} - 125\text{mV})$,		60		μs	
T_{RST}	Reset Active Timeout Period	$T_A = 0^{\circ}\text{C}$ to 70°C	140		560	ms	
		$T_A = -40^{\circ}\text{C}$ to 105°C	100	240	840		
t_{MR}	$\overline{\text{MR}}$ Minimum Pulse Width		10			μs	
	$\overline{\text{MR}}$ Glitch Immunity	Note 3		100		ns	

Notes:

1. Production testing done at $T_A = 25^{\circ}\text{C}$. Over-temperature specifications guaranteed by design only using six sigma design limits.
2. RESET output is active LOW for the ASM811 and RESET output is active HIGH for the ASM812.
3. Glitches of 100ns or less typically will not generate a reset pulse.



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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{MD}	\overline{MR} to RESET Propagation Delay	Note 2		0.5		μs
V_{IH}	\overline{MR} Input Threshold	$V_{CC} > V_{TH} (MAX)$, ASM811/812L/M/J	2.3			V
V_{IL}					0.8	
V_{IH}	\overline{MR} Input Threshold	$V_{CC} > V_{TH} (MAX)$, ASM811/812R/S/T	$0.7V_{CC}$			V
V_{IL}					$0.25V_{CC}$	
	\overline{MR} Pullup Resistance		10	20	30	$k\Omega$
V_{OL}	Low \overline{RESET} Output Voltage (ASM811)	$V_{CC} = V_{TH} \text{ min.}, I_{SINK} = 1.2mA$, ASM811R/S/T			0.3	V
		$V_{CC} = V_{TH} \text{ min.}, I_{SINK} = 3.2mA$, ASM811L/M/J			0.4	
		$V_{CC} > 1.1V, I_{SINK} = 50\mu A$			0.3	
V_{OH}	High \overline{RESET} Output Voltage (ASM811)	$V_{CC} > V_{TH} \text{ max.}, I_{SOURCE} = 500\mu A$, ASM811R/S/T	$0.8V_{CC}$			V
		$V_{CC} > V_{TH} \text{ max.}, I_{SOURCE} = 800\mu A$, ASM811L/M/J	$V_{CC} - 1.5$			
V_{OL}	Low RESET Output Voltage (ASM812)	$V_{CC} = V_{TH} \text{ max.}, I_{SINK} = 1.2mA$, ASM812R/S/T			0.3	V
		$V_{CC} = V_{TH} \text{ max.}, I_{SINK} = 3.2mA$, ASM812L/M/J			0.4	
V_{OH}	High RESET Output Voltage (ASM812)	$1.8V < V_{CC} < V_{TH} \text{ min.}, I_{SOURCE} = 150\mu A$	$0.8V_{CC}$			V

Notes:
 1. Production testing done at $T_A = 25^\circ C$. Over-temperature specifications guaranteed by design only using six sigma design limits.
 2. RESET output is active LOW for the ASM811 and RESET output is active HIGH for the ASM812.
 3. Glitches of 100ns or less typically will not generate a reset pulse.

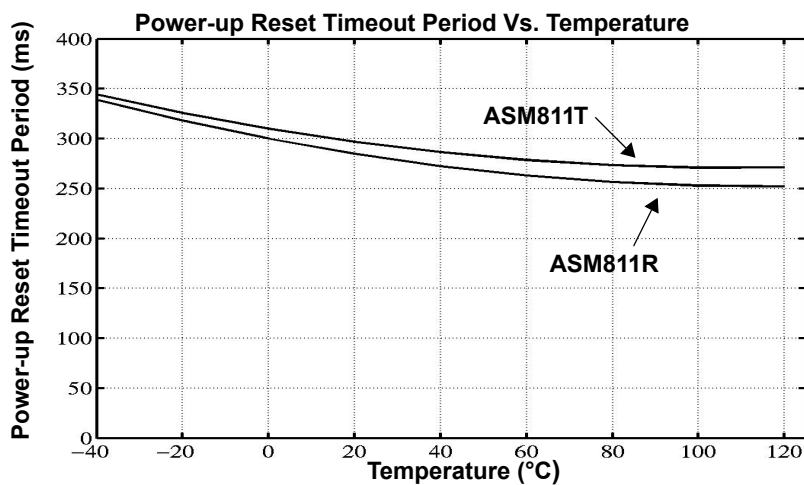
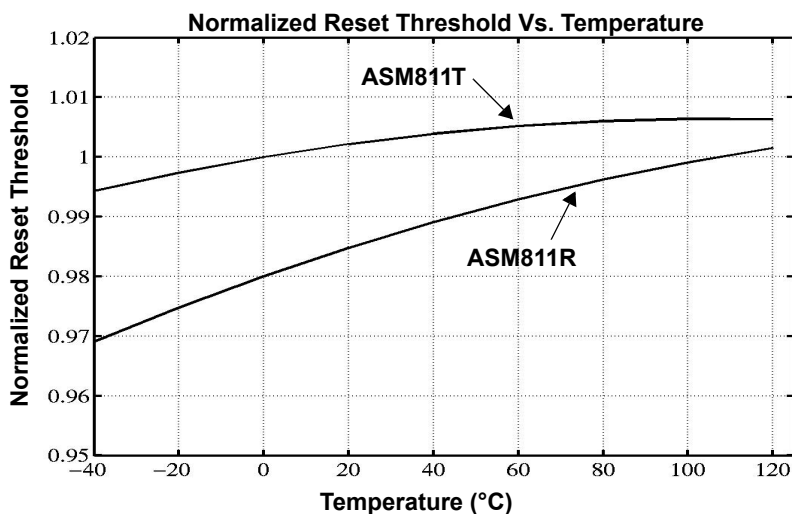
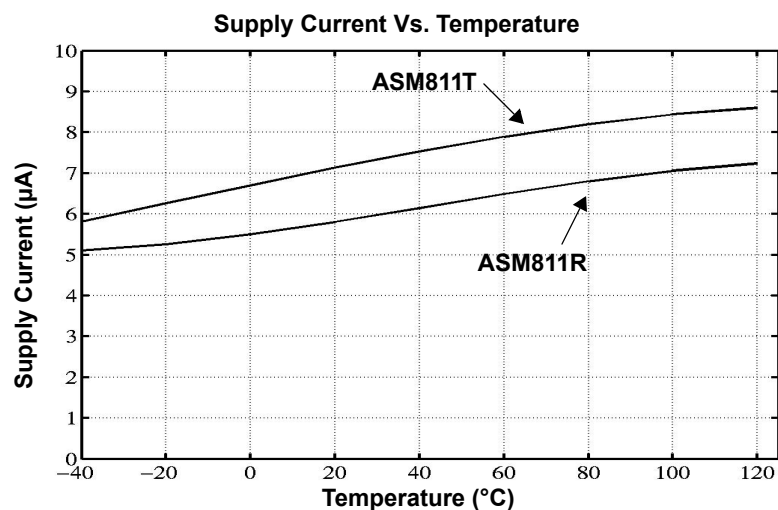


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Typical Operating Characteristics

Unless otherwise noted, V_{CC} is over the full voltage range, $T_A = -40^{\circ}\text{C}$ to 105°C . Typical values at $T_A = 25^{\circ}\text{C}$,

$V_{CC} = 5\text{V}$ for L/M/J devices, $V_{CC} = 3.3\text{V}$ for T/S devices and $V_{CC} = 3\text{V}$ for R devices.

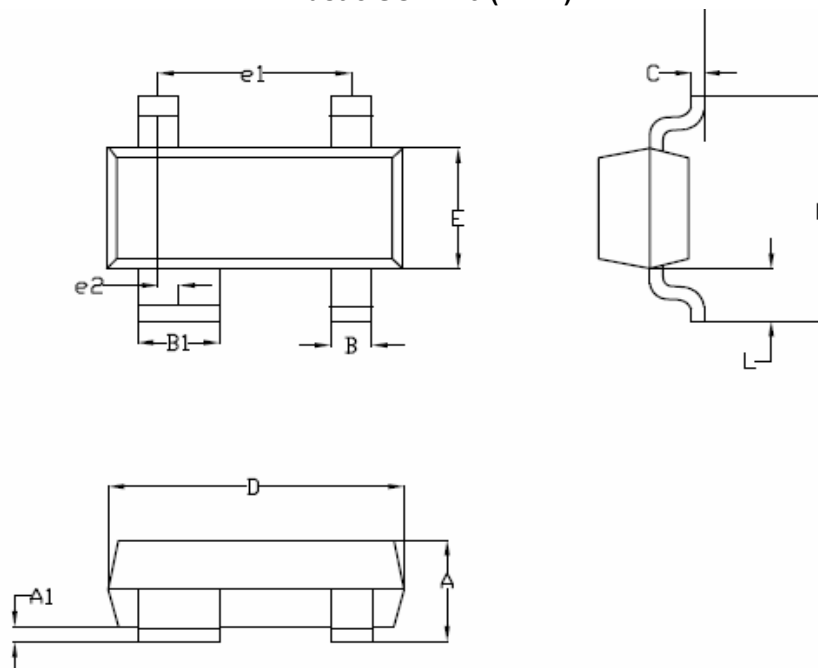




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Package Dimensions:

Plastic SOT-143 (4-Pin)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.031	0.048	0.80	1.22
A1	0.002	0.006	0.05	0.15
B	0.012	0.020	0.30	0.50
B1	0.030	0.035	0.76	0.89
C	0.003	0.008	0.08	0.20
D	0.110	0.120	2.80	3.04
E	0.047	0.055	1.20	1.40
e1	0.075BSC		1.92 BSC	
e2	0.181 BSC		4.60 BSC	
H	0.083	0.104	2.10	2.64
L	0.016	0.024	0.400	0.600



Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pin-Package	Package Marking (LL Lot Code)
ASM811 ACTIVE LOW RESET, TIN-LEAD PLATED DEVICES				
ASM811LEUS	4.63	-40°C to +105°C	4-SOT143	SMLL
ASM811MEUS	4.38	-40°C to +105°C	4-SOT143	SNLL
ASM811JEUS	4.00	-40°C to +105°C	4-SOT143	SOLL
ASM811TEUS	3.08	-40°C to +105°C	4-SOT143	SPLL
ASM811SEUS	2.93	-40°C to +105°C	4-SOT143	SQLL
ASM811REUS	2.63	-40°C to +105°C	4-SOT143	SRLL
ASM812 ACTIVE HIGH RESET, TIN-LEAD PLATED DEVICES				
ASM812LEUS	4.63	-40°C to +105°C	4-SOT143	SSLL
ASM812MEUS	4.38	-40°C to +105°C	4-SOT143	STLL
ASM812JEUS	4.00	-40°C to +105°C	4-SOT143	SULL
ASM812TEUS	3.08	-40°C to +105°C	4-SOT143	SVLL
ASM812SEUS	2.93	-40°C to +105°C	4-SOT143	SWLL
ASM812REUS	2.63	-40°C to +105°C	4-SOT143	SXLL
ASM811 ACTIVE LOW RESET, LEAD FREE DEVICES				
ASM811LEUSF	4.63	-40°C to +105°C	4-SOT143	NMLL
ASM811MEUSF	4.38	-40°C to +105°C	4-SOT143	NNLL
ASM811JEUSF	4.00	-40°C to +105°C	4-SOT143	NOLL
ASM811TEUSF	3.08	-40°C to +105°C	4-SOT143	NPLL
ASM811SEUSF	2.93	-40°C to +105°C	4-SOT143	NQLL
ASM811REUSF	2.63	-40°C to +105°C	4-SOT143	NRLL
ASM812 ACTIVE HIGH RESET, LEAD FREE DEVICES				
ASM812LEUSF	4.63	-40°C to +105°C	4-SOT143	NSLL
ASM812MEUSF	4.38	-40°C to +105°C	4-SOT143	NTLL
ASM812JEUSF	4.00	-40°C to +105°C	4-SOT143	NULL
ASM812TEUSF	3.08	-40°C to +105°C	4-SOT143	NVLL
ASM812SEUSF	2.93	-40°C to +105°C	4-SOT143	NWLL
ASM812REUS	2.63	-40°C to +105°C	4-SOT143	NXLL

Notes:

- For parts to be packed in Tape and Reel, add "-T" at the end of the part number.
- Alliance Semiconductor's lead free parts are RoHS compliant. All parts are Lead Free by default. Contact factory for Non Lead Free devices

April 2005



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Related Products:

	ASM809	ASM810	ASM811	ASM812
Max Supply Current	15 μ A	15 μ A	15 μ A	15 μ A
Package Pins	3	3	4	4
Manual RESET input			■	■
Package Type	SOT - 23	SOT - 23	SOT - 143	SOT - 143
Active-HIGH RESET Output		■		■
Active-LOW $\overline{\text{RESET}}$ Output	■		■	



ASM811, ASM812



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