COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

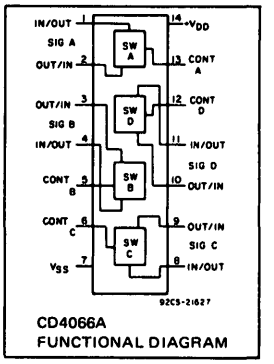
The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- 15-V digital or ± 7.5-V peak-to-peak switching
- 80Ω typical ON resistance for 15-V operation
- Switch ON resistance matched to within 5 Ω over 15-V signal-input range
- ON resistance flat over full peak-to-peak signal range
- High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity: < 0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ
- Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch ON = 40 MHz (typ.)
- Quiescent current specified to 15-V
- Maximum control input leakage current of 1-μA at 15-V (Full package-temperature range)



CD4066A
FUNCTIONAL DIAGRAM

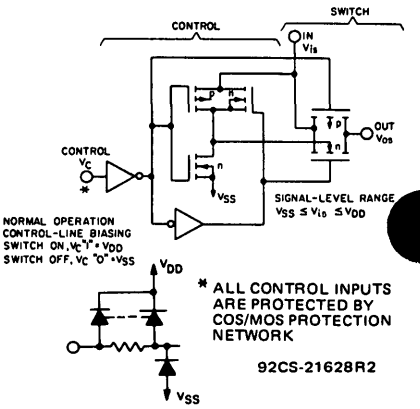


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +125°C

OPERATING TEMPERATURE RANGE (T_A).

PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY VOLTAGE RANGE, V_{DD}

(Voltages referenced to V_{SS}) . . . . . -0.5 to +15 V

INPUT CURRENT (TRANSMISSION GATE INCL.) . . . . . ±10 mA

POWER DISSIPATION PER PACKAGE.

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C . . . . . 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C . . . 200 mW

DEVICE DISSIPATION PER SECTION·

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

ALL SIGNAL AND DIGITAL CONTROL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temperature Range)	–	3	12	V

SPECIAL CONSIDERATIONS – CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.
3. Minimum bilateral switch output load resistance is 100 Ω.

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values are in Volts*			LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
			V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Quiescent Device Current, I_L max. D, F, H Pkgs.			5	0.25	–	–	7.5	0.01	0.25	μA
			10	0.5	–	–	15	0.01	0.5	
			15	2	–	–	40	0.02	2	
E Pkg			5	–	2.5	15	–	0.25	2.5	μA
			10	–	5	30	–	0.25	5	
			15	–	50	500	–	0.5	50	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})										
ON Resistance, R_{ON} Max	$V_C = V_{DD}$	V_{SS}	V_{is}							Ω
	$R_L = 10k\Omega$*									
	+7.5	-7.5	-7.5 to +7.5	220	250	300	320	80	280	
	+15	0	0 to +15							
	+5	-5	-5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	-2.5	-2.5 to +2.5	3000	3500	5200	5500	270	5000	
	-5	0	0 to +5							
Δ_{ON} Resistance Between Any 2 of 4 Switches, ΔR_{ON}	$R_L = 10k\Omega$*									Ω
	+7.5 or +15	-7.5 or 0	+7.5 to -7.5; +15 to 0	–	–	–	–	5	–	
	+5 or +10	-5 or 0	+5 to -5; +10 to 0	–	–	–	–	10	–	
Sine Wave Response (Distortion)	+5	-5	5V p-p▲	–	–	–	–	0.4	–	%
	$R_L = 10k\Omega$, $f_{is} = 1kHz$									
Frequency Response Switch ON (Sine-Wave Input)	+5	-5	-5 p-p	–	–	–	–	40	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -3dB$									
Feedthrough-Switch OFF	+5	-5	-5 p-p	–	–	–	–	1.25	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -50dB$									
Input or Output Leakage – Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C = V_{SS}$	±7.5	–	–	–	–	±0.1	±100*	nA
	+7.5	-7.5								
	+5	-5	±5	–	–	–	–	±0.1	±100*	
Crosstalk Between Any 2 of the 4 Switches (f at -50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$, $R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)} = -50dB$		(A) 5V p-p	–	–	–	–	0.9	–	MHz

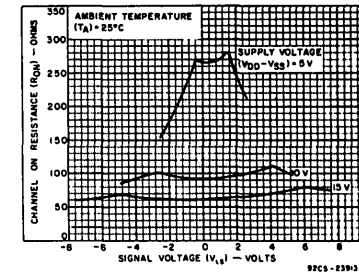


Fig. 2 (a) – Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

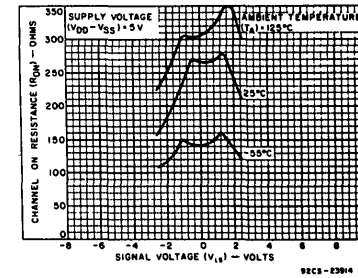


Fig. 2 (b) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

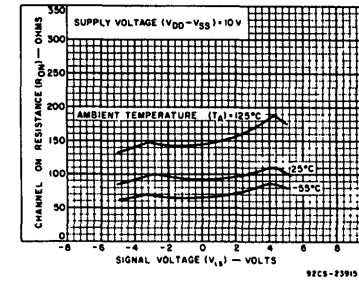


Fig. 2 (c) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

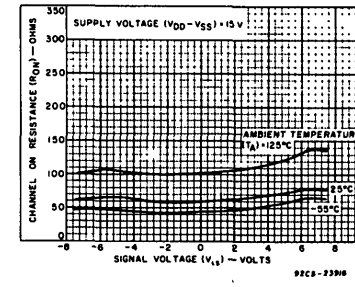


Fig. 2 (d) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

CD4066A Typ s

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*	V_{DD} (V)	LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
			-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$, V_{SS} = GND, C_L = 15pF, V_{IS} = sq wave, t_r, t_f = 20 ns (Input Signal)	V_{DD} = 5	–	–	–	–	20	50	ns
		V_{DD} = 10	–	–	–	–	10	25	
Capacitance: Input, C_{IS}	V_{DD} = +5, $V_{CC} = V_{SS}$ = -5		–	–	–	–	8	–	pF
Output, C_{OS}			–	–	–	–	8	–	
Feedthrough, C_{IOS}			–	–	–	–	0.5	–	
CONTROL (V_C)									
Noise Immunity, V_{NL} Min	$V_{IS} \leq V_{DD}$, I_{IS} = 10μA, $V_{DD} - V_{SS}$ = 10		2	2	2	2	2 min 4.5	–	V
Input Leakage Current, I_{IL} Max.	$V_{IS} \leq V_{DD}$, $V_{DD} - V_{SS}$ = 15, $V_C \leq V_{DD} - V_{SS}$		±1				$\pm 10^{-6}$	±1	μA
Crosstalk Control Input to Signal Output	$V_{DD}-V_{SS}$ = 10, V_C = 10 (sq wave), $t_{rC} = t_{fC}$ = 20 ns	R_L = 10kΩ	–	–	–	–	50	–	mV
Propagation Delay, t_{pdC}		R_L = 300kΩ, $V_{IS} \leq 10$, C_L = 15pF	–	–	–	–	35	–	ns
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1kΩ, C_L=15pF, V_C = 10 (sq. wave), t_r, t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage measurement for automatic testing.

Δ Symmetrical about 0 volts. • For all test conditions.

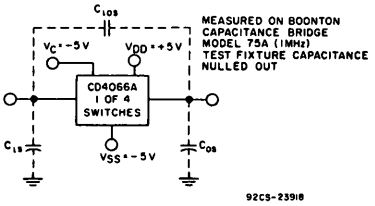


Fig. 6 – Capacitance test circuit.

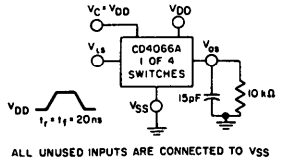


Fig. 8 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

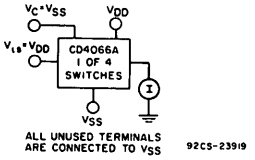


Fig. 7 – OFF switch input or output leakage.

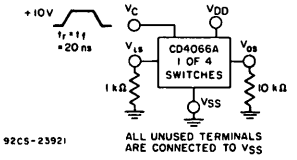


Fig. 9 – Crosstalk-control input to signal output.

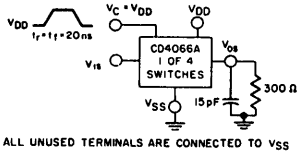


Fig. 11 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

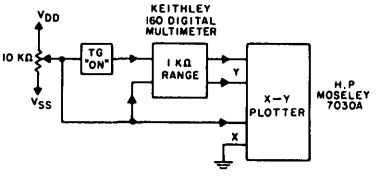


Fig. 3 – Channel ON resistance measurement circuit.

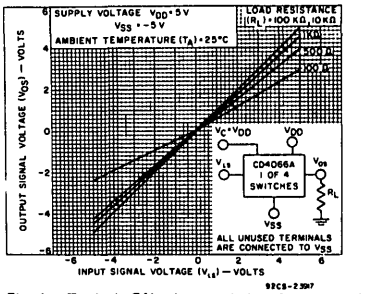


Fig. 4 – Typical ON characteristics for 1 of 4 channels.

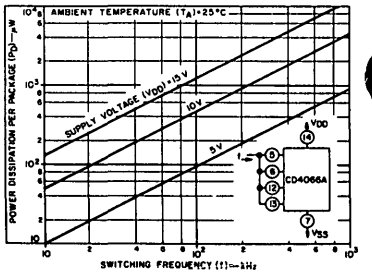


Fig. 5 – Power dissipation per package vs. switching frequency.

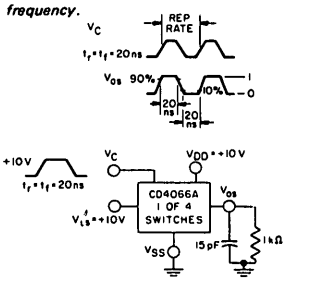


Fig. 10 - Maximum allowable control input repetition rate.

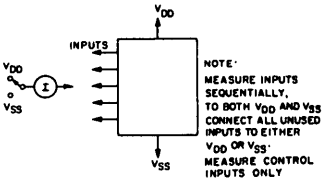


Fig. 12 – Input leakage current test circuit.