CS4201

CrystalClear® Audio Codec '97 with Headphone Amplifier

Features

- Integrated High-Performance Headphone Amplifier
- On-chip PLL for use with External Clock Sources
- Sample Rate Converters
- S/PDIF Digital Audio Output
- AC '97 2.1 Compliant
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Four Analog Line-level Stereo Inputs for LINE IN, CD, VIDEO, and AUX
- Two Analog Line-level Mono Inputs for Modem and Internal PC Beep
- Dual Microphone Inputs
- High Quality Pseudo-Differential CD Input
- Integrated High-Performance Microphone Pre-Amplifier
- Separate Stereo Line-level Output
- Extensive Power Management Support
- Meets or Exceeds the Microsoft® PC 99 Audio Performance Requirements
- CrystalClear® 3D Stereo Enhancement
- I^2S Serial Digital Outputs Enable Cost Effective 6-channel Audio Applications

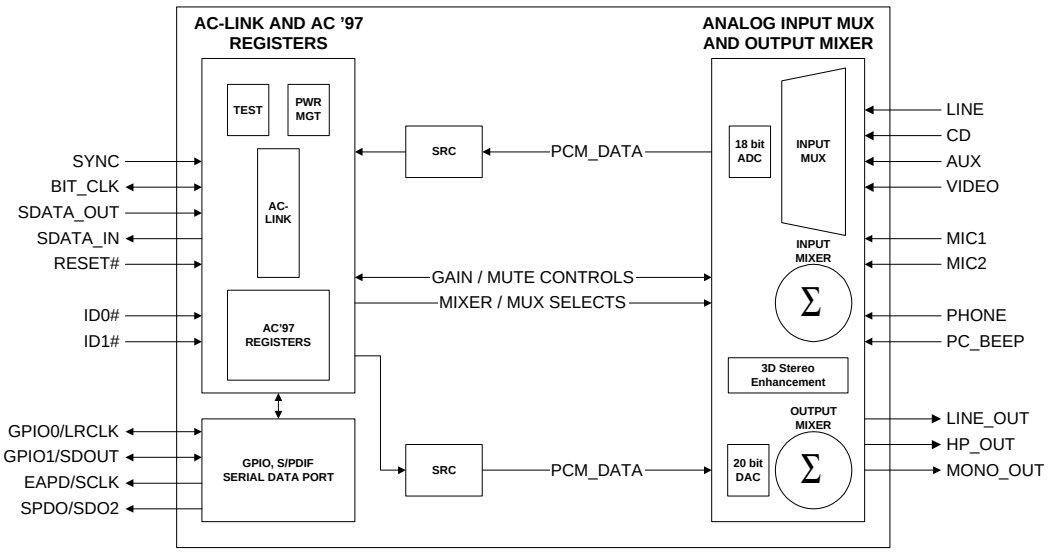
Description

The CS4201 is an AC '97 2.1 compatible stereo audio codec designed for PC multimedia systems. Using the industry leading CrystalClear® delta-sigma and mixed signal technology, the CS4201 enables the design of PC 99-compliant desktop, portable, and entertainment PCs, where high-quality audio is required.

The CS4201, when coupled with a PCI audio accelerator or core logic supporting the AC '97 interface, implements a cost effective, superior quality, audio solution. The CS4201 surpasses PC 99 and AC '97 2.1 audio quality standards.

ORDERING INFO

CS4201-KQ	48-pin TQFP	9x9x1.4 mm
CS4201-JQ	48-pin TQFP	9x9x1.4 mm



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC®
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

TABLE OF CONTENTS

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V ±5%, DVdd = 3.3 V ±5%; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz; Z_{AL}=100 kΩ/ 1000 pF load for Mono and Line Outputs; Z_{AL}=32 Ω/ 200 pF load for Headphone Outputs; C_{DL} = 18 pF load (Note 1); Measurement bandwidth is 20 Hz - 20 kHz, 18-bit linear coding for ADC functions, 20-bit linear coding for DAC functions; Mixer registers set for unity gain.

Parameter (Note 2)	Symbol	Path (Note 3)	CS4201-KQ			CS4201-JQ			Unit
			Min	Typ	Max	Min	Typ	Max	
Full Scale Input Voltage									
Line Inputs		A-D	0.91	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs (20 dB = 0)		A-D	0.91	1.00	-	0.91	1.00	-	V_{RMS}
Mic Inputs (20 dB = 1)		A-D	0.091	0.10	-	0.091	0.10	-	V_{RMS}
Full Scale Output Voltage									
Line and Mono Outputs		D-A	0.91	1.0	1.13	0.91	1.0	1.13	V_{RMS}
Headphone Output		D-A	-	1.4	-	-	1.4	-	V_{RMS}
Frequency Response (Note 4)	FR								
Analog Ac = ± 0.5 dB		A-A	20	-	20,000	20	-	20,000	Hz
DAC Ac = ± 0.5 dB		D-A	20	-	20,000	20	-	20,000	Hz
ADC Ac = ± 0.5 dB		A-D	20	-	20,000	20	-	20,000	Hz
Dynamic Range	DR								
Stereo Analog inputs to LINE_OUT		A-A	90	95	-	-	90	-	dB FS A
Mono Analog inputs to LINE_OUT		A-A	85	90	-	-	85	-	dB FS A
DAC Dynamic Range		D-A	85	90	-	-	87	-	dB FS A
ADC Dynamic Range		A-D	85	90	-	-	85	-	dB FS A
DAC SNR (-20 dB FS input w/ CCIR-RMS filter on output)	SNR	D-A	-	70	-	-	-	-	dB
Total Harmonic Distortion + Noise (-3 dB FS input signal):	THD+N								
Line Output		A-A	-	-90	-80	-	-	-74	dB FS
Headphone Output		A-A	-	-75	-	-	-	-70	dB FS
LINE		D-A	-	-87	-80	-	-	-74	dB FS
ADC (all inputs)		A-D	-	-84	-80	-	-	-74	dB FS
Power Supply Rejection Ratio (1 kHz, 0.5 V_{RMS} w/ 5 V DC offset)(Note 4)			40	60	-	-	40	-	dB
Interchannel Isolation			70	87	-	-	87	-	dB
Spurious Tone (Note 4)			-	-100	-	-	-100	-	dB FS
Input Impedance (Note 4)			10	-	-	10	-	-	kΩ

Notes:
1. Z_{AL} refers to the analog output pin loading and C_{DL} refers to the digital output pin loading.
2. Parameter definitions are given in *Section 13*, *Parameter and Term Definitions*.
3. Path refers to the signal path used to generate this data. These paths are defined in *Section 13*, *Parameter and Term Definitions*.
4. This specification is guaranteed by silicon characterization; it is not production tested.

ANALOG CHARACTERISTICS (Continued)

Parameter (Note 2)	Symbol	Path (Note 3)	CS4201-KQ			CS4201-JQ			Unit
			Min	Typ	Max	Min	Typ	Max	
External Load Impedance									
Line Output			10	-	-	10	-	-	kΩ
Headphone Output			32	-	-	32	-	-	Ω
Output Impedance									
Line Output			-	730	-	-	730	-	Ω
Headphone Output (Note 4)			-	0.8	-	-	0.8	-	Ω
Input Capacitance (Note 4)			-	5	-	-	5	-	pF
Vrefout			2.2	2.4	2.5	2.2	2.4	2.5	V

MIXER CHARACTERISTICS (for **CS4201**-KQ only)

Parameter	Min	Typ	Max	Unit
Mixer Gain Range Span				
PC Beep	-	45.0	-	dB
Line In, Aux, CD, Video, Mic1, Mic2, Phone	-	46.5	-	dB
Mono Out, Line Out, Headphone Out	-	46.5	-	dB
ADC Gain	-	22.5	-	dB
Step Size				
All volume controls except PC Beep	-	1.5	-	dB
PC Beep	-	3.0	-	dB

ABSOLUTE MAXIMUM RATINGS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	-0.3	-	6.0	V
	+5 V Digital	-0.3	-	6.0	V
	Analog	-0.3	-	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)	-	-	1.25	W
Input Current per Pin	(Except Supply Pins)	-10	-	10	mA
Output Current per Pin	(Except Supply Pins)	-15	-	15	mA
Analog Input voltage		-0.3	-	AVdd+ 0.3	V
Digital Input voltage		-0.3	-	DVdd + 0.3	V
Ambient Temperature	(Power Applied)	-55	-	110	°C
Storage Temperature		-65	-	150	°C

RECOMMENDED OPERATING CONDITIONS (AVss1 = AVss2 = DVss1 = DVss2 = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	+3.3 V Digital	DVdd1, DVdd2	3.135	3.3	3.465	V
	+5 V Digital	DVdd1, DVdd2	4.75	5	5.25	V
	Analog	AVdd1, AVdd2	4.75	5	5.25	V
Operating Ambient Temperature			0	-	70	°C

DIGITAL CHARACTERISTICS (AVss = DVss = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DVdd = 3.3V					
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	2.15	-	-	V
High level output voltage	V_{oh}	3.0	3.25	-	V
Low level output voltage	V_{ol}	-	0.03	.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SPDIF_OUT SDATA_IN, EAPD		 - -	 24 4	 - -	 mA mA
DVdd = 5.0 V					
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	3.25	-	-	V
High level output voltage	V_{oh}	4.5	4.95	-	V
Low level output voltage	V_{ol}	-	0.03	.35	V
Input Leakage Current (AC-link inputs)		-10	-	10	µA
Output Leakage Current (Tri-stated AC-link outputs)		-10	-	10	µA
Output buffer drive current BIT_CLK, SPDIF_OUT SDATA_IN, EAPD (Note 4)		 - -	 24 4	 - -	 mA mA

AC '97 SERIAL PORT TIMING

Standard test conditions unless otherwise noted: $T_{ambient}$ = 25° C, AVdd = 5.0 V, DVdd = 3.3 V; C_L = 55 pF load.

Parameter	Symbol	Min	Typ	Max	Unit
RESET Timing					
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK start-up delay (XTL mode)	$T_{rst2clk}$	-	4.0	-	µs
(OSC mode)		-	4.0	-	µs
(PLL mode)		-	2.5	-	ms
1st SYNC active to CODEC READY 'set'	$T_{sync2crd}$	-	62.5	-	µs
Vdd stable to RESET# inactive	$T_{vdd2rst\#}$		TBD		
Clocks					
BIT_CLK frequency	F_{clk}	-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter (depends on XTL_IN source)		-	-	750	ps
BIT_CLK high pulse width	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width	T_{clk_low}	36	40.7	45	ns
SYNC frequency	F_{sync}	-	48	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Data Setup and Hold					
Output propagation delay from rising edge of BIT_CLK	T_{co}	-	6	8	ns
Input setup time from falling edge of BIT_CLK	T_{isetup}	10	-	-	ns
Input hold time from falling edge of BIT_CLK	T_{ihold}	0	-	-	ns
Input signal rise time	T_{irise}	2	-	6	ns
Input signal fall time	T_{ifall}	2	-	6	ns
Output signal rise time (Note 4)	T_{orise}	2	4	6	ns
Output signal fall time (Note 4)	T_{ofall}	2	4	6	ns
Misc. Timing Parameters					
End of Slot 2 to BIT_CLK, SDATA_IN low (PR4)	T_{s2_pdown}	162.8	285	-	ns
SYNC pulse width (PR4) Warm Reset	T_{sync_pr4}	1.0	-	-	µs
SYNC inactive (PR4) to BIT_CLK start-up delay	$T_{sync2clk}$	162.8	285	-	ns
Setup to trailing edge of RESET# (ATE test mode) (Note 4)	$T_{setup2rst}$	15	-	-	ns
Rising edge of RESET# to Hi-Z delay (Note 4)	T_{off}	-	-	25	ns

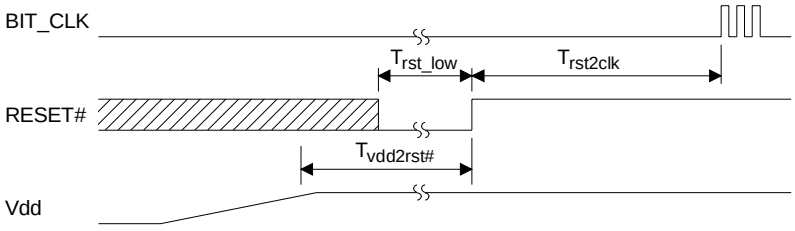


Figure 1. Power Up Timing

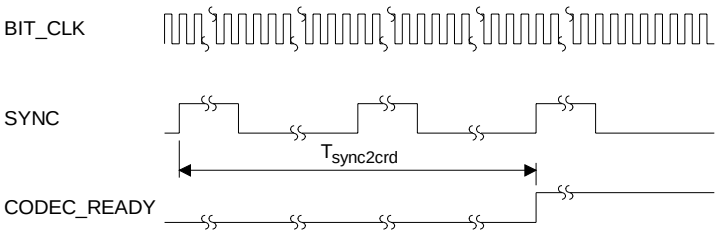


Figure 2. Codec Ready from Startup or Fault Condition

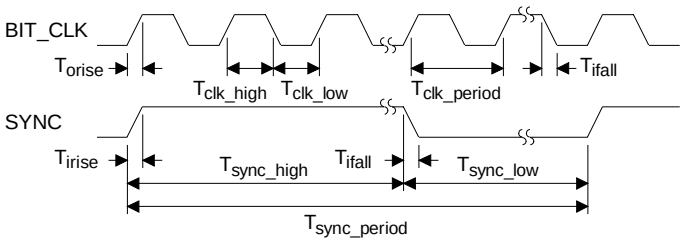


Figure 3. Clocks

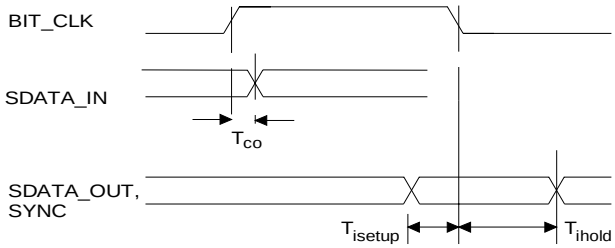


Figure 4. Data Setup and Hold

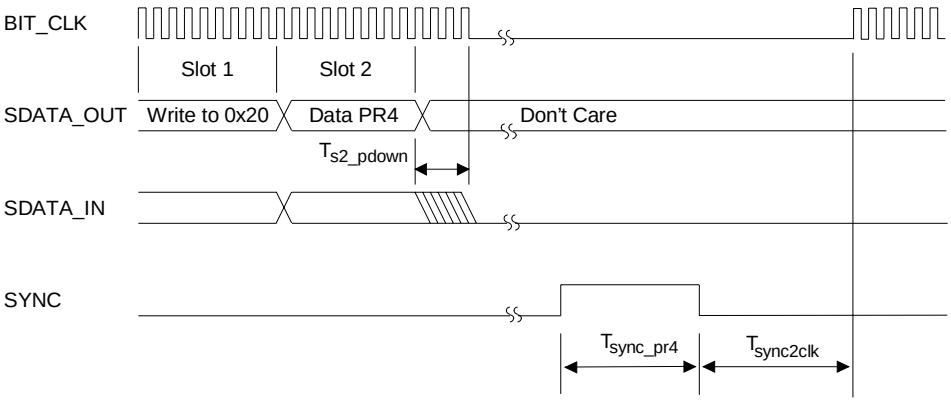


Figure 5. PR4 Powerdown and Warm Reset

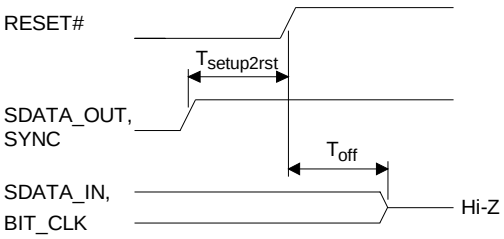


Figure 6. Test Mode

2. GENERAL DESCRIPTION

The CS4201 is a mixed-signal serial audio codec with integrated headphone power amplifier compliant to the Intel® document *Audio Codec '97 Specification*, revision 2.1 [6] (referred to as AC '97). It is designed to be paired with a digital controller interface, typically located on the PCI bus or integrated within the system chip set. The controller is responsible for all communications between the CS4201 and the remainder of the system. The CS4201 contains two distinct functional sections: digital and analog. The digital section includes the AC-link interface, S/PDIF interface, serial data port, power management support, GPIO, and Sample Rate Converters (SRCs). The analog section includes the analog input multiplexer (mux), stereo output mixer, mono output mixer, headphone amplifier, stereo Analog-to-Digital Converters (ADCs), stereo Digital-to-Analog Converters (DACs), and their associated volume controls.

2.1 AC-Link

All communication with the CS4201 is established with a 5-wire digital interface to the controller, as shown in Figure 7. This interface is called the AC-link. All clocking for the serial communication is synchronous to the BIT_CLK signal. BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs. Both input and output AC-link audio frames are organized as a sequence of 256 serial bits forming 13 groups referred to as 'slots'. During each audio frame, data is passed bi-directionally between the CS4201 and the controller. The input frame is driven from the CS4201 on the SDATA_IN line. The output frame is driven from the controller on the SDATA_OUT line. The controller is also responsible for issuing reset commands via the RESET# signal. After being reset, the CS4201 is responsible for notifying the controller that it is ready for operation after synchronizing its internal functions. The CS4201 AC-link signals must use the same digital supply voltage as the controller chip, either +5 V or +3.3 V. See Section 3, *AC-Link Frame Definition*, for detailed AC-Link information.

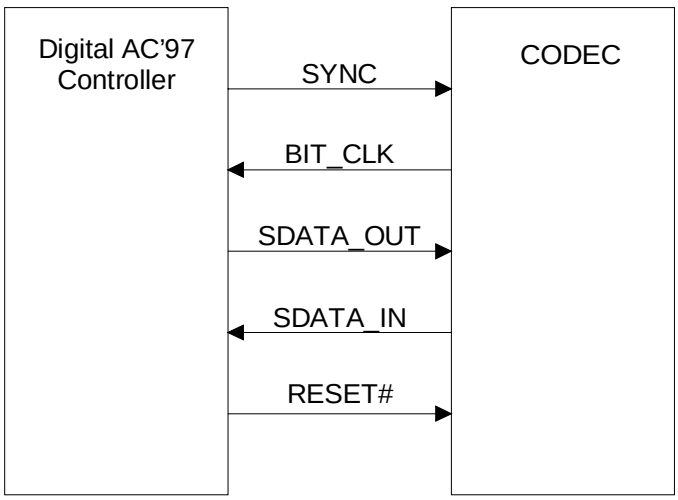


Figure 7. AC-link Connections

2.2 Control registers

The CS4201 contains a set of AC ’97 compliant control registers, as well as a set of Cirrus defined control registers. These registers control the basic functions and features of the CS4201. Read accesses of the control registers by the AC ’97 controller are accomplished with the requested register index in Slot 1 of a SDATA_OUT frame. The following SDATA_IN frame will contain the read data in its Slot 2. Write operations are similar, with the register index in Slot 1 and the write data in Slot 2 of a SDATA_OUT frame. The function of each input and output frame is detailed in Section 3, *AC-Link Frame Definition*. Individual register descriptions are found in Section 4, *Register Interface*.

2.3 Sample Rate Converters

The sample rate converters (SRC) provide high accuracy digital filters supporting sample frequencies other than 48 kHz to be captured from the CS4201 or played from the controller. AC ’97 requires support for 2 audio rates (44.1 and 48 kHz). In addition, the Intel® I/O Controller Hub (ICHx) specification [8] requires support for 5 more audio rates (8, 11.025, 16, 22.05, and 32 kHz). The CS4201 supports all these rates, as shown in Table 7.

2.4 Output Mixers

The CS4201 has two output mixers, illustrated in Figure 8. The stereo output mixer sums together the analog inputs to the CS4201, including the PC_BEEP and PHONE signals, according to the settings in the volume control registers. The stereo output mix is then sent to the LINE_OUT and HP_OUT pins of the CS4201. The mono output mixer generates a monophonic sum of the left and right channels from the stereo input mixer. The mono output mix is then sent to the MONO_OUT pin on the CS4201.

2.5 Input Mux

The input multiplexer controls which analog input is sent to the ADCs. The output of the input mux is converted to stereo 18-bit digital PCM data and sent to the controller chip via the AC-link SDATA_IN signal.

2.6 Volume Control

The CS4201 volume registers control analog input levels to the input mixer and analog output volumes, including the master volume level, and the headphone volume level. The PC_BEEP volume control uses 3 dB steps with a range from 0 dB to -45 dB of attenuation. All other analog volume controls use 1.5 dB steps. The analog inputs have a mixing range of +12 dB of signal gain to -34.5 dB of signal attenuation. The analog output volume controls have from 0 dB to -46.5 dB of attenuation for LINE_OUT, HP_OUT and MONO_OUT.

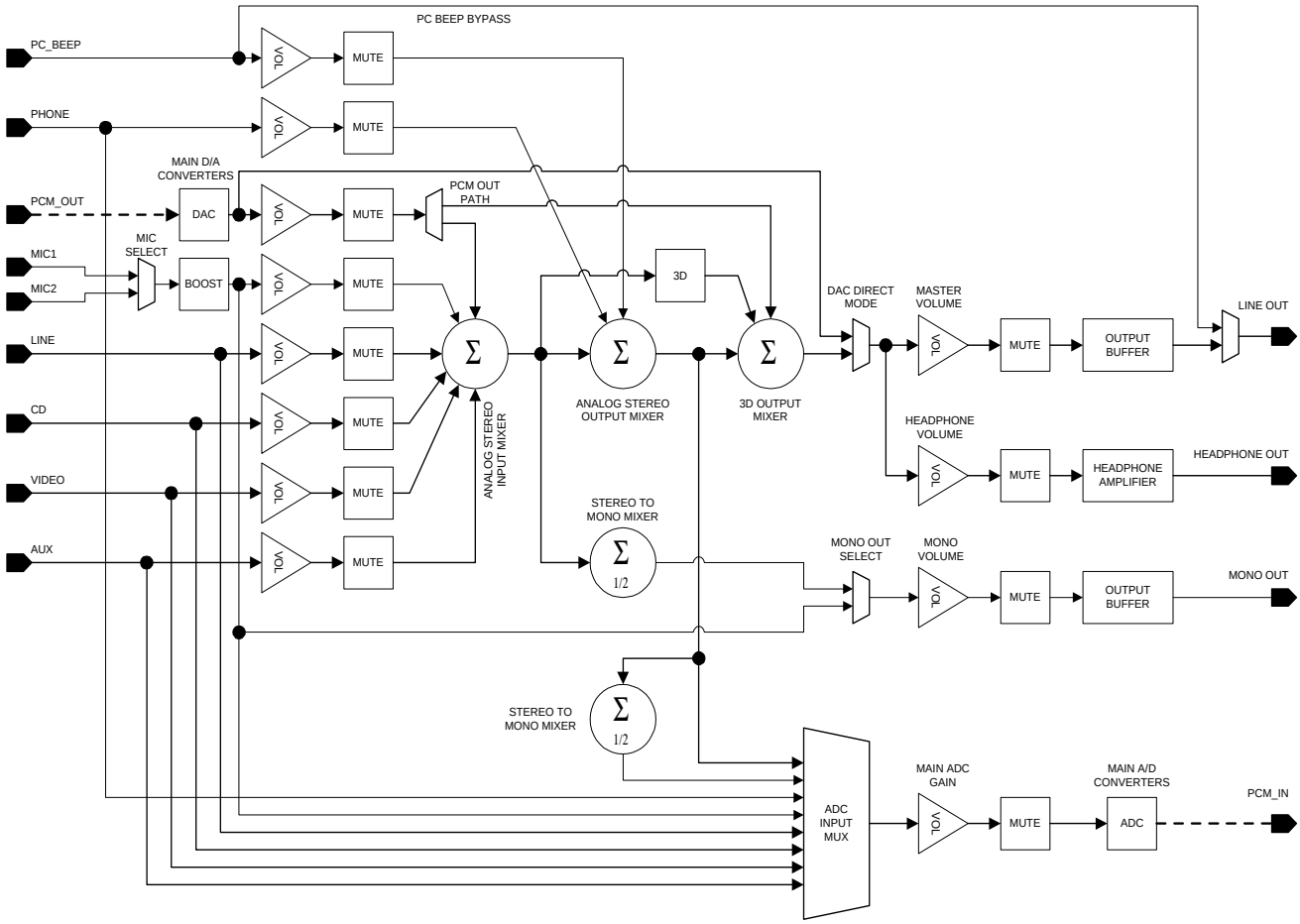


Figure 8. Mixer Diagram

3. AC-LINK FRAME DEFINITION

The AC-link is a bi-directional serial port with data organized into frames consisting of one 16-bit and twelve 20-bit time-division multiplexed slots. The first slot, called the tag slot, contains bits indicating if the CS4201 is ready to receive data (input frame) and which, if any, other slots contain valid data. Slots 1 through 12 contain audio or control/status data. Both the serial data output and input frames are defined from the controller perspective, not from the CS4201 perspective.

The controller synchronizes the beginning of a frame with the SYNC signal. Figure 9 shows the position of each bit location within the frame. The first bit position in a new serial data frame is F0 and the last bit position in the serial data frame is F255. When SYNC goes active (high) and is sampled active by the CS4201 (on the falling edge of BIT_CLK), both devices are synchronized to a new serial data frame. The data on the SDATA_OUT pin at this clock edge is the final bit of the previous frame's serial data. On the next rising edge of BIT_CLK, the first bit of Slot 0 is driven by the controller on the SDATA_OUT pin. On the next falling edge of BIT_CLK, the CS4201 latches this data in, as the first bit of the frame.

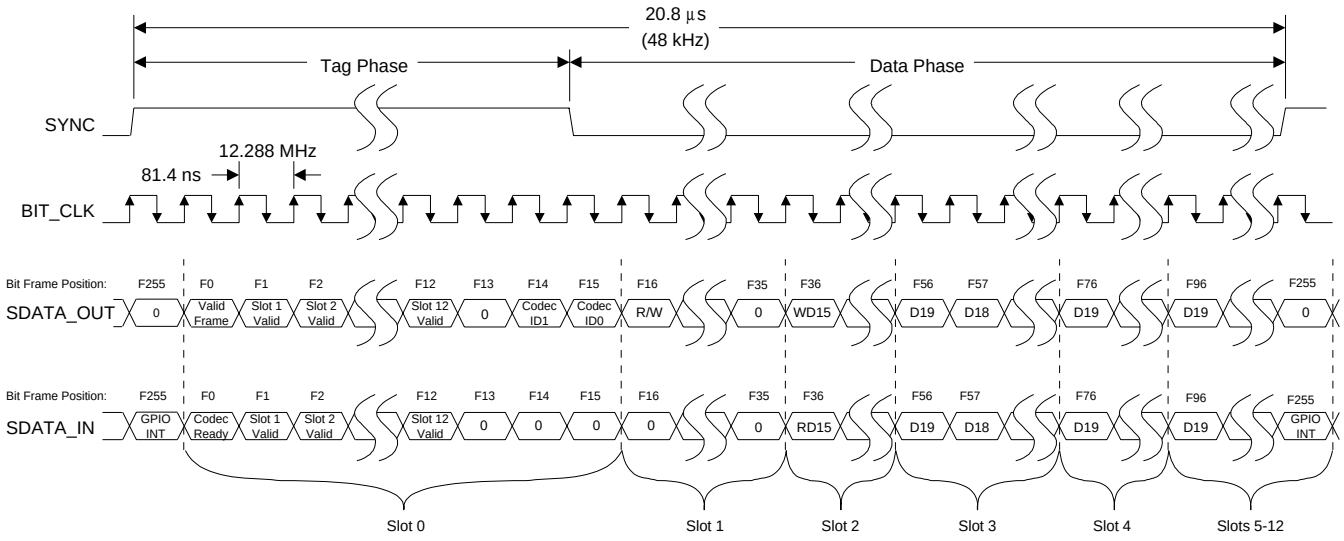


Figure 9. AC-link Input and Output Framing

3.1 AC-Link Serial Data Output Frame

In the serial data output frame, data is passed on the SDATA_OUT pin to the CS4201 from the controller. Figure 9 illustrates the serial port timing.

The PCM playback data being passed to the CS4201 is shifted out MSB first in the most significant bits of each slot. Any PCM data from the AC ’97 controller that is not 20 bits wide should be left justified in its corresponding slot and dithered or zero-padded in the unused bit positions.

Bits that are reserved should always be ‘cleared’ by the AC ’97 controller.

3.1.1 Serial Data Output Slot Tags (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	Slot 9 Valid	Slot 10 Valid	Slot 11 Valid	Slot 12 Valid	Reserved	Codec ID1	Codec ID0

Valid Frame — Determines if any of the following slots contain either valid playback data for the CS4201 DACs or data for read/write operations. When ‘set’, at least one of the other AC-link slots contain valid data. If this bit is ‘clear’, the remainder of the frame is ignored.

Slot [1:2] Valid — Indicates the validity of data in their corresponding serial data output slots. If a bit is ‘set’, the corresponding output slot contains valid data. If a bit is ‘cleared’, the corresponding slot will be ignored.

Slot [3:11] Valid — Indicates Slot [3:11] contains valid playback data for the CS4201. If a Slot Valid bit is ‘set’, the named slot contains valid audio data. If the bit is ‘clear’, the slot will be ignored. The CS4201 supports alternate slot mapping as defined in the AC ’97 2.1 specification. For more information, see Section 4.24, *AC Mode Control Register (Index 5Eh)*.

Slot 12 Valid — Indicates Slot 12 contains valid GPIO control data.

Codec ID[1:0] — Codec ID of the audio codec being accessed during this current AC-link frame. Codec ID[1:0] = 00 indicates the primary codec is being accessed. Codec ID[1:0] = 01, 10, or 11 indicates one of three possible secondary codecs is being accessed. A non-zero value of one or more of the Codec ID bits indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

3.1.2 Command Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/$\overline{W}$	RI6	RI5	RI4	RI3	RI2	RI1	RI0	Reserved											

R/$\overline{W}$ — Read/$\overline{\text{Write}}$. When this bit is ‘set’, a read of the AC ’97 register specified by the register index bits will occur in the primary AC ’97 2.1 audio codec. When the bit is ‘cleared’, a write will occur. For any read or write access to occur, the Frame Valid bit (F0) must be ‘set’ and the Codec ID in bits F[14:15] must match the Codec ID of the AC ’97 2.1 audio codec being accessed. Additionally, for a primary codec, the Slot 1 Valid bit (F1) must be ‘set’ for a read access and both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be ‘set’ for a write access. For a secondary codec, both the Slot 1 Valid bit (F1) and the Slot 2 Valid bit (F2) must be ‘cleared’ for read and write accesses.

RI[6:0] — Register index/address. Bits RI[6:0] contain the 7-bit register index to the AC ’97 registers in the CS4201. All registers are defined at word addressable boundaries. RI0 must be ‘cleared’ to access CS4201 registers.

3.1.3 Command Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	Reserved			

WD[15:0] Bits WD[15:0] contain the 16-bit value to be written to the register. If an access is a read, this slot is ignored.

NOTE: For any write to an AC '97 register, the write is defined to be an 'atomic' access. This means that when the slot valid bit for Slot 1 is 'set', the slot valid bit for Slot 2 should always be 'set' during the same audio frame. No write access may be split across 2 frames.

3.1.4 PCM Playback Data (Slots 3-11)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD[19:0] 20-bit PCM playback (2's complement) data for the left and right DACs and/or the S/PDIF transmitter. Table 9 lists a cross reference for each function and its respective slot. The mapping of a given slot to a DAC is determined by the state of the ID[1:0] bits found in the *Extended Audio ID Register (Index 28h)* and by the SM[1:0] and AMAP bits found in the *AC Mode Control Register (Index 5Eh)*.

3.1.5 GPIO Data (Slot12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Implemented														GPIO1	GPIO0	Reserved			

GPIO[1:0] GPIO pin control bits. These bits control the GPIO pins on the CS4201 which are configured as outputs. Write accesses using GPIO pin control bits configured as outputs will be reflected on the GPIO pin output on the next AC-link frame. Write accesses using GPIO pin control bits configured as inputs will have no effect and are ignored. If the GPOC bit in the *Misc. Crystal Control Register (Index 60h)* is 'set', the bits in output Slot 12 are ignored and GPIO pins configured as outputs are controlled through the *GPIO Pin Status Register (Index 54h)*.

3.2 AC-Link Serial Data Input Frame

In the serial data input frame, data is passed on the SDATA_IN pin from the CS4201 to the AC '97 controller. The data format for the input frame is very similar to the output frame. Figure 9 illustrates the serial port timing.

The PCM capture data from the CS4201 is shifted out MSB first in the most significant 18 bits of each slot. The least significant 2 bits in each slot will be 'cleared'. If the host requests PCM data from the AC '97 Controller that is less than 18 bits wide, the controller should dither and round or just round (but not truncate) to the desired bit depth.

Bits that are reserved or not implemented in the CS4201 will always be returned 'cleared'.

3.2.1 Serial Data Input Slot Tag Bits (Slot 0)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Codec Ready	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	Slot 5 Valid	Slot 6 Valid	Slot 7 Valid	Slot 8 Valid	0	0	0	Slot 12 Valid	Reserved		

Codec Ready — Indicates the readiness of the CS4201 AC-link and Control and Status registers. Immediately after a Cold Reset this bit will be 'clear'. Once the CS4201 clocks and voltages are stable, this bit will be 'set'. Until the Codec Ready bit is 'set', no AC-link transactions should be attempted by the controller. The Codec Ready bit does not indicate readiness of the DACs, ADCs, Vref, or any other analog function. Those must be checked in the *Powerdown Control/Status Register (Index 26h)* by the controller before any access is made to the mixer registers. Any accesses to the CS4201 while Codec Ready is 'cleared' are ignored.

Slot 1 Valid — Indicates Slot 1 contains a valid read back address.

Slot 2 Valid — Indicates Slot 2 contains valid register read data.

Slot [3:8] Valid — Indicates Slot [3:8] contains valid capture data from the CS4201 ADC. If a bit is 'set' the corresponding input slot contains valid data.

Slot 12 Valid — Indicated Slot 12 contains valid GPIO status data.

3.2.2 Status Address Port (Slot 1)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	RI6	RI5	RI4	RI3	RI2	RI1	RI0	SR3	SR4	SR5	SR6	SR7	SR8	SR9	0	SR11	0	Reserved	

RI[6:0] — Register index. The Read-Back Address Port echoes the AC '97 register address when a register read has been requested in the previous frame. The CS4201 will only echo the register index for a read access. Write accesses will not return valid data in Slot 1.

SR[3:9,11] — Slot Request for Slots 3 - 9 and 11. If SRx is 'set', this indicates the CS4201 SRC does not need a new sample on the next AC-link frame for that particular slot. If SRx is 'cleared', the SRC indicates a new sample is needed on the following frame. If the VRA bit in the *Extended Audio Status/Control Register (Index 2Ah)* is 'cleared', the SR bits are always 0. When VRA is 'set', the SRCs are enabled and the SR bits are used to request data.

3.2.3 Status Data Port (Slot 2)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Reserved			

RD[15:0] 16-bit register value. The Read-Back Data Port contains the register data requested by the controller from the previous read request. All read requests will return the read address in the Read-Back Address Port (Slot 1) and the register data in the Read-Back Data Port (Slot 2) on the following serial data frame.

3.2.4 PCM Capture Data (Slot 3-8)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	0	0

CD[17:0] 18-bit PCM (2's complement) data. The mapping of a given slot to an ADC is determined by the state of the ID[1:0] bits found in the *Extended Audio ID Register (Index 28h)* and the SM[1:0] and AMAP bits found in the *AC Mode Control Register (Index 5Eh)*. The definition of each slot can be found in Table 9.

The capture data in Slot [3:8] will only be valid when the respective slot valid bit is 'set' in Slot 0.

3.2.5 GPIO Pin Status (Slot 12)

Bit 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPIO1	GPIO0	Reserved			GPIO_INT

GPIO[1:0] Status of the GPIO[1:0] pins. If the pin is configured as an input, the GPIO pin status will be reflected on Slot 12 of the SDATA_IN stream. If the pin is configured as an output, the output pin status, which is controlled by the GPIO pin control bit in the SDATA_OUT stream, will be reflected back on the GPIO pin status bit of the SDATA_IN stream in the next frame.

GPIO_INT This bit indicates that a GPIO interrupt event has occurred. The occurrence of this interrupt is determined by the GPIO interrupt requirements as outlined in the *GPIO Pin Wakeup Mask Register (Index 52h)* description. The GPIO_INT bit is 'cleared' by writing a '0' to the GPIO Pin Status bit corresponding to the GPIO pin which generated the interrupt.

3.3 AC '97 Reset Modes

The CS4201 supports four reset methods, as defined in the AC '97 Specification: *Cold AC '97 Reset, Warm AC '97 Reset, Register AC '97 Reset, and New Warm AC '97 Reset*. A Cold Reset results in all AC '97 logic (registers included) initialized to its default state. A Warm Reset leaves the contents of the AC '97 register set unaltered. A Register Reset initializes only the AC '97 registers to their default states. AC '97 2.1 additionally defines a so-called New Warm Reset, a Warm Reset variation. The timing of power-up/reset events is discussed in detail in Section 5, *Power Management*.

3.3.1 Cold AC '97 Reset

A Cold Reset is achieved by asserting RESET# for a minimum of 1 µs after the power supply rails have stabilized. This is done in accordance with the minimum timing specifications in the *AC '97 Serial Port Timing* section. Once de-asserted, all of the CS4201 registers will be reset to their default power-on states and the BIT_CLK and SDATA_IN signals will be reactivated.

3.3.2 Warm AC '97 Reset

A Warm Reset allows the AC-link to be reactivated without losing information in the CS4201 registers. Warm Reset is the required resume sequence to recover from a $D3_{hot}$ state where the AC-link had been halted yet full power had been maintained. A primary codec Warm Reset is initiated when the SYNC signal is driven high for at least 1 µs and then driven low in the absence of the BIT_CLK clock signal. The BIT_CLK clock will not restart until at least 2 normal BIT_CLK clock periods (162.8 ns) after the SYNC signal is de-asserted. A secondary codec Warm Reset is recognized when the primary codec on the AC-link resumes BIT_CLK generation. The CS4201 will wait for BIT_CLK to be stable and then restore SDATA_IN activity and S/PDIF and/or serial data port transmission on the following frame.

3.3.3 Register AC '97 Reset

The third reset mode provides a register reset to the CS4201. This is available only when the CS4201 AC-link is active and the Codec Ready bit is 'set'. The audio (including extended audio) registers (*Index 00h - 38h*) and the vendor specific registers (*Index 5Ah - 7Ah*) are reset to their default states by a write of any value to the *Reset Register (Index 00h)*. The modem (including GPIO) registers (*Index 3Ch - 56h*) are reset to their default states by a write of any value to the *Extended Modem ID Register (Index 3Ch)*.

3.3.4 New Warm AC '97 Reset

The New Warm Reset also allows the AC-link to be reactivated without losing information in the registers. New Warm Reset is the required resume sequence to recover from a D3cold state where AC-link power has been removed. New Warm Reset is recognized by the low-high transition of RESET# after the AC-link has been programmed into PR4 powerdown. The New Warm Reset functionality can be disabled by setting the CRST bit in the *Misc. Crystal Control Register (Index 60h)*.

3.4 AC-Link Protocol Violation - Loss of SYNC

The CS4201 is designed to handle SYNC protocol violations. The following are situations where the SYNC protocol has been violated:

- The SYNC signal is not sampled high for exactly 16 BIT_CLK clock cycles at the start of an audio frame.
- The SYNC signal is not sampled high on the 256th BIT_CLK clock period after the previous SYNC assertion.
- The SYNC signal goes active high before the 256th BIT_CLK clock period after the previous SYNC assertion.

Upon loss of synchronization with the controller, the CS4201 will mute all analog outputs and 'clear' the Codec Ready bit in the serial data input frame until two valid frames are detected. During this detection period, the CS4201 will ignore all register reads and writes and will discontinue the transmission of PCM capture data.

4. REGISTER INTERFACE

Reg	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	0	ID4	0	0	0	0	1990h
02h	Master Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone Volume	Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Volume	Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0	0000h
0Ch	Phone Volume	Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP	0	3D	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
22h	3D Control	0	0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	S0	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC	000Fh
28h	Ext'd Audio ID	ID1	ID0	0	0	0	0	AMAP	0	0	0	0	0	0	0	0	VRA	x201h
2Ah	Ext'd Audio Stat/Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VRA	0000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ch	Ext'd Modem ID	ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x000h
3Eh	Ext'd Modem Stat/Ctrl	0	0	0	0	0	0	0	PRA	0	0	0	0	0	0	0	GPIO	0100h
4Ch	GPIO Pin Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GC1	GC0	0003h
4Eh	GPIO Pin Polarity/Type	1	1	1	1	1	1	1	1	1	1	1	1	1	1	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GS1	GS0	0000h
52h	GPIO Pin Wakeup Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GW1	GW0	0000h
54h	GPIO Pin Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GI1	GI0	0000h
Cirrus Defined Registers:																		
5Eh	AC Mode Control	0	0	0	0	ASPM	0	0	DDM	AMAP	SPAS	SM1	SM0	0	0	0	0	0080h
60h	Misc. Crystal Control	0	0	0	DPC	0	0	Reserved		10dB	CRST	Reserved		GPOC	Reserved		0	0002h
68h	S/PDIF Control	SPEN	Val	0	Fs	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Emph	Copy	/Audio	Pro	0000h
6Ah	Serial Port Control	SDEN	0	0	0	0	0	0	0	0	0	0	0	S2EN	SDSC	SDF1	SDF0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4352h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	0	DID2	DID1	DID0	1	REV2	REV1	REV0	5949h

Table 1. Register Overview

4.1 Reset Register (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	SE4	SE3	SE2	SE1	SE0	0	ID8	ID7	0	0	ID4	0	0	0	0

SE[4:0] 3D Stereo Enhancement Technique.
00110 - Crystal 3D Stereo Enhancement.

ID8 ID8 = 1, 18-bit ADC resolution.

ID7 ID7 = 1, 20-bit DAC resolution.

ID4 Headphone out support. The state of this bit depends on the state of the HPCFG pin.

Default 1990h, read-only data

Any write to this register causes a Register Reset to the default state of the audio (*Index 00h - 38h*) and vendor specific (*Index 5Ah - 7Ah*) registers. A read from this register returns configuration information about the CS4201.

4.2 Master/Headphone Volume Register (Index 02h-04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	ML5	ML4	ML3	ML2	ML1	ML0	0	0	MR5	MR4	MR3	MR2	MR1	MR0

Mute Master mute for the LINE_OUT_L/R or HP_OUT_L/R output signals.

ML[4:0] Volume control for the left channel output signal. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB. See Table 2 for further gain levels.

ML5 Setting ML5 sets the left channel attenuation to -46.5 dB by forcing ML[4:0] to a '1' state. ML[5:0] will read back 01111 when ML5 has been 'set'. Table 2 summarizes this behavior.

MR[4:0] Volume control for the right channel output signal. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB. See Table 2 for further gain levels.

MR5 Setting MR5 sets the right channel attenuation to -46.5 dB by forcing MR[4:0] to a '1' state. MR[5:0] will read back 011111 when MR5 has been 'set'. Table 2 summarizes this behavior.

Default 8000h, corresponding to 0 dB attenuation and mute on.

If the HPCFG pin is left floating, register 02h controls the Master Volume and register 04h controls the Headphone Volume. If the HPCFG pin is tied 'low', register 02h controls the Headphone Volume and register 04h is a read-only register and always returns 0000h when 'read'.

Mx5..Mx0 Write	Mx5..Mx0 Read	Gain Level
000000	000000	0 dB
000001	000001	-1.5 dB
…	…	...
011111	011111	-46.5 dB
100000	011111	-46.5 dB
...	...	...
111111	011111	-46.5 dB

Table 2. Analog Mixer Output Attenuation

4.3 Mono Volume Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	MM5	MM4	MM3	MM2	MM1	MM0

Mute — When 'set', mutes the MONO_OUT signal.

MM[4:0] — Mono Attenuation. Least significant bit represents -1.5 dB with 00000 = 0 dB. The total range is 0 dB to -46.5 dB. See Table 2 for further gain levels.

MM5 — Setting MM5 sets the mono attenuation to -46.5 dB by forcing MM[4:0] to a '1' state. MM[5:0] will read back 011111 when MM5 has been 'set'. Table 2 summarizes this behavior.

Default — 8000h, corresponding to 0 dB attenuation and Mute 'set'.

4.4 PC_BEEP Volume Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	PV3	PV2	PV1	PV0	0

Mute — When 'set', mutes the PC_BEEP signal.

PV[3:0] — Volume control for the PC_BEEP pin. Least significant bit represents -3 dB with 0000 = 0 dB. The total range is 0 dB to -45 dB.

Default — 0000h, unmuted, with 0 dB attenuation after the CS4201 is removed from the reset state.

4.5 Phone Volume Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	0	0	GN4	GN3	GN2	GN1	GN0

Mute — When 'set', mutes the PHONE signal.

GN[4:0] — Phone Volume Control. Least significant bit represents -1.5 dB with 01000 = 0 dB. The total range is +12 dB to -34.5 dB. See Table 4 for further gain levels.

Default — 8008h, 0 dB attenuation and Mute 'set'.

4.6 Microphone Volume Register (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	0	0	0	0	0	20dB	0	GN4	GN3	GN2	GN1	GN0

Mute — When ‘set’, mutes MIC1/MIC2 signal.

GN[4:0] — MIC1/MIC2 Volume Control. Least significant bit represents -1.5 dB with 01000 = 0 dB. The total range is +12 dB to -34.5 dB. See Table 3 for further gain levels.

20dB — Enables 20 dB microphone boost block. In combination with the 10dB boost bit in the *Misc. Crystal Control Register (Index 60h)* this bit allows for variable boost from 0 dB to +30 dB. Table 3 summarizes this behavior.

Default — 8008h, 0 dB attenuation and Mute ‘set’.

This register controls the gain level of the Microphone input source to the Input Mixer. It also controls the +20 dB gain block which connects to the input volume control and to the Input Record Mux. The selection of MIC1 or MIC2 input pins is controlled by the MS bit in the *General Purpose Register (Index 20h)*.

GN4 - GN0	Gain Level			
	10dB = 0 20dB = 0	**10dB = 1 20dB = 0**	**10dB = 0 20dB = 1**	**10dB = 1 20dB = 1**
00000	+12.0 dB	+22.0 dB	+32.0 dB	+42.0 dB
00001	+10.5 dB	+20.5 dB	+30.5 dB	+40.5 dB
…	…	...	...	...
00111	+1.5 dB	+11.5 dB	+21.5 dB	+31.5 dB
01000	0.0 dB	+10.0 dB	+20.0 dB	+30.0 dB
01001	-1.5 dB	+8.5 dB	+18.5 dB	+28.5 dB
…	…	...	...	...
11111	-34.5 dB	-24.5 dB	-14.5 dB	-4.5 dB

Table 3. Microphone Input Gain Values

4.7 Stereo Analog Mixer Input Gain Registers (Index's 10h - 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	GL4	GL3	GL2	GL1	GL0	0	0	0	GR4	GR3	GR2	GR1	GR0

Mute — When 'set', mutes the respective input signal. Setting this bit mutes both right and left inputs.

GL[4:0] — Left Volume Control. Least significant bit represents -1.5 dB with 01000 = 0 dB. The total range is +12 dB to -34.5 dB. See Table 4 for further gain levels.

GR[4:0] — Right Volume Control. Least significant bit represents -1.5 dB with 01000 = 0 dB. The total range is +12 dB to -34.5 dB. See Table 4 for further gain levels.

Default — 8808h, 0 dB gain with Mute enabled.

These registers control the gain levels of the analog input sources to the Input Mixer. The analog inputs associated with *Stereo Analog Mixer Input Gain Registers (Index's 10h - 18h)* are found in Table 5.

GN4 - GN0	Gain Level
00000	+12.0 dB
00001	+10.5 dB
…	…
00111	+1.5 dB
01000	0.0 dB
01001	-1.5 dB
…	…
11111	-34.5 dB

Table 4. Analog Mixer Input Gain Values

Register Index	Function
10h	Line In Volume
12h	CD Volume
14h	Video Volume
16h	Aux Volume
18h	PCM Out Volume

Table 5. Stereo Volume Register Index

4.8 Input Mux Select Register (Index 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SL2	SL1	SL0	0	0	0	0	0	SR2	SR1	SR0

SL[2:0] Left Channel ADC input source select.

SR[2:0] Right Channel ADC input source select.

Default 0000h, Mic inputs selected for both channels.

When capturing PCM data, this register controls the input MUX for the ADCs. Table 6 lists the possible values for each input.

Sx2 - Sx0	Record Source
000	Mic
001	CD Input
010	Video Input
011	Aux Input
100	Line Input
101	Stereo Mix
110	Mono Mix
111	Phone Input

Table 6. Input Mux Selection

4.9 Record Gain Register (Index 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	0	0	0	GL3	GL2	GL1	GL0	0	0	0	0	GR3	GR2	GR1	GR0

Mute When ‘set’, mutes the input to the ADCs.

GL[3:0] Left ADC gain. Least significant bit represents +1.5 dB with 0000 = 0 dB.
The total range is 0 dB to +22.5 dB.

GR[3:0] Right ADC gain. Least significant bit represents +1.5 dB with 0000 = 0 dB.
The total range is 0 dB to +22.5 dB.

Default 8000h, 0 dB gain with Mute on.

4.10 General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
POP	0	3D	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0

POP — This bit controls the PCM out path. When 'cleared', the PCM out path is mixed pre 3D. When 'set', the PCM out path is mixed post 3D.

3D — 3D Enable. If 'set', enables the CrystalClear™ 3D stereo enhancement. This function is not available in DAC Direct Mode (DDM).

MIX — Mono Output Path. When 'clear', the Mono Mix out (a mix of the 4 analog stereo sources plus Mic and PCM_OUT) is selected for MONO_OUT. When 'set', the Mic path is sent to Mono Out.

MS — Microphone Select. Determines which of the two Mic inputs are passed to the mixer. When 'set', MIC2 input is selected; when 'clear' MIC1 is selected.

LPBK — Loopback. If 'set', enables ADC/DAC Loopback Mode. This bit routes the ADC output to the DAC input without involving the AC-link.

Default — 0000h.

4.11 3D Control Register (Index 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	S0

S[3:0] — Spatial Enhancement Depth Control. Spatial Enhancement is enabled by the 3D bit in the *General Purpose Register (Index 20h)*.
0000 - Minimum spatial enhancement.
1111 - Maximum spatial enhancement.

Default — 0000h, minimum spatial enhancement added.

4.12 Powerdown Control/Status Register (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC

EAPD — External Amplifier Power Down. The EAPD pin follows this bit. Generally used to power-down external amplifiers. The EAPD bit is mutually exclusive with the SDSC bit in the *Serial Port Control Register (Index 6Ah)*. The SDSC bit must be 'cleared' before the EAPD bit may be 'set'. If the SDSC bit is '1', EAPD is a read-only bit and always returns '0'.

PR6 — When 'set', the headphone amplifier is powered down.

PR5 — When 'set', the internal master clock is disabled (BIT_CLK running). The only way to recover from setting this bit is through a cold AC '97 reset (driving the RESET# signal active).

PR4 — When 'set', the AC-link is powered down (BIT_CLK off). The AC-link can be restarted through a warm AC '97 reset using the SYNC signal, or a cold AC '97 reset using the RESET# signal (the primary codec only).

PR3 — When 'set', the analog mixer and voltage reference are powered down. When clearing this bit, the ANL, ADC, and DAC bits should be checked before writing any mixer registers.

PR2 — When 'set', the analog mixer is powered down (the voltage reference is still active). When clearing this bit, the ANL bit should be checked before writing any mixer registers.

PR1 — When 'set', the DACs are powered down. When clearing this bit, the DAC bit should be checked before sending any data to the DACs.

PR0 — When 'set', the ADCs and the ADC input muxes are powered down. When clearing this bit, no valid data will be sent down the AC-link until the ADC bit goes high.

REF — Voltage Reference Ready Status. When 'set', indicates the voltage reference is at a nominal level.

ANL — Analog Ready Status. When 'set', the analog output mixer, input multiplexer, and volume controls are ready. When 'clear', no volume control registers should be written.

DAC — DAC Ready Status. When 'set', the DACs are ready to receive data across the AC-link. When 'clear', the DACs will not accept any valid data.

ADC — ADC Ready Status. When 'set', the ADCs are ready to send data across the AC-link. When 'clear', no data will be sent to the controller.

Default — 0000h, all blocks are powered on. The lower four bits will eventually change as the CS4201 finishes an initialization and calibration sequence.

The PR[6:0] and the EAPD bits are power-down control for different sections of the CS4201 as well as external amplifiers. The REF, ANL, DAC, and ADC bits are read-only status bits which, when 'set', indicate that a particular section of the CS4201 is ready. After the controller receives the Codec Ready bit in Slot 0, these status bits must be checked before writing to any mixer registers.

4.13 Extended Audio ID Register (Index 28h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID0	0	0	0	0	AMAP	0	0	0	0	0	0	0	0	VRA

ID[1:0] Codec configuration ID. Primary is 00; Secondary is 01,10,or 11. This is a reflection of the ID[1:0]# configuration pins. The state of the ID[1:0] bits is determined at power-up from the Codec ID[1:0]# pins and the current clocking scheme, see Table 15.

AMAP Audio Slot Mapping. The AMAP bit indicates whether the optional AC '97 2.1 compliant AC-link slot to audio DAC mapping is supported. This bit is a shadow of the AMAP bit in the *AC Mode Control Register (Index 5Eh)*. The PCM playback and capture slots are mapped according to Table 9.

VRA Variable Rate PCM Audio. The VRA bit indicates whether variable rate PCM audio is supported. This bit always returns '1', indicating that variable rate PCM audio is available.

Default x201h.

The *Extended Audio ID Register (Index 28h)* is a read only register.

4.14 Extended Audio Status/Control Register (Index 2Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VRA

VRA Enable Variable Rate Audio. When 'set', this bit allows access to the *PCM Front DAC Rate Register (Index 2Ch)* and the *PCM L/R ADC Rate Register (Index 32h)*. This bit must be 'set' in order to use variable PCM playback or capture rates. The VRA bit also serves as a power-down for the DAC and ADC SRC blocks. Clearing VRA will reset the *PCM Front DAC Rate Register (Index 2Ch)* and the *PCM L/R ADC Rate Register (Index 32h)* to their default values. The SRC data path is flushed and the Slot Request bits for the currently active DAC slots will be fixed at '0'.

Default 0000h.

4.15 PCM DAC Rate Register (Index 2Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR[15:0] DAC Sample Rate Select. Can only be written when the VRA bit of the *Extended Audio Status/Control Register (Index 2Ah)* is 'set'. If the VRA bit is 'clear', all writes are ignored and the register reads back BB80h; corresponding to a 48 kHz sample rate. If the VRA bit is 'set', seven standard sample rates are available. If a sample rate written to the register is not directly supported, the attempted value to be written will be decoded according to the ranges indicated in Table 7. All register read transactions will reflect the actual value stored (column 2 in Table 7) and not the one attempted to be written.

Default BB80h, indicating 48 kHz sample rate.

Sample Rate (Hz)	SR[15:0]	SR[15:12] decode range
8,000	1F40	0 or 1
11,025	2B11	2
16,000	3E80	3
22,050	5622	4 or 5
32,000	7D00	6 or 7
44,100	AC44	8,9,Ah
48,000	BB80	Bh,Ch,Dh,Eh,Fh

Table 7. Standard Sample Rates

4.16 PCM ADC Rate Register (Index 32h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR[15:0] ADC Sample Rate Select. Can only be written when the VRA bit of the *Extended Audio Status/Control Register (Index 2Ah)* is 'set'. If the VRA bit is 'clear', all writes are ignored and the register reads back BB80h; corresponding to a 48 kHz sample rate. If the VRA bit is 'set', seven standard sample rates are available. If a sample rate written to the register is not directly supported, the attempted value to be written will be decoded according to the ranges indicated in Table 7. All register read transactions will reflect the actual value stored (column 2 in Table 7) and not the one attempted to be written.

Default BB80h, indicating 48 kHz sample rate.

4.17 Extended Modem ID Register (Index 3Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ID[1:0] Codec configuration ID. Primary is 00; Secondary is 01,10,or 11. This is a reflection of the ID[1:0]# configuration pins. The state of the ID[1:0] bits is determined at power-up from the Codec ID[1:0]# pins and the current clocking scheme, see Table 15.

Default x000h. Indicating no supported modem functions.

The Extended Modem ID is a *read/write* register that identifies the CS4201 modem capabilities. Writing any value to this location issues a reset to modem registers (*Index 3Ch-54h*), including GPIO registers (*Index 4Ch - 54h*). Audio registers are not reset by a write to this location.

4.18 Extended Modem Status/Control Register (Index 3Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	PRA	0	0	0	0	0	0	0	GPIO

PRA GPIO Power Down. When ‘set’, the GPIO pins are tri-state and powered down. Input Slot 12 is marked invalid if the AC-link is active. The Serial data mode and the GPIO mode of operation are mutually exclusive. To use any GPIO function, SDEN of the *Serial Port Control Register (Index 6Ah)* must be ‘0’ prior to clearing PRA. If the SDEN bit is ‘1’, PRA is a read-only bit and always returns ‘1’.

GPIO GPIO. When ‘set’, indicates the GPIO subsystem is ready for use. If GPIO is ‘set’, input Slot 12 will also be marked valid.

Default 0100h

4.19 GPIO Pin Configuration Register (Index 4Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GC1	GC0

GC[1:0] GPIO Pin Configuration. When ‘set’, defines the corresponding GPIO pin as an input. When ‘clear’, defines the corresponding GPIO pin as an output.

Default 0003h

After a cold reset, power up, or modem register reset (see *Extended Modem ID Register (Index 3Ch)*) all GPIO pins are configured as inputs.

4.20 GPIO Pin Polarity/Type Configuration Register (Index 4Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	GP1	GP0

GP[1:0] GPIO Pin Configuration. The register defines GPIO input polarity (0 = Low, 1 = High active) when a GPIO pin is configured as an input. It defines GPIO output type (0 = CMOS, 1 = OPEN-DRAIN) when a GPIO pin is configured as an output. The GC[1:0] bits in the *GPIO Pin Configuration Register (Index 4Ch)* define the GPIO pins as inputs or outputs. See Table 8.

Default FFFFh

When the GPIO pin is defined as an input, its status is reported in the *GPIO Pin Status Register (Index 54h)* as well as input Slot 12.

GCx	GPx	Function	Configuration
0	0	Output	CMOS drive
0	1	Output	Open drain
1	0	Input	Active Low
1	1	Input	Active High (default)

Table 8. GPIO Input/Output Configurations

4.21 GPIO Pin Sticky Register (Index 50h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GS1	GS0

GS[1:0] GPIO Pin Sticky. The register defines GPIO input type (0 = not sticky, 1 = sticky) when a GPIO pin is configured as an input. The GPIO pin status of an input configured as “sticky” is ‘cleared’ by writing a ‘0’ to the corresponding bit of the *GPIO Pin Status Register (Index 54h)*, and by reset.

Default 0000h

After a cold reset or a modem register reset, this register defaults to all 0’s specifying “non-sticky”. “Sticky” is defined as edge sensitive, “non-sticky” as level sensitive.

4.22 GPIO Pin Wakeup Mask Register (Index 52h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GW1	GW0

GW[1:0] GPIO Pin Wakeup. The register provides a mask for determining if an input GPIO change will generate a wakeup or GPIO_INT (0 = No, 1 = yes). When the AC-link is powered down (*Powerdown Control/Status Register (Index 26h)* bit PR4 = 1 for primary codecs), a wakeup event will trigger the assertion of SDATA_IN. When the AC-link is powered up, a wakeup event will appear as GPIO_INT = 1 on bit 0 of input Slot 12.

Default 0000h

An AC-link wakeup interrupt is defined as a '0' to '1' transition on SDATA_IN when the AC-link is powered down (*Powerdown Control/Status Register (Index 26h)* bit PR4 = 1 for primary codecs). GPIO bits which have been programmed as inputs, "sticky", and "wakeup", upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-link wakeup if and only if the AC-link was powered down. Once the controller has re-established communication with the CS4201 following a Warm Reset, it will continue to signal the wakeup event through the GPIO_INT bit of input Slot 12 until the AC '97 controller clears the interrupt-causing bit in the *GPIO Pin Status Register (Index 54h)*; or the "wakeup", config, or "sticky" status of that GPIO pin changes.

After a cold reset or a modem register reset (see *Extended Modem ID Register (Index 3Ch)*) this register defaults to all 0's, specifying no wakeup event. The upper 14 bits of this register always return '0'.

4.23 GPIO Pin Status Register (Index 54h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	GI1	GI0

GI[1:0] GPIO Pin Status. This register reflects the state of all GPIO pin inputs and outputs. These values are also reflected in Slot 12 of every SDATA_IN frame. GPIO inputs configured as "sticky" are 'cleared' by writing a '0' to the corresponding bit of this register. The GPIO_INT bit in input Slot 12 is 'cleared' by clearing all interrupt causing bits in this register.

Default 0000h, The default value is always the state of the GPIO pin.

GPIO pins which have been programmed as inputs and "sticky", upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause the individual GI bit to go asserted '1', and remain asserted until a write of '0' to that bit. GPIO pins which have been programmed as outputs are controlled either through output Slot 12 or through this register, depending on the state of the GPOC bit in the *Misc. Crystal Control Register (Index 60h)*. If the GPOC bit is 'cleared', the GI bits in this register are read-only and reflect the status of the corresponding GPIO output pin set through output Slot 12. If the GPOC bit is 'set', the GI bits in this register are read/write bits and control the corresponding GPIO output pins.

4.24 AC Mode Control Register (Index 5Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	ASPM	0	0	DDM	AMAP	SPAS	SM1	SM0	0	0	0	0

ASPM — Analog S/PDIF Mode. This bit controls the input source to the S/PDIF transmitter block. When 'clear', the S/PDIF transmitter will receive data from the corresponding AC-link output slots. The actual slots are determined by the state of the SPAS bit. If 'set', the S/PDIF transmitter block will receive data from the ADC output.

DDM — DAC Direct Mode. This bit controls the source to the line and headphone output drivers. When 'set', the Left and Right DAC directly drive the line and headphone outputs by bypassing the audio mixer. When 'clear', the audio mixer is the source for the line and headphone outputs.

AMAP — Audio Slot Mapping. This read/write bit controls whether the CS4201 responds to the Codec ID to slot mapping as outlined in the AC '97 2.1 Specification. This bit is shadowed in the *Extended Audio ID Register (Index 28h)*. Refer to Table 9 for the slot mapping configurations.

SPAS — Alternate S/PDIF Slot Mapping. This bit controls the mapping of output slots to the S/PDIF transmitter. If this bit is '0' (default), the S/PDIF transmitter will receive data from the same slots as the DACs. If this bit is '1', alternate (independent) slots will be routed to the S/PDIF transmitter. The alternate slots are the same as the SDO2 slots in Table 9.

SM[1:0] — Slot Map. These bits define the Slot Mapping for the CS4201 when the AMAP bit is 'cleared'. Refer to Table 9 for the slot mapping configurations.

Default — 0080h

Slot Assignment Mode	Codec ID		Slot Map		AMAP	Slot Assignments							
						DAC		SDOUT		SDO2		ADC	
	ID1	ID0	SM1	SM0		SPDIF for SPAS = 0				SPDIF for SPAS = 1			
						L	R	L	R	L	R	L	R
AMAP Mode 0	0	0	X	X	1	3	4	7	8	6	9	3	4
AMAP Mode 1	0	1	X	X	1	3	4	7	8	6	9	3	4
AMAP Mode 2	1	0	X	X	1	7	8	6	9	10	11	7	8
AMAP Mode 3	1	1	X	X	1	6	9	7	8	10	11	7	8
Slot Map Mode 0	X	X	0	0	0	3	4	7	8	6	9	3	4
Slot Map Mode 1	X	X	0	1	0	7	8	6	9	10	11	7	8
Slot Map Mode 2	X	X	1	0	0	6	9	7	8	10	11	7	8
Slot Map Mode 3	X	X	1	1	0	5	11	7	8	6	9	5	6

Table 9. Slot Assignments

4.25 Misc. Crystal Control Register (Index 60h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DPC	0	0	Reserved		10dB	CRST	Reserved		GPOC	Reserved		0

DPC — DAC Phase Control. This bit controls the phase of the PCM stream sent to the DAC (after SRC). When 'cleared' the phase of the signal will remain unchanged. When this bit is 'set', each PCM sample will be inverted before being sent to the DAC.

10dB — This bit, when 'set', enables an additional boost of 10 dB on the selected microphone input. In combination with the 20dB boost bit in the *Microphone Volume Register (Index 0Eh)* this bit allows for variable boost from 0 dB to +30 dB in steps of 10 dB.

CRST — Force Cold Reset. This bit is used as an override to the New Warm Reset behavior defined during PR4 powerdown. If this bit is 'set', an active RESET# signal will force a Cold Reset to the CS4201 during a PR4 powerdown.

GPOC — General Purpose Output Control. This bit specifies the mechanism by which the status of a General Purpose Output pin can be controlled. If this bit is 'cleared', the GPO status is controlled through the standard AC '97 method of setting the appropriate bits in output Slot 12. If this bit is 'set', the GPO status is controlled through the *GPIO Pin Status Register (Index 54h)*.

Default — 0002h

4.26 S/PDIF Control Register (Index 68h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPEN	Val	0	Fs	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Emph	Copy	/Audio	Pro

SPEN — S/PDIF Enable. This bit enables S/PDIF data transmission on the SPDO/SDO2 pin. The SPEN bit routes the left and right channel data from the AC '97 controller or from the ADC output to the S/PDIF transmitter block. The actual data routed to the S/PDIF block is controlled through the ASPM/AMAP/SM1:0/SPAS configuration in the *AC Mode Control Register (Index 5Eh)*. This bit can only be 'set' if the S2EN bit in the *Serial Port Control Register (Index 6Ah)*) is '0'. When 'set', SPEN is a read-only bit and always returns '0'.

Val — Validity Bit. This bit is mapped to the V bit (bit 28) of every *sub-frame*. If this bit is '0', the signal is suitable for conversion or processing.

Fs — Sample Rate. This bit indicates the sampling rate for the S/PDIF data. The inverse of this bit is mapped to bit 25 of the channel status block. When the Fs bit is 'clear', the sampling frequency is 48 kHz. When 'set', the sampling frequency is 44.1 kHz. The actual rate at which S/PDIF data are being transmitted solely depends on the master clock frequency of the CS4201. The Fs bit is merely an indicator to the S/PDIF receiver.

L — Generation Status. This bit is mapped to bit 15 of the channel status block. For category codes 001xxxx, 0111xxx and 100xxxx a value of '0' indicates original material and a value of '1' indicates a copy of original material. For all other category codes the definition of the L bit is reversed.

CC[6:0] — Category Code. These bits are mapped to bits 8-14 of the channel status block.

Emph — Data Emphasis. This bit is mapped to bit 3 of the channel status block. If the Emph bit is '1', 50/15us filter pre-emphasis is indicated. If the bit is '0', no pre-emphasis is indicated.

Copy — Copyright. This bit is mapped to bit 3 of the channel status block. If the Copy bit is '1' copyright is not asserted and copying is permitted.

/Audio — Audio / Non-Audio. This bit is mapped to bit 1 of the channel status block. If the /Audio bit is '0', the data transmitted over S/PDIF is assumed to be digital audio. If the /Audio bit is '1', non-audio data is assumed.

Pro — Pro. This bit is mapped to bit 0 of the channel status block. If the Pro bit is '0', consumer use of the audio control block is indicated. If the bit is '1', professional use is indicated.

Default — 0000h.

Note: For a further discussion of the proper use of the channel status bits see application note *AN22: Overview of Digital Audio Interface Data Structures [3]*.

4.27 Serial Port Control Register (Index 6Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SDEN	0	0	0	0	0	0	0	0	0	0	0	S2EN	SDSC	SDF1	SDF0

SDEN — Serial Data Output Enable. When 'set', enables transmission of serial data on the SDOUT pin. It is also the master enable for S2EN and SDSC. The Serial data mode and the GPIO mode of operation are mutually exclusive. The PRA bit in the *Extended Modem ID Register (Index 3Ch)* must be 'set' prior to setting SDEN. If PRA is '0', SDEN is 'cleared' and will always returns '0'.

S2EN — Serial Port 2 Enable. Enables transmission of serial data on the SPDO/SDO2 pin. Serial Port 2 and S/PDIF modes of operation are mutually exclusive. SPEN of the *S/PDIF Control Register (Index 68h)* must be '0' and SDEN must be '1' prior to setting S2EN. If SPEN is '1' or SDEN is '0', S2EN is 'cleared' and will always return '0'.

SDSC — Serial Clock Enable. This bit enables transmission of a serial data clock on the EAPD/SCLK pin. This bit is mutually exclusive with the EAPD bit of the *Powerdown Control/Status Register (Index 26h)*. EAPD must be '0' and SDEN must be '1' before SDSC may be 'set'. If EAPD is '1' or SDEN is '0', SDSC will be 'cleared' and always return '0'.

SDF[1:0] — Serial Data Format. These bits determine the serial data format for both serial ports. Table 10 lists the available formats.

Default — 0000h

The slot assignments for the serial ports SDOUT and SDO2 are defined by AMAP and SM1:0 bit of the *AC Mode Control Register (Index 5Eh)*. The slot assignments are found in Table 9.

SDF1	SDF0	Serial Data Format
0	0	I^2S
0	1	Left Justified
1	0	Right Justified, 20-bit data
1	1	Right Justified, 16-bit data

Table 10. Serial Data Format Selection

4.28 Vendor ID1 Register (Index 7Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0

F[7:0] — First Character of Vendor ID.
43h - ASCII 'C' character.

S[7:0] — Second Character of Vendor ID.
52h - ASCII 'R' character.

Default — 4352h, Read-only data.

4.29 Vendor ID2 Register (Index 7Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0	0	DID2	DID1	DID0	1	REV2	REV1	REV0

T[7:0] Third Character of Vendor ID.
59h - ASCII ‘Y’ character.

DID[2:0] Device ID.
100 - CS4201.

REV[2:0] Revision.
001 - Revision ‘A’.

Default 594xh, Read-only data.

The two Vendor ID registers provide a means to determine the manufacturer of the AC ’97 audio codec. The first three bytes of the Vendor ID registers contain the ASCII code for the first three letters of Crystal (CRY). The final byte of the Vendor ID registers is divided into a Device ID field and a Revision field. Table 11 lists the currently defined Device ID’s.

DID2-DID0	Part Name
000	CS4297
001	CS4297A
010	CS4294/CS4298
011	CS4299
100	CS4201

Table 11. Device ID with Corresponding Part Number

5. POWER MANAGEMENT

The *Powerdown Control/Status Register (Index 26h)* controls the power management functions. Bits 14:8 in this register control the internal powerdown states of the CS4201. Powerdown control is available for individual subsections of the CS4201 by asserting any PRx bit alone or in any combination with other PRx bits. Most powerdown states can be resumed by clearing the corresponding PRx bit. PR4 and PR5 require special resume sequences. The PR4 flow is very complex and has different behavior depending on whether the CS4201 is configured as a primary or secondary codec. Contact Cirrus Logic for complete detailed functionality. Table 12 shows the mapping of the power control bits to the functions they manage.

When PR0 is 'set', the main ADCs and the Input Mux are shut down and the ADC bit (bit 0 in the *Powerdown Control/Status Register (Index 26h)*) is 'cleared' indicating the ADCs are no longer in a ready state. The same is true for the DACs, the analog mixers, and the reference voltage (Vrefout). When the PR2 or PR3 bit of the mixer is 'cleared', the mixer section will begin a power-on process and the corresponding powerdown status bit will be 'set' when the hardware is ready.

The PR5 bit disables all internal clocks and powers down the DACs and the ADCs, but maintains operation of the BIT_CLK and the analog mixer. A cold reset is the only way to restore operation to the CS4201 after a global powerdown. To achieve a complete digital powerdown, PR4 and PR5 must be asserted within a single AC output frame. This will also drive BIT_CLK 'low'.

The CS4201 does not automatically mute any input or output when the powerdown bits are 'set'. The software driver controlling the AC '97 device must manage muting the input and output analog signals before putting the part into any power management state. The definition of each PRx bit may affect a single subsection or a combination of subsection within the CS4201. Table 13 contains the matrix of subsections affected by the respective PR function. Table 14 shows the different operating power consumptions levels for different powerdown functions.

PR Bit	Function
PR0	Main ADCs and Input Mux Powerdown
PR1	Main DACs Powerdown
PR2	Analog Mixer Powerdown (Vref on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	AC-link Powerdown (BIT_CLK off)*
PR5	Internal Clock Disable
PR6	Headphone Out Powerdown
* Applies only to primary codec	

Table 12. Powerdown PR Bit Functions

PR Bit	ADC	DAC	Mixer	Headphone	Analog Reference	AC Link	Internal Clock Off
PR0	●						
PR1		●					
PR2	●	●	●	●			
PR3	●	●	●	●	●		
PR4						●	
PR5	●	●					●
PR6				●			

Table 13. Powerdown PR Function Matrix

Power State	I_{DVdd} (mA) [DVdd=3.3 V]	I_{DVdd} (mA) [DVdd=5 V]	I_{AVdd1} (mA)	I_{AVdd2} (mA)
Full Power + SRC's	27.1	44.3	34.9	5.6
Full Power + S/PDIF[a]	31.9	48.7	34.9	5.6
Full Power + HP[b]	26.3	42.7	34.9	40.6
Full Power	26.3	42.7	34.9	5.6
ADCs off (PR0)	23.4	38.1	26.0	5.6
DACs off (PR1)	24.5	39.3	28.3	5.6
Audio off (PR2)	21.5	34.1	2.9	0.8 µA
Vref off (PR3)	21.2	34.1	2.8	0.8 µA
HP amp off (PR6)	26.3	42.7	33.1	27 µA
AC-Link off (PR4)	20.9	35.2	34.9	5.6
Internal Clocks off (PR5)	3.8	6.4	19.8	5.6
Digital off (PR4+PR5)	14 µA	28 µA	19.8	5.6
PR3+PR4+PR5	14 µA	28 µA	2.3	0.5 µA
RESET	1.5 µA	8 µA	2.9	0.8 µA

Table 14. Power Consumption by Powerdown Mode

[a] Assuming standard resistive load for transformer coupled coaxial S/PDIF output (Rload = 292 Ohm, DVdd = 3.3 V) (Rload = 415 Ohm, DVdd = 5 V). General: $I_{DVdd\ S/PDIF} = I_{DVdd}$ + DVdd/Rload/2

[b] HP_OUT_L, HP_OUT_R driving 4 Vpp into 32 Ohm resistive load.

6. ANALOG HARDWARE DESCRIPTION

The analog input hardware consists of four line-level stereo inputs (LINE_L/R, CD_L/GND/R, VIDEO_L/R, and AUX_L/R), two selectable mono microphone inputs (MIC1 and MIC2), and two mono inputs (PC_BEEP and PHONE). The analog output hardware consists of a mono output (MONO_OUT), a stereo line output (LINE_OUT_L/R), and a stereo headphone output (HP_OUT_L/R). This section describes the analog hardware needed to interface with these pins. The designs presented in this section comply with specifications detailed in Chapter 17 of the Microsoft® document, *PC Design Guidelines* [7], referred to as PC 99. For information on EMI reduction techniques refer to the application note *AN165: CS4297A/CS4299 EMI Reduction Techniques* [5].

6.1 Analog Inputs

All analog inputs to the CS4201, including CD_GND, should be capacitively coupled to the input pins. Unused analog inputs should be connected together and then connected through a capacitor to analog ground or tied to the Vrefout line directly. The maximum allowed voltage for analog inputs, except the microphone input, is 1 V_{RMS}. For the microphone input the maximum allowed voltage depends on the selected boost setting.

6.1.1 Line-Level Inputs

Figure 10 shows circuitry for a line-level input. This design can be replicated for the Line, Video and Aux inputs. This design attenuates the input by 6 dB, bringing the signal from the PC 99 specified 2 V_{RMS}, to the CS4201 maximum allowed 1 V_{RMS}.

6.1.2 CD Input

The CD line-level input has an extra pin, CD_GND, providing a pseudo-differential input for both CD_L and CD_R. This pin takes the common-mode noise out of the CD inputs when connected to the CD analog source ground. Following the provided reference designs in Figure 11 and Figure 12 provides extra attenuation of common mode noise coming from the CD-ROM drive, thereby producing a higher quality signal. One percent resistors are recommended since closely matched resistor values provide better common-mode attenuation of unwanted signals. The circuit shown in Figure 11 can be used to attenuate a 2 V_{RMS} CD input signal by 6 dB. The circuit shown in Figure 12 can be used for a 1 V_{RMS} CD input signal.

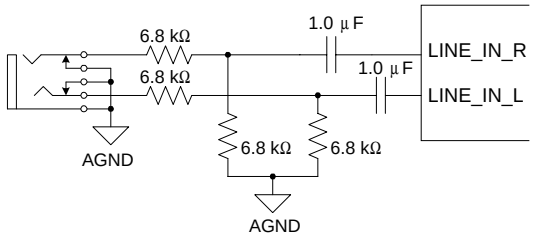


Figure 10. Line Input (Replicate for Video and AUX)

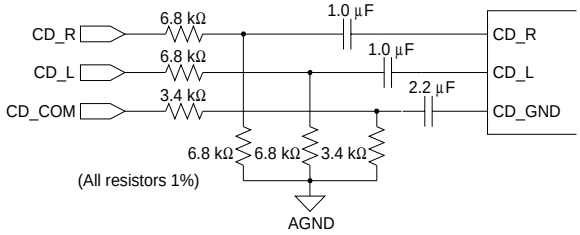


Figure 11. Differential 2 V_{RMS} CD Input

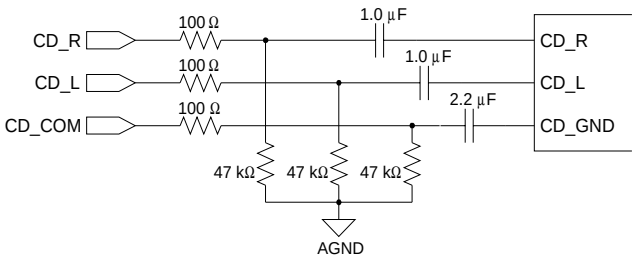


Figure 12. Differential 1 V_{RMS} CD Input

6.1.3 Microphone Inputs

Figure 13 illustrates a microphone input circuit that supports lower gain dynamic and phantom-powered microphones that use the right channel (ring) of the jack for power. It also supports the recommended advanced frequency response for voice recognition as specified in PC 99. Note the microphone input to the CS4201 has an integrated pre-amplifier. Using combinations of the 10dB bit in the *Misc. Crystal Control Register (Index 60h)* and the 20dB bit in the *Microphone Volume Register (Index 0Eh)*), the pre-amplifier gain can be set to 0 dB, 10 dB, 20 dB, or 30 dB.

6.1.4 PC Beep Input

The PC_BEEP input is useful for mixing the output of the "beeper" (timer chip), provided in many PCs, with the other audio signals. When the CS4201 is held in reset, PC_BEEP is passed directly to the line output. This allows the system sounds or "beeps" to be available before the AC '97 interface has been activated. This feature is affected by the HPCFG pin; see Section 12 for the pin description. Figure 14 illustrates a typical input circuit for the PC_BEEP input. If PC_BEEP is driven from a CMOS gate, the 4.7 kΩ resistor should be tied to analog ground instead of +5 VA. Although this input is described for a low-quality beeper, it is of the same high-quality as all other analog inputs and may be used for other purposes.

6.1.5 Phone Input

One application of the PHONE input is to interface to the output of a modem analog front end (AFE) device so that modem dialing signals and protocol negotiations may be monitored through the audio system. Figure 15 shows a design for a modem connection where the output is fed from the CS4201 MONO_OUT pin through a divider. The divider ratio shown does not attenuate the signal, providing an output voltage of 1 V_{RMS}. If a lower output voltage is desired, the resistors can be replaced with appropriate values, as long as the total load on the output is kept greater than 10 kΩ. The PHONE input is attenuated by 6 dB to accommodate a line-level source of 2 V_{RMS}.

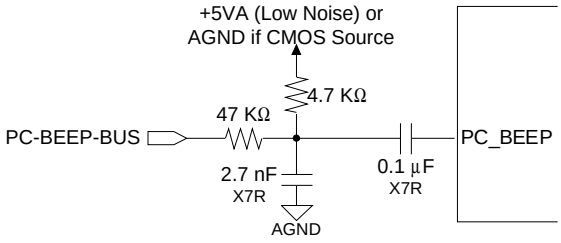


Figure 14. PC_BEEP Input

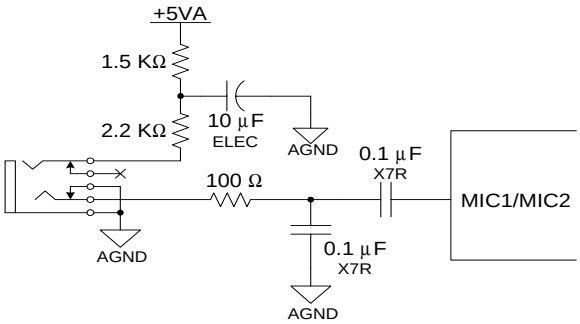


Figure 13. Microphone Input

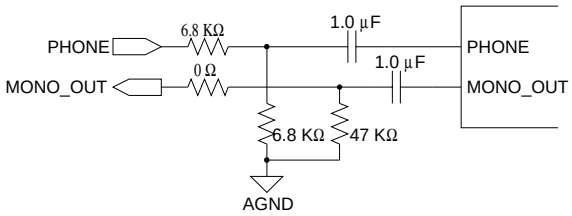


Figure 15. Modem Connection

6.2 Analog Outputs

Each analog output is DC-biased up to the Vrefout voltage signal reference which is nominally 2.4 V. This requires the outputs be AC-coupled to external circuitry (AC loads must be greater than 10 kΩ for LINE_OUT or 32 Ω for HP_OUT). The HP_OUT coupling capacitors should be 220 µF or greater in order to prevent low frequency roll-off. In addition, the LINE_OUT_L, LINE_OUT_R, and MONO_OUT pins require 680 pF to 1000 pF NPO dielectric capacitors between the corresponding pin and analog ground.

6.2.1 Stereo Outputs

The LINE_OUT and HP_OUT stereo outputs depend on the configuration of the HPCFG pin. As shown in Figure 16, if the HPCFG pin is left floating, the part behaves as specified in AC '97. As shown in Figure 17, if the HPCFG pin is grounded, the part behaves as if HP_OUT was the only output. In this case, LINE_OUT will be muted, the *Master Volume Register (Index 02h)* will control HP_OUT and PC_BEEP will be routed to HP_OUT during RESET.

6.2.2 Mono Output

The mono output, MONO_OUT, can be either a sum of the left and right output channels, attenuated by 6 dB to prevent clipping at full scale, or the selected Mic signal. The mono out channel can drive the PC internal mono speaker using an appropriate buffer circuit.

6.3 Miscellaneous Analog Signals

The AFLT1 and AFLT2 pins must have a 1000 pF NPO capacitor to analog ground. These capacitors provide a single-pole low-pass filter at the inputs to the ADCs. This makes low-pass filters at each analog input pin unnecessary.

The REFFLT pin must have a 2.2 µF and 0.1 µF capacitor connected to analog ground with a short, wide trace to this pin (see Figure 17 in Section 11, *Grounding and Layout*, for an example). The 2.2 µF capacitor must not be replaced by any other value and must be ceramic with low leakage current. Electrolytic capacitors should not be used. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the CS4201. Likewise, digital signals should be kept away from REFFLT for similar reasons.

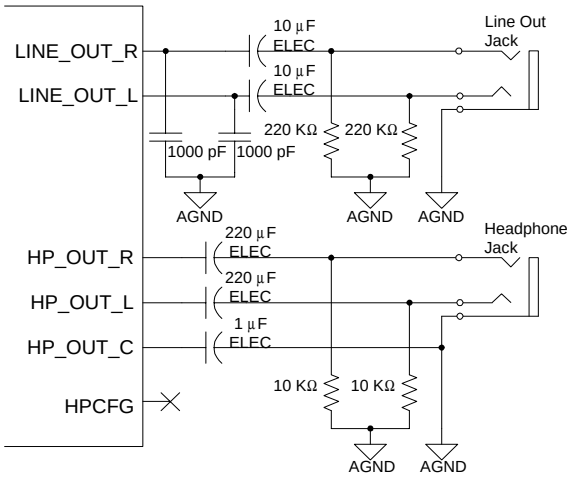


Figure 16. Line Out and Headphone Out Setup

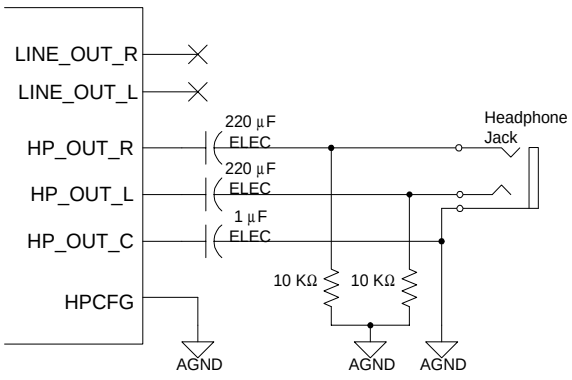


Figure 17. Line Out/Headphone Out Setup

6.4 Power Supplies

The power supplies providing analog power should be as clean as possible to minimize coupling into the analog section which could degrade analog performance. One analog power pin, AVdd2, supplies power to the headphone output circuitry on the CS4201. The other analog power pin, AVdd1, supplies power to the rest of the CS4201 analog circuitry. The +5 V analog supply should be generated from a voltage regulator (7805 type) connected to a +12 V supply. This helps isolate the analog circuitry from noise typically found on +5 V digital supplies. A typical voltage regulator circuit for analog power using a MC78M05CDT +5V regulator is shown in Figure 18. The digital power pins, DVdd1 and DVdd2, should be connected to the same digital supply as the controller's AC-link interface. Since the digital interface on the CS4201 may operate at either +3.3 V or +5 V, proper connection of these pins will depend on the digital power supply of the controller.

6.5 Reference Design

Figure 19 shows a simple reference design for the CS4201 using the internal headphone amplifier in a line out\headphone out setup.

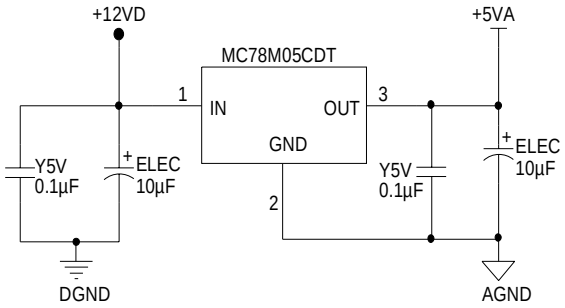


Figure 18. +5V Analog Voltage Regulator

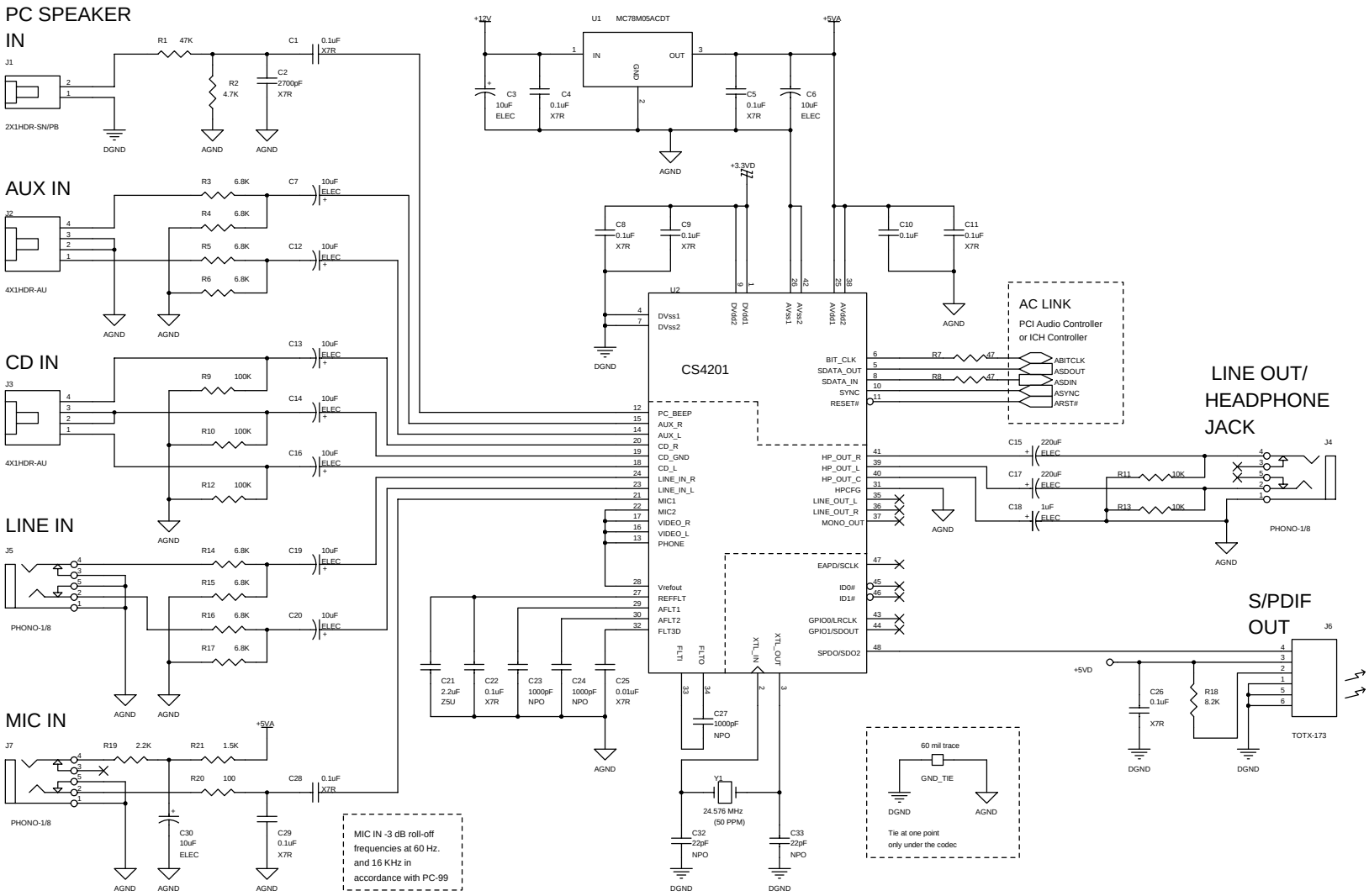
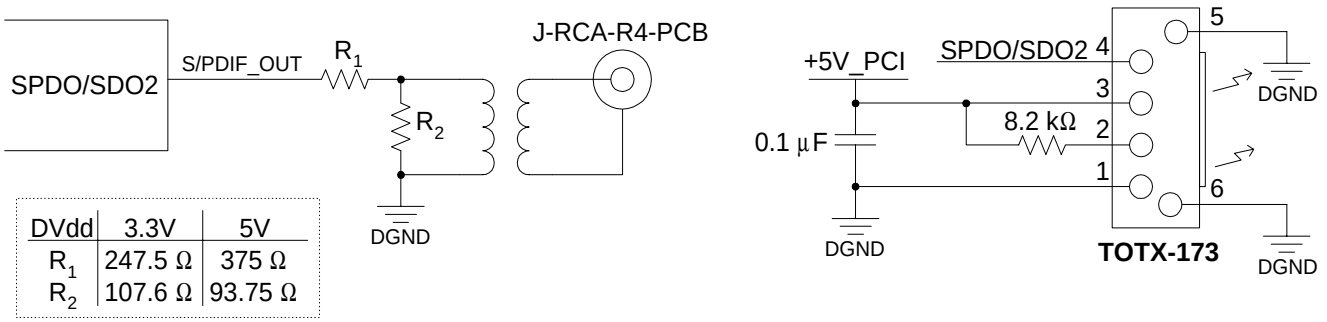


Figure 19. CS4201 Reference Design

7. SONY/PHILIPS DIGITAL INTERFACE (S/PDIF)

The S/PDIF digital output is used to interface the CS4201 to consumer audio equipment external to the PC. This output provides an interface for storing digital audio data or playing digital audio data to digital speakers. Figure 20 illustrates the circuit necessary for implementation of the IEC-958 optical or consumer interface. For further information on S/PDIF operation, see the application note *AN22: Overview of Digital Audio Interface Data Structures* [3]. Also see application note *AN134: AES and S/PDIF Recommended Transformers* [4] for information on S/PDIF recommended transformers.



DVdd	3.3V	5V
R_1	247.5 Ω	375 Ω
R_2	107.6 Ω	93.75 Ω

Figure 20. Consumer and Optical S/PDIF Outputs

8. CLOCKING

The CS4201 may be operated as the primary or secondary codec. As a primary codec, the system clock for the AC-link may be generated from an external 24.576 MHz clock source, a 24.576 MHz crystal, or use the internal Phase Locked Loop (PLL). The PLL allows the CS4201 to accept external clock frequencies other than 24.576 MHz. The CS4201 uses the presence or absence of a valid clock on the XTL_IN pin in conjunction with the ID[1:0]# pins to determine the clocking configuration.

8.1 PLL Operation (External Clock)

The PLL mode is activated if a valid clock is present on XTL_IN during the rising edge of RESET#. Once PLL mode is entered, the XTL_OUT pin is redefined as the PLL loop filter, as shown in Figure 21. The ID[1:0]# inputs determine the configuration of the internal divider ratios required to generate the 12.288 MHz BIT_CLK output, see Table 15 for additional details. In PLL mode, the CS4201 is configured as a primary codec independent of the state of the ID[1:0]# pins. If 24.576 MHz is chosen as the external clock input (ID[1:0]# left open or both pulled to logic 1), the PLL is disabled and the clock is used directly. The loop filter is not required and XTL_OUT is left unconnected. For all other clock input choices, the loop filter is required. The ID[1:0] bits of the *Extended Audio ID Register (Index 28h)* and the *Extended Modem ID Register (Index 3Ch)* will always report 0 in PLL mode.

8.2 24.576 MHz Crystal Operation

If a valid clock is not present on XTL_IN during the rising edge of RESET#, the device disables the PLL input and latches the state of the ID[1:0]# inputs. If the ID[1:0]# inputs are both pulled high or left floating, the device is configured as a primary codec. An external 24.576 MHz crystal is used as the system clock as shown in Figure 22. If either ID[1:0]# inputs are pulled low, the device is determined to be a secondary codec. The BIT_CLK pin is configured as an input and the CS4201 is driven from the 12.288 MHz BIT_CLK of the primary codec. The ID[1:0] bits of the *Extended Audio ID Register (Index 28h)* and the *Extended Modem ID Register (Index 3Ch)* will report the state of the ID[1:0]# inputs.

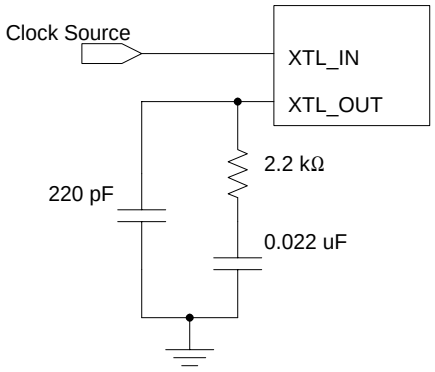


Figure 21. PLL External Loop Filter

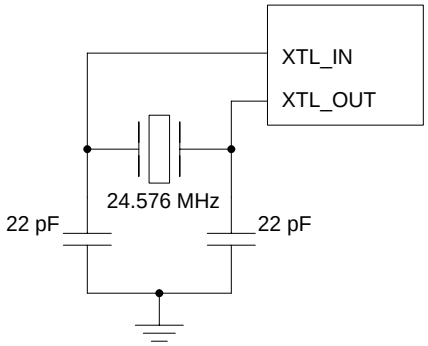


Figure 22. External Crystal

External Clock on XTL_IN	ID1#	ID0#	AC-Link Timing Mode	Codec ID	Clock Source	Clock Rate (MHz)	PLL Active	Application Notes
Yes	1	1	Primary	0	External	24.576	No	clock generator driving XTL_IN
Yes	1	0	Primary	0	External	14.31818	Yes	external clock source driving XTL_IN loop filter connected to XTL_OUT
Yes	0	1	Primary	0	External	27.000	Yes	
Yes	0	0	Primary	0	External	48.000	Yes	
No	1	1	Primary	0	XTAL	24.576	No	crystal connected to XTL_IN, XTL_OUT
No	1	0	Secondary	1	BIT_CLK	12.288	No	BIT_CLK from primary codec driving BIT_CLK on all secondary codecs
No	0	1	Secondary	2	BIT_CLK	12.288	No	
No	0	0	Secondary	3	BIT_CLK	12.288	No	

Table 15. Clocking Configurations

9. SERIAL DATA PORTS

9.1 Overview

The CS4201 features two serial data ports that can be used to send AC-link data to one or two external stereo DACs to support a total of up to six audio channels. The first serial port takes the digital audio data from the SDOUT slots and the second serial port takes the digital audio data from the SDO2 slots. See Table 9 for the actual slots used depending on configuration.

Each serial port consists of four signals: MCLK, SCLK, LRCLK, and SDATA. The existing 256 Fs BIT_CLK will be used as MCLK. All clocks are shared between the two serial ports with only the SDATA pins being separate; SDOUT for the first serial port and SDO2 for the second serial port. Figure 23 shows the principal connections for multi-channel applications of the CS4201.

The serial data port is controlled by the SDEN, S2EN, and SDSC bits in the *Serial Port Control Register (Index 6Ah)*. All the pins for the serial data ports are multiplexed with other functions and cannot be used unless the other function is disabled or powered down. Refer to Section 10, *Exclusive Functions*, for additional information on controlling the serial data ports. Some audio DACs can run in an internal SCLK mode where SCLK is internally derived from MCLK and LRCLK. In this case, SCLK generation in the CS4201 is optional.

A feature has been designed into the CS4201 that allows the phase of the internal DAC to be reversed. This is necessary since it is unknown what phase response a particular external DAC might have. Also, the phase response of the internal DAC can vary depending on the path determined by the POP bit in the *General Purpose Register (Index 20h)*, the DDM bit in the *AC Mode Control Register (Index 5Eh)* and which output (LINE_OUT or HP_OUT) is being used. This feature assures that all DACs in a system have the same phase response to maintain the accuracy of spatial cues. The DAC phase is controlled by the DPC bit in the *Misc. Crystal Control Register (Index 60h).*

Please note the data sent to the serial ports is straight from the AC-link. There is no SRC and no volume control available on this data, so it is the responsibility of the controller or host software to provide this functionality if desired.

9.2 Serial Data Formats

In order to support a wide variety of serial audio DACs, the CS4201 can provide serial data in four different formats. The desired format is selected through the SDF[1:0] bits in the *Serial Port Control Register (Index 6Ah)*. Both serial ports, if enabled, use the same serial data format. In all cases, LRCLK will be synchronous with Fs, and SCLK will be 64 Fs (BIT_CLK / 4). Serial data is transitioned by the CS4201 on the falling edge of SCLK and latched by the DAC on the next rising edge. Serial data is shifted out MSB first in all supported formats, but LRCLK polarity as well as data justification, alignment, and resolution vary. Table 16 shows the principal characteristics of each format.

SDF[1:0]	LRCLK Polarity	Data Justification	Data Alignment (MSB vs. LRCLK)	Data Resolution	Timing Diagram	Recommended DAC
0 0	negative	left justified	1 SCLK delayed	20-bit	Figure 24	CS4334
0 1	positive	left justified	not delayed	20-bit	Figure 25	CS4335
1 0	positive	right justified	not delayed	20-bit	Figure 26	CS4337
1 1	positive	right justified	not delayed	16-bit	Figure 27	CS4338

Table 16. Serial Data Formats and Compatible DACs

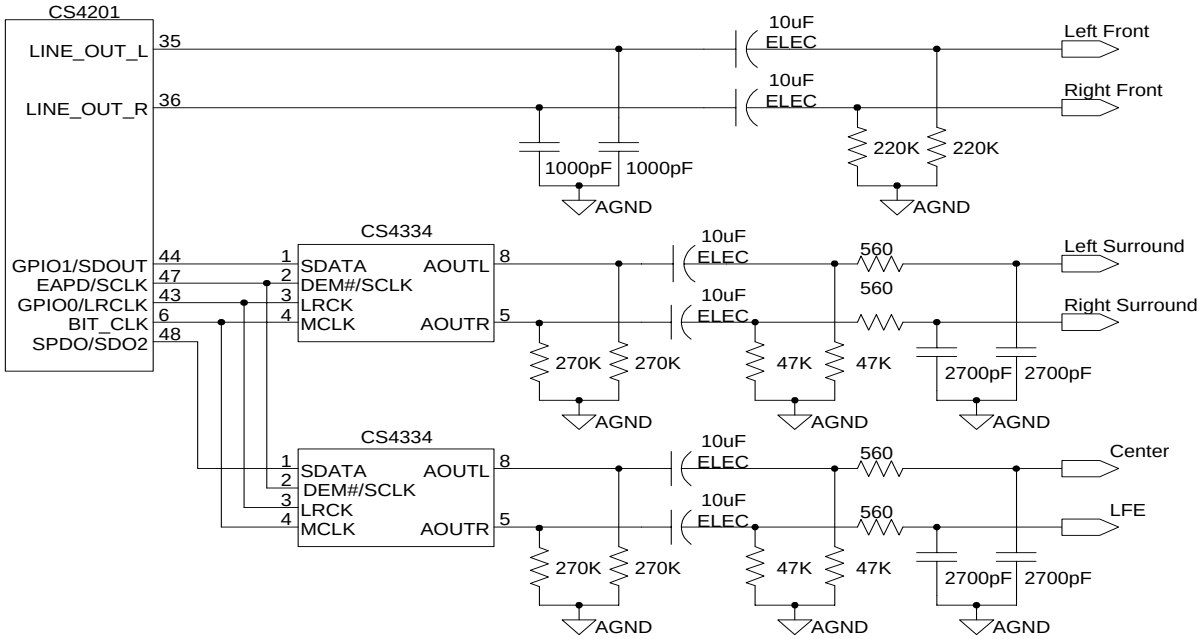


Figure 23. Serial Data Port Connection Diagram

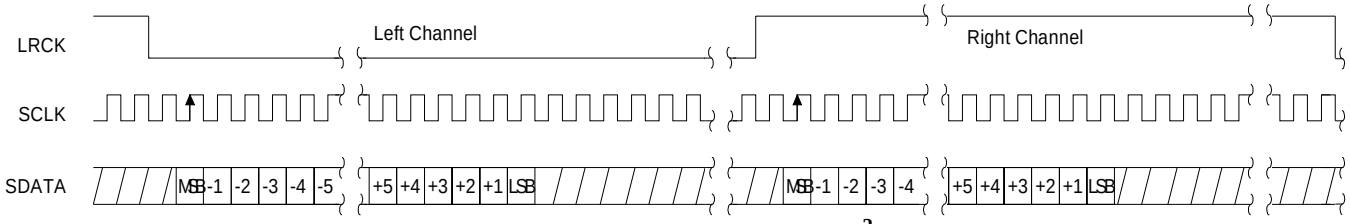


Figure 24. Serial Data Format 0 (I^2S)

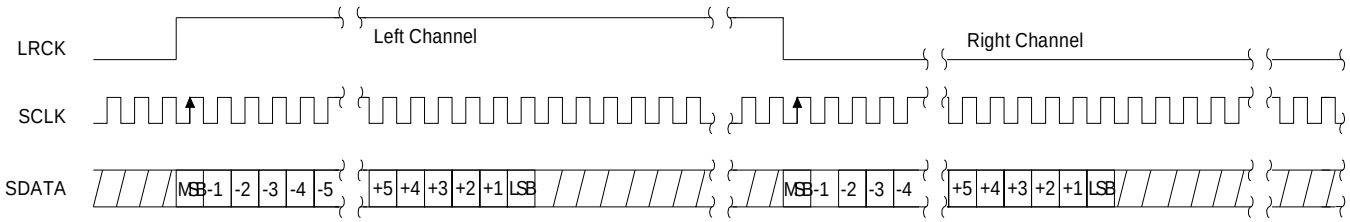


Figure 25. Serial Data Format 1 (Left Justified)

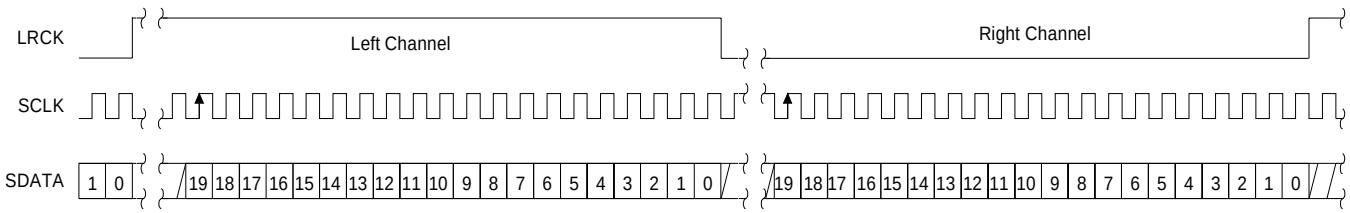


Figure 26. Serial Data Format 2 (Right Justified, 20-bit data)

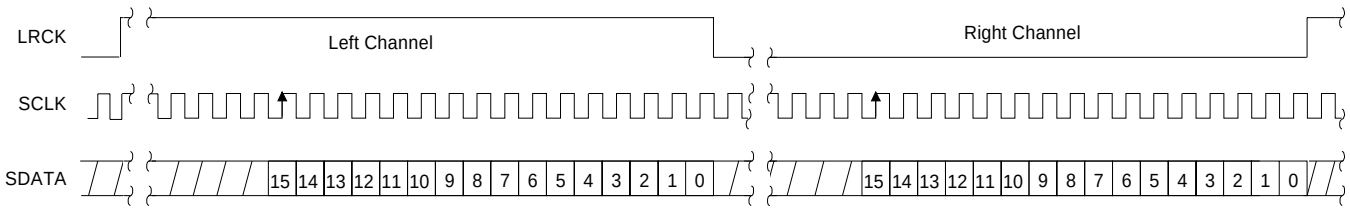


Figure 27. Serial Data Format 3 (Right Justified, 16-bit data)

10. EXCLUSIVE FUNCTIONS

Some of the digital pins on the CS4201 have multiplexed functionality. These functions are mutually exclusive and cannot be requested at the same time. The following pairs of functions are mutually exclusive:

- GPIO and Serial Data Port (GPIO0 pin is shared with LRCLK pin and GPIO1 pin is shared with SDOUT pin)
- EAPD and Serial Data Port Serial Clock (EAPD pin is shared with SCLK pin)
- S/PDIF and Second Serial Data Port (SPDO pin is shared with SDO2 pin)

There is no priority assigned to these operational modes. A function currently in use must be disabled or powered down before the corresponding exclusive function can be enabled. The following control bits for these functions will behave differently than normal bits: the EAPD bit in the *Power-down Control/Status Register (Index 26h)*, the PRA bit in the *Extended Modem Status/Control Register (Index 3Eh)*, the SPEN bit in the *S/PDIF Control Register (Index 68h)*, and the SDEN, S2EN and SDSC bits in the *Serial Port Control Register (Index 6Ah)*. These bits can become read-only if they control a feature that is currently unavailable because the corresponding exclusive feature is already in use.

11. GROUNDING AND LAYOUT

Figure 28 shows the conceptual layout for the CS4201. The decoupling capacitors should be located physically as close to the pins as possible. Also, note the connection of the REFFLT decoupling capacitors to the ground return trace connected directly to the ground return pin, AVss1.

It is strongly recommended that separate analog and digital ground planes be used. Separate ground planes keep digital noise and return currents from modulating the CS4201 ground potential and degrading performance. The digital ground pins should be connected to the digital ground plane and kept separate from the analog ground connections of the CS4201 and any other external analog circuitry. All analog components and traces should be located over the analog ground plane and all digital components and traces should be located over the digital ground plane.

The common connection point between the two ground planes (required to maintain a common ground voltage potential) should be located under the CS4201. The AC-link digital interface connection traces should be routed such that the digital ground plane lies underneath these signals (on the internal ground layer). This applies along the entire length of these traces from the AC '97 controller to the CS4201.

Refer to the Application Note *AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices* [2] for more information on layout and design rules.

.

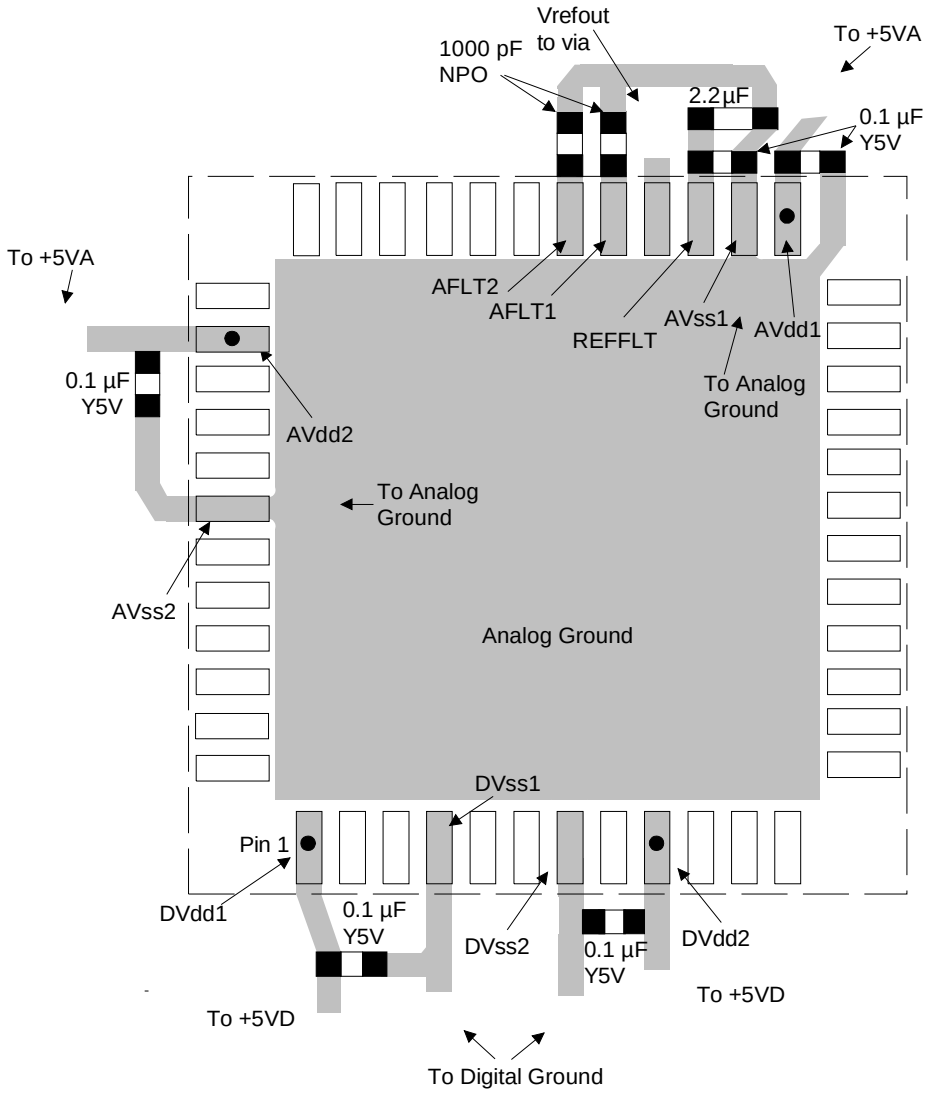
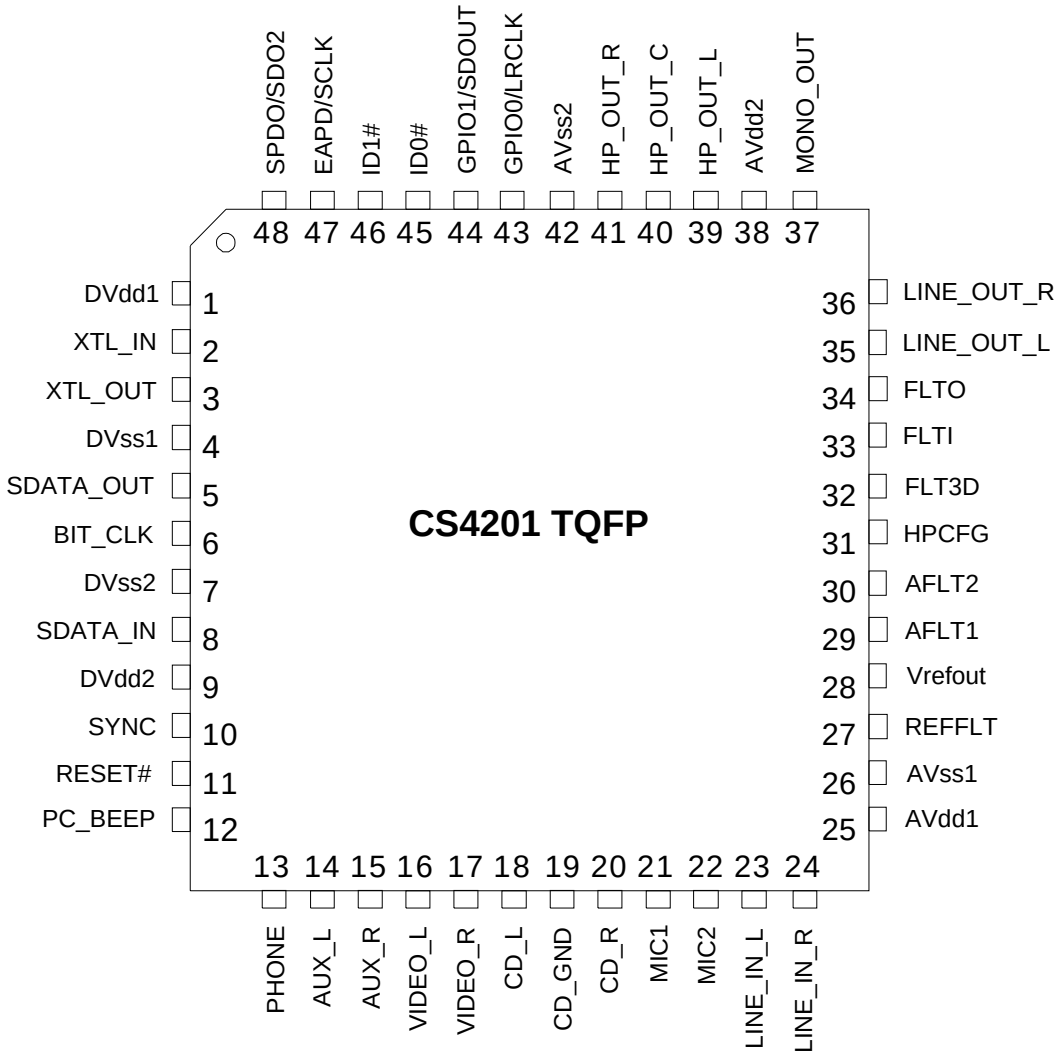


Figure 28. Conceptual Layout for the CS4201

12. PIN DESCRIPTIONS



Audio I/O

PC_BEEP - Analog Mono Source, Input, Pin 12

The PC_BEEP input is intended to allow the PC system POST (Power On Self-Test) tones to pass through to the audio subsystem. The PC_BEEP input has two connections: the first connection is to the analog output mixer, the second connection is directly to the LINE_OUT stereo outputs (if HPCFG is floating) or through the headphone amplifier to the HP_OUT pins (if HPCFG is tied low). While the RESET# pin is actively being asserted to the CS4201, the PC_BEEP bypass path to the LINE_OUT/HP_OUT outputs is enabled. While the CS4201 is in the normal operation mode with RESET# de-asserted, PC_BEEP is a monophonic source to the analog output mixer. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

PHONE - Analog Mono Source, Input, Pin 13

This analog input is a monophonic source to the analog output mixer. It is intended to be used as a modem subsystem input to the audio subsystem. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

MIC1 - Analog Mono Source, Input, Pin 21

This analog input is a monophonic source to the analog output mixer. It is intended to be used as a desktop microphone connection to the audio subsystem. The CS4201 internal mixer microphone input is MUX selectable with either MIC1 or MIC2 as the input. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

MIC2 - Analog Mono Source, Input, Pin 22

This analog input is a monophonic source to the analog output mixer. It is intended to be used as an alternate microphone connection to the audio subsystem. The CS4201 internal mixer microphone input is MUX selectable with either MIC1 or MIC2 as the input. The maximum allowable input is 1 V_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

LINE_IN_L, LINE_IN_R - Analog Line Source, Inputs, Pins 23 and 24

These inputs form a stereo input pair to the CS4201. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

CD_L, CD_R - Analog CD Source, Inputs, Pins 18 and 20

These inputs form a stereo input pair to the CS4201. It is intended to be used for the Red Book CD audio connection to the audio subsystem. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

CD_GND - Analog CD Common Source, Input, Pin 19

This analog input is used to remove common mode noise from Red Book CD audio signals. The impedance on the input signal path should be one half the impedance on the CD_L and CD_R input paths. This pin requires AC-coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC-coupled to analog ground.

VIDEO_L, VIDEO_R - Analog Video Audio Source, Inputs, Pins 16 and 17

These inputs form a stereo input pair to the CS4201. It is intended to be used for the audio signal output of a video device. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

AUX_L, AUX_R - Analog Auxiliary Source, Inputs, Pins 14 and 15

These inputs form a stereo input pair to the CS4201. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. If these inputs are not used, they should both be connected to the Vrefout pin or both AC-coupled, with separate AC-coupling caps, to analog ground.

LINE_OUT_L, LINE_OUT_R - Analog Line Level, Outputs, Pins 35 and 36

These signals are analog outputs from the stereo output mixer. The full-scale output voltage for each output is nominally 1 V_{RMS} (sinusoidal). These outputs are internally biased at the Vrefout voltage reference and require either AC-coupling to external circuitry or DC-coupling to a buffer op-amp biased at the Vrefout voltage. These pins need a 680-1000 pF NPO capacitor attached to analog ground.

HP_OUT_L, HP_OUT_R - Analog Headphone, Outputs, Pins 39 and 41

These signals are analog outputs from the stereo output mixer. The full-scale output voltage for each output is nominally 4 V_{pp}. These outputs are internally biased at the Vrefout voltage reference and require AC-coupling to external circuitry. The HP_OUT pins can directly drive resistive loads as low as 32 Ω (such as standard consumer headphones). Capacitive loading must not exceed 200 pF/pin. The outputs are short circuit protected for infinite duration.

HP_OUT_C - Analog Headphone Output Common Source, Input, Pin 40

This analog input is used to remove common mode noise from the headphone outputs. This is achieved by biasing the headphone amplifier with the common mode noise on the headphone amplifier ground plane. This pin should be AC-coupled through a 1 µF ELEC capacitor to analog ground (AVss2) near the headphone jack.

MONO_OUT - Analog Mono Line Level, Output, Pin 37

This signal is an analog output from the stereo-to-mono mixer. The full-scale output voltage for this output is nominally 1 V_{RMS} (sinusoidal). This output is internally biased at the Vrefout voltage reference and requires either AC-coupling to external circuitry or DC-coupling to a buffer op-amp biased at the Vrefout voltage. This pin needs a 680 - 1000 pF NPO capacitor attached to analog ground.

Analog Reference, Filters, and Configuration

REFFLT - Internal Reference Voltage, Input, Pin 27

This is the voltage reference used internal to the part. A 0.1 µF and a 2.2 µF capacitor with short, wide traces must be connected to this pin. No other connections should be made to this pin. Do not use an electrolytic 2.2 µF capacitor; use type Z5U or Y5V. Two 1.0 µF capacitors in parallel can be used in place of the 2.2 µF capacitor.

Vrefout - Voltage Reference, Output, Pin 28

All analog inputs and outputs are centered around Vrefout which is nominally 2.4 Volts. This pin may be used to level shift external circuitry. It can also drive up to 5 mA of DC which can be used for microphone bias.

AFLT1 - Left Channel Antialiasing Filter, Input, Pin 29

This pin needs a 1000 pF NPO capacitor attached to analog ground.

AFLT2 - Right Channel Antialiasing Filter, Input, Pin 30

This pin needs a 1000 pF NPO capacitor attached to analog ground.

FLTI, FLTO - Filter Input/Filter Output, Pins 33 and 34

A 1000 pF capacitor must be attached between FLTI and FLTO if the 3D function is used.

FLT3D - 3D Filter, Pin 32

A 0.01 µF X7R capacitor must be attached from this pin to AGND if the 3D function is used.

HPCFG - Headphone Configuration, Input, Pin 31

This pin is the configuration control for the signal routing to the headphone amplifier. If this pin is left floating, LINE_OUT and HP_OUT function as defined in the AC '97 specification. If this pin is grounded, the HP_OUT behaves as a buffered line output. The LINE_OUT outputs are muted, the control for the HP_OUT will be *Master Volume Register (Index 02h)* and PC_BEEP is routed to HP_OUT during RESET. The pin is internally pulled up to the analog supply voltage.

AC-Link

RESET# - AC '97 Chip Reset, Input, Pin 11

This active low signal is the asynchronous cold reset input to the CS4201. The CS4201 must be reset before it can enter normal operating mode.

SYNC - AC-Link Serial Port Sync pulse, Input, Pin 10

This signal is the serial port timing signal for the AC-link. Its period is the reciprocal of the maximum sample rate, 48 kHz, and is generated by the AC '97 controller synchronous to BIT_CLK. SYNC is also an asynchronous input when the CS4201 is configured as a primary device and is in a PR4 powerdown state. A series terminating resistor of 47 Ω should be connected on this signal close to the controller.

BIT_CLK - AC-Link Serial Port Master Clock, Input/Output, Pin 6

This input/output signal controls the master clock timing for the AC-link. When the CS4201 is in primary mode, this signal is a 12.288 MHz output clock signal derived from either a 24.576 MHz crystal or from the internal PLL based on the XTL_IN input clock. When the CS4201 is in secondary mode, this signal is an input which controls the AC-link serial interface and generates all internal clocking including the AC-link serial interface timing and the analog sampling clocks. A series terminating resistor of 47 Ω should be connected on this signal close to the CS4201 in primary mode or close to the BIT_CLK source in secondary mode.

SDATA_OUT - AC-Link Serial Data Input Stream to AC '97, Input, Pin 5

This input signal receives the control information and digital audio output streams. The data is clocked into the CS4201 on the falling edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal close to the controller.

SDATA_IN - AC-Link Serial Data Output Stream from AC '97, Output, Pin 8

This output signal transmits the status information and digital audio input streams from the ADCs. The data is clocked out of the CS4201 on the rising edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal as close to the CS4201 as possible.

Clock and Configuration

XTL_IN - Crystal Input/Clock Input, Pin 2

This pin requires either a 24.576 MHz crystal, with the other pin attached to XTL_OUT, or an external CMOS clock. The crystal must be designed for fundamental mode, parallel resonance operation. When configured as a secondary codec, all timing is derived from the BIT_CLK input signal; this pin should be left floating. See Section 8, *Clocking*, for additional details.

XTL_OUT - Crystal Output/ PLL Loop Filter, Pin 3

Used for a crystal placed between this pin and XLT_IN. If an external clock is used on XTL_IN, this pin is configured as the loop filter for the internal PLL circuitry. See Section 8, *Clocking*, for additional details.

ID1#, ID0# - Codec ID, Inputs, Pins 45 and 46

These pins select the Codec ID for the CS4201, as well as determine the rate of the incoming clock in PLL mode. They are only sampled after the rising edge of RESET#. These pins are internally pulled up to the digital supply voltage and should be left floating for logic '0' or tied to digital ground for logic '1'.

Misc. Digital Interfaces

SPDO/SDO2 - Sony/Philips Digital Interface Output / Serial Data Output 2, Pin 48

This pin generates the S/PDIF digital output from the CS4201 when the SPEN bit in the *S/PDIF Control Register (Index 68h)* is 'set'. This output may be used to directly drive a resistive divider and coupling transformer to an RCA-type connector for use with consumer audio equipment. This pin also provides the serial data for the second serial data port when the S2EN bit in the *Serial Port Control Register (Index 6Ah)* is 'set'. These two functions are mutually exclusive. When neither function is being used this output is driven to a logic '0'.

EAPD/SCLK - External Amplifier Power Down / Serial Clock, Output, Pin 47

This signal is designated as a power down control for audio amplifiers external to the CS4201. The output is determined by the EAPD bit in the *Powerdown Control/Status Register (Index 26h)* and is low by default. When the serial data interface is enabled, this output is configured as the serial clock for both serial data ports when the SDSC bit in the *Serial Port Control Register (Index 6Ah)* is 'set'.

GPIO0/LRCLK - General Purpose I/O / Left-Right Clock, Input/Output, Pin 43

This pin is a general purpose I/O pin that can be used to interface with various external circuitry. When configured as an input, it functions as a Schmitt triggered input with 350 mV hysteresis at 5 V and 220 mV hysteresis at 3.3 V. When configured as an output, it can function as a normal CMOS output (4 mA drive) or as an open drain output. This pin also provides the L/R clock for both serial data ports when the SDEN bit in the *Serial Port Control Register (Index 6Ah)* is 'set'. This bit powers up in the high impedance state for backward compatibility.

GPIO1/SDO1 - General Purpose I/O / Serial Data Ouput 1, Input/Output, Pin 44

This pin is a general purpose I/O pin that can be used to interface with various external circuitry. When configured as an input, it functions as a Schmitt triggered input with 350 mV hysteresis at 5 V and 220 mV hysteresis at 3.3 V. When configured as an output, it can function as a normal CMOS output (4 mA drive) or as an open drain output. This pin also provides the serial data for the first serial data port when the SDEN bit in the *Serial Port Control Register (Index 6Ah)* is 'set'. This bit powers up in the high impedance state for backward compatibility.

Power Supplies

DVdd1, DVdd2 - Digital Supply Voltage, Pins 1 and 9

Digital supply voltage for the AC-link section of the CS4201. These pins can be tied to +5 V digital or to +3.3 V digital. The CS4201 and controller's AC-link should share a common digital supply.

DVss1, DVss2 - Digital Ground, Pins 4 and 7

Digital ground connection for the AC-link section of the CS4201. These pins should be isolated from analog ground currents.

AVdd1, AVdd2 - Analog Supply Voltage, Pins 25 and 38

Analog supply voltage for the analog and mixed signal section of the CS4201 (AVdd1) as well as the headphone amplifier (AVdd2). These pins must be tied to the analog +5 V power supply. It is strongly recommended that +5 V be generated from a voltage regulator to ensure proper supply currents and noise immunity from the rest of the system.

AVss1, AVss2 - Analog Ground, Pins 26 and 42

Ground connection for the analog, mixed signal, and substrate sections of the CS4201 (AVss1) as well as the headphone amplifier (AVss2). These pins should be isolated from digital ground currents.

13. PARAMETER AND TERM DEFINITIONS

AC '97 Specification

Refers to the *Audio Codec '97 Component Specification Ver 2.1* published by Intel® Corporation [6].

AC '97 Controller or Controller

Refers to the control chip which interfaces to the audio codec AC-link. This has been also called *DC '97* for Digital Controller '97 [6].

AC '97 Registers or Codec Registers

Refers to the 64-field register map defined in the AC '97 Specification.

ADC

Refers to a single Analog-to-Digital converter in the CS4201. "ADCs" refers to the stereo pair of Analog-to-Digital converters. The CS4201 ADCs have 18-bit resolution.

DAC

A single Digital-to-Analog converter in the CS4201 "DACs" refers to the stereo pair of Digital-to-Analog converters. The CS4201 DACs have 20-bit resolution.

SRC

Sample Rate Converter. Converts data derived at one sample rate to a differing sample rate. The CS4201 operates at a fixed sample frequency of 48 kHz. The internal sample rate converters are used to convert digital audio streams playing back at other frequencies to 48 kHz.

Codec

Refers to the chip containing the ADCs, DACs, and analog mixer. In this data sheet, the codec is the CS4201.

FFT

Fast Fourier Transform.

Resolution

The number of bits in the output words to the DACs, and in the input words to the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

dB FS A

dB FS is defined as dB relative to full-scale. The "A" indicates an A weighting filter was used.

Frequency Response (FR)

FR is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

Dynamic Range (DR)

DR is the ratio of the RMS full-scale signal level divided by the RMS sum of the noise floor, in the presence of a signal, available at any instant in time (no change in gain settings between measurements). Measured over a 20 Hz to 20 kHz bandwidth with units in dB FS A.

Total Harmonic Distortion plus Noise (THD+N)

THD+N is the ratio of the RMS sum of all non-fundamental frequency components, divided by the RMS full-scale signal level. It is tested using a -3 dB FS input signal and is measured over a 20 Hz to 20 kHz bandwidth with units in dB FS.

Signal to Noise Ratio (SNR)

SNR, similar to DR, is the ratio of an arbitrary sinusoidal input signal to the RMS sum of the noise floor, in the presence of a signal. It is measured over a 20 Hz to 20 kHz bandwidth with units in dB.

S/PDIF

Sony/Phillips Digital Interface. This interface was established as a means of digitally interconnecting consumer audio equipment. The documentation for S/PDIF has been superseded by the IEC-958 consumer digital interface document.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded AC-coupled line input channel with 1 kHz, 0 dB, signal present on the other line input channel. Units are in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage to get an equal code on both channels. For the DACs, the difference in output voltages for each channel when both channels are fed the same code. Units are in dB.

PATHS

A-D: Analog in, through the ADC, onto the serial link.

D-A: Serial interface inputs through the DAC to the analog output.

A-A: Analog in to Analog out (analog mixer).

PLL

Phase Lock Loop. Circuitry for generating a desired clock from an external clock source.

14. REFERENCES

1) Cirrus Logic, Audio Quality Measurement Specification, Version 1.0, 1997.
http://www.cirrus.com/products/papers/meas/meas.html

2) Cirrus Logic, AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, Version 6.0, February 1998.

3) Cirrus Logic, AN22: Overview of Digital Audio Interface Data Structures, Version 2.0, February 1998.

4) Cirrus Logic, AN134: AES and S/PDIF Recommended Transformers, Version 2, April 1999.

5) Cirrus Logic, AN165: CS4297A/CS4299 EMI Reduction Techniques, Version 1.0, September 1999.

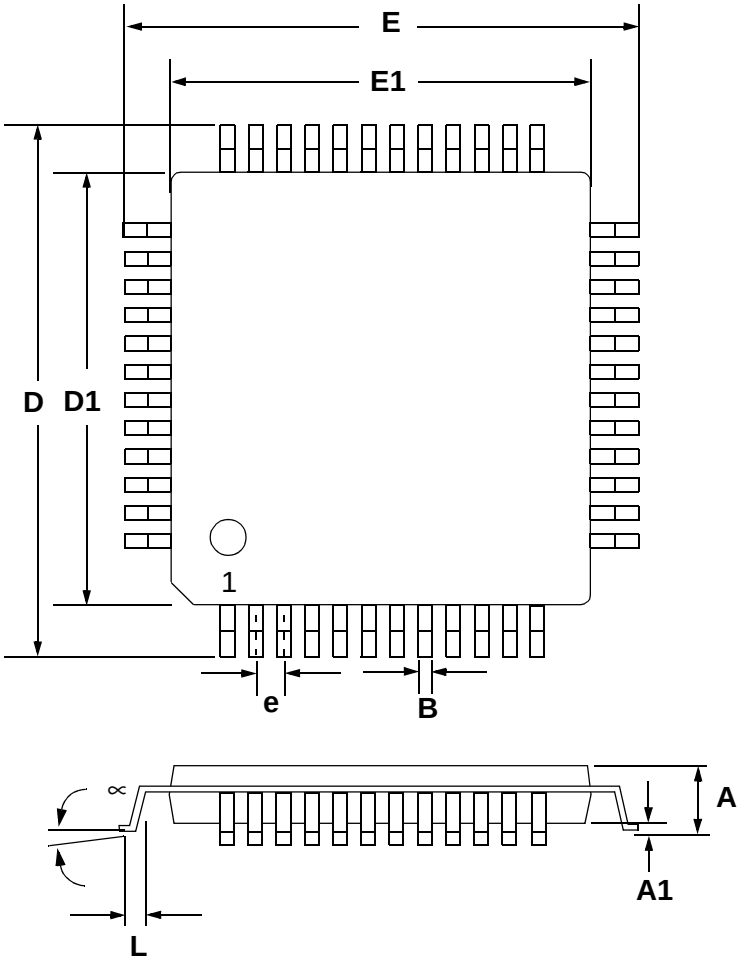
6) Intel®, Audio Codec '97 Component Specification, Revision 2.1, May 1998.
http://developer.intel.com/ial/scalableplatforms/audio/index.htm

7) Microsoft®, PC 99 System Design Guide, Version 1.0, July 1999.
http://www.microsoft.com/hwdev/desguid/

8) Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub, June 1999
http://developer.intel.com/design/chipsets/datashts/290655.htm

15. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

• Notes •


SMART
Analog
™