

**Genesys Logic, Inc.** 

# GL822

## USB 2.0 SD 3.0/MMC/MS Card Reader Controller

**Product Overview** 





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## CHAPTER 1 GENERAL DESCRIPTION

The GL822 is a USB 2.0 SD 3.0 UHS-I Memory Card Reader single chip. It supports USB 2.0 high-speed transmission to Secure Digital<sup>TM</sup> (SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard<sup>TM</sup> (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick<sup>TM</sup> (MS), Memory Stick Duo<sup>TM</sup> (MS Duo), High Speed Memory Stick<sup>TM</sup> (HS MS), Memory Stick PRO<sup>TM</sup> (MS PRO), Memory Stick PRO<sup>TM</sup> Duo (MS PRO Duo), Memory Stick PRO-HG<sup>TM</sup> (MS PRO-HG) and MS PRO Micro on one chip. It also supports next generation huge density memory cards (up to 2TB), such as SDXC and Memory Stick XC. As a single chip solution for USB 2.0 flash card reader, the GL822 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and SD/MMC card interface specification.

The GL822 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Its' pin assignment design fits to card sockets to provide easier PCB layout. Inside the chip, it integrates 5V to 3.3V and 3.3V to 1.8V regulators and power MOSFETs and it enables the function of on-chip clock source (OCCS) which means no external 12MHz XTAL is needed and that effectively reduces the total BOM cost.



## **CHAPTER 2 FEATURES**

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0
  - Comply with USB Storage Class specification rev. 1.0
  - Support one device address and up to four endpoints:
  - Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3)
- Integrated USB building blocks
  - USB 2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR)
- Embedded 8051 micro-controller
  - Embedded mask ROM and internal SRAM
- Secure Digital<sup>TM</sup> (SD)
  - Support SD specification v1.0 / v1.1 / v2.0/ SDHC (Up to 32GB)
  - Support SD specification v3.0 UHS-I: SDR25/SDR50/DDR50/SDR104
  - Support 1.8V/3.3V switch signal pads
  - Support up to 208 MHz clock frequency
  - Support SDXC (Up to 2TB)
- MultiMediaCard<sup>TM</sup> (MMC)
  - Support MMC specification v3.x / v4.0 / v4.1 / v4.2.
- x1/x4/x8 bit data bus Memory Stick<sup>TM</sup> / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG / Memory Stick XC
  - Comply with Memory Stick specification: MS 1.43 / MS PRO 1.05 / MS HG Micro 1.00 / MS PRO-HG Duo 1.03 with 8-bit data bus / MS XC 1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- On chip clock source (OCCS) and no need of 12MHz Crystal Clock input.
- On-Chip 5V to 3.3V and 3.3V to 1.8V regulators
- Support 5V to 3.3V Band Gap Regulator for stable voltage supply
- Provide Over-Current protection mechanism for safety power supply
- On-Chip power MOSFETs for supplying flash media card power
- Support Power Saving mode/ Selective suspend mode for better power management.

Available in QFN-28(A) and LQFP-48 package.

- Support external serial EEPROM interface for the flexibility to load the vendor information and system options. Only available in LQFP-48 package.
- Package available in 28 pin QFN (5x5 mm), 28 pin SSOP (209 mil) and 48 pin LQFP(7x7 mm)

Package Type	Version	Power Source	Power Management
SSOP-28	01, 03, …N	5V	Not support
QFN-28 (A)	01, 03,N	3.3V	Power Saving Mode/ Selective Suspend Mode
QFN-28 (B)	02, 04, …N+1	5V	Not support
LQFP-48	01, 03, …N	5V/3.3V	Power Saving Mode/ Selective Suspend Mode

**Table 2.1 - Product Difference Overview** 



#### CHAPTER 4 BLOCK DIAGRAM



#### **Functional Block Diagram**

#### **OCCS USB PHY**

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

#### SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

#### **EPFIFO**

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3), Bulk In/Out FIFO

- **Control FIFO** FIFO of control endpoint 0. It is 64-byte FIFO and used for endpoint 0 data transfer.
- Interrupt FIFO 64-byte depth FIFO of endpoint 3 for status interrupt
- Bulk In/Out FIFO It can be in the TX mode or RX mode:
  - It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
    It can be directly accessed by micro-controller



#### MCU

8051	micro-controller	inside.
0051	mero controner	monue.

- 8051 Core Compliant with Intel 8051 high speed micro-controller FW code on ROM
- ROM
- SRAM Internal RAM area for MCU access

#### MHE

•	MIF	Media Interface: SD/MMC/MS/MS PRO/MS PRO-HG
•	MCFIFO	It can access by MCU for memory card short data packet.

#### Regulator

• 5V to 3.3V	Band Gap Regulator for stable voltage supply for USB PHY, PMOS.
	When Power source is 3.3V, the 5V to 3.3V regulator will be disabled.
• 3.3V to 1.8V	For core logic and internal memory.

#### **PMOS**

On-Chip power MOSFETs provide Over-Current protection mechanism.