v02.1209

HMC670LC3C

13 Gbps, 1:2 Fanout Buffer

Typical Applications

The HMC670LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Clock Buffering up to 13 GHz

Features

Inputs Terminated Internally in 50 Ohms

Differential Inputs are DC Coupled

Propagation Delay: 55 ps

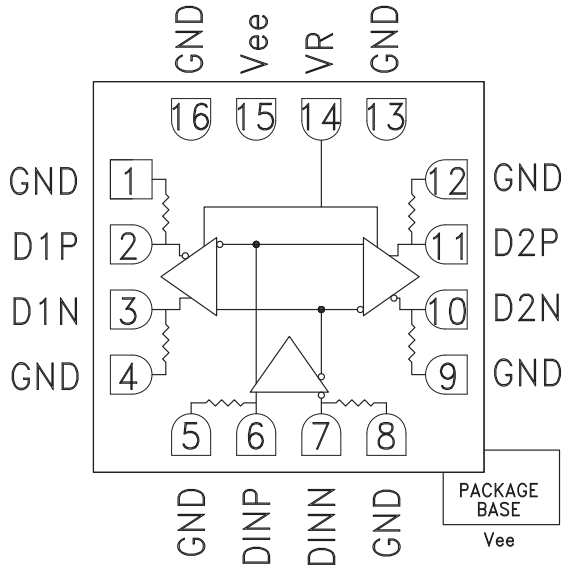
Fast Rise and Fall Times: 24 / 22 ps

Programmable Differential
Output Voltage Swing: 400 - 1100 mV

Power Dissipation: 240 mW

16 Lead Ceramic 3x3mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC670LC3C is a 1:2 Fanout Buffer designed to support data transmission rates up to 13 Gbps, and clock frequencies as high as 13 GHz. All differential inputs and outputs are DC coupled and terminated on chip with 50 Ohm resistors to ground. The outputs may be used in either single-ended or differential modes, and should be AC or DC coupled into 50 Ohm resistors connected to ground.

The HMC670LC3C also features an output level control pin, VR which allows for loss compensation or for signal level optimization. The HMC670LC3C operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant 3x3 mm SMT package.

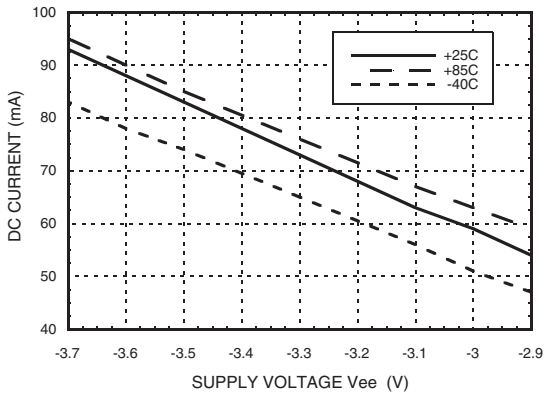
Electrical Specifications, T_A = +25 °C, Vee = -3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			75		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Clock Bandwidth, 3 dB	200 mVpp Input		12.2		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVpp
	Differential, peak-to-peak		1100		mVpp
Output High Voltage			-10		mV
Output Low Voltage			-570		mV

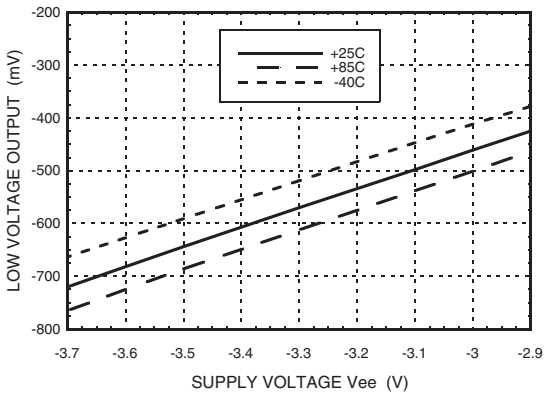
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Rise / Fall Time	Single-Ended, 20% - 80%		24 / 22		ps
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter J_R	rms [1]			0.2	ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [2]		2	6	ps
Propagation Delay, td			55		ps
D1 to D2 Data Skew, t_{SKEW}			0		ps
[1] Upper limit of random jitter, J_R, determined by measuring and integrating output phase noise with a sinusodal input at 5, 10, and 13.5 GHz over temperature.					
[2] Deterministic jitter measured at 5, 10, and 13.5 GHz with a 200 mVpp, 2^{15}-1 PRBS input sequence.					

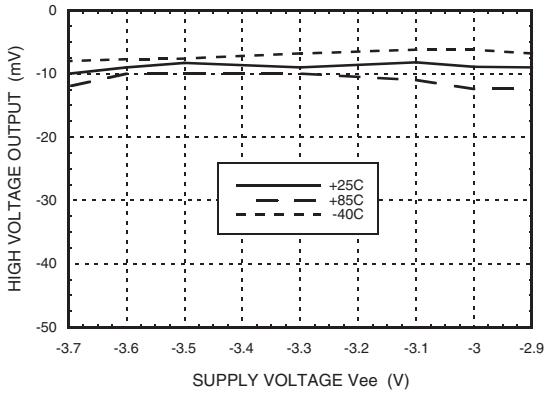
DC Current vs. Supply Voltage [1]



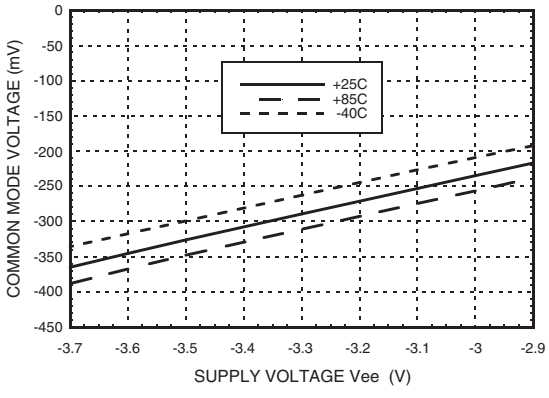
Output Low Voltage vs. Supply Voltage [1] [2]



Output High Voltage vs. Supply Voltage [1] [2]

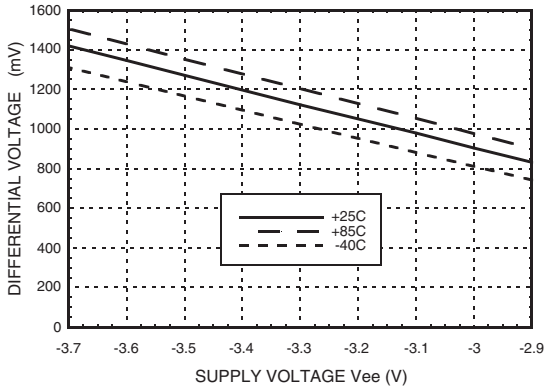


Common Mode Voltage vs. Supply Voltage [1] [2]

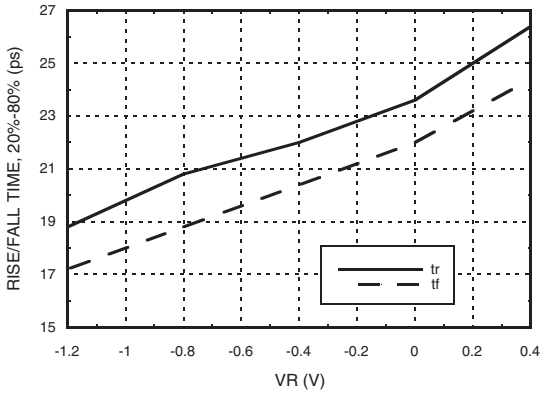


[1] VR = 0.0V [2] Frequency = 1 GHz

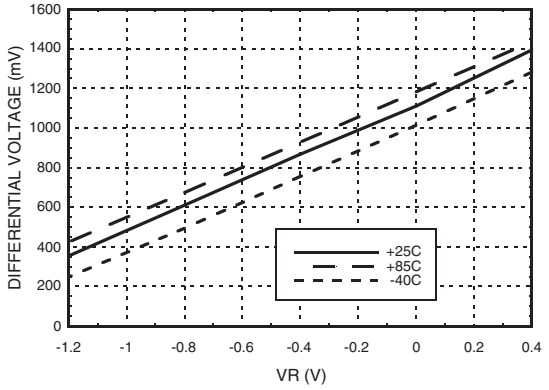
Output Differential vs. Supply Voltage [1] [2]



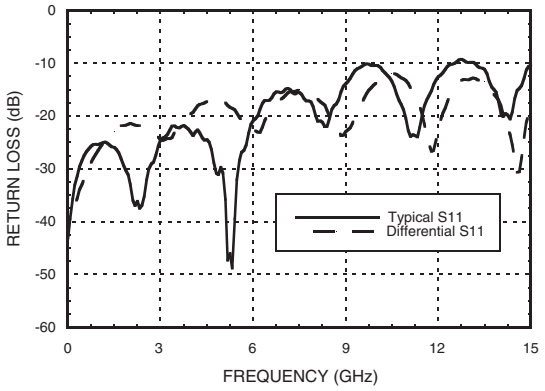
Rise / Fall Time vs. VR [3]



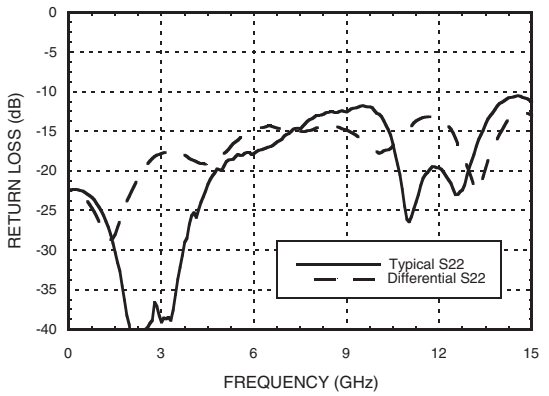
Output Differential vs. VR [2]



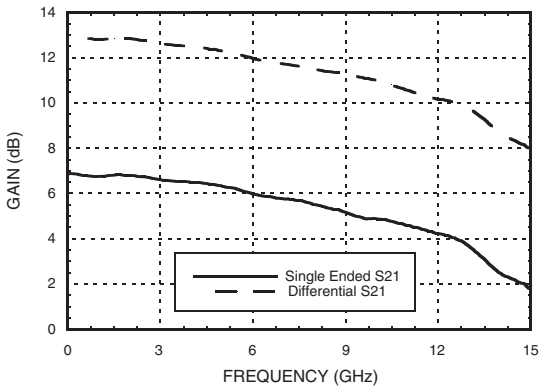
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

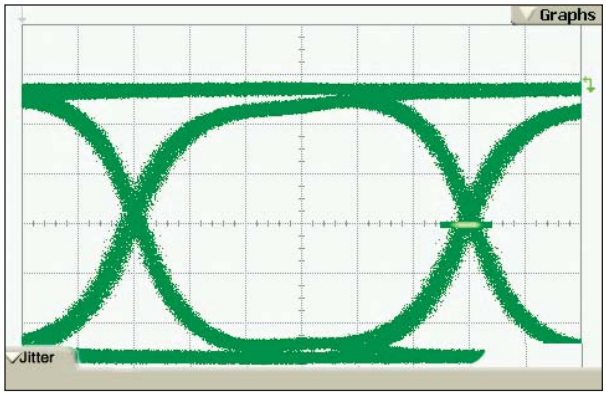


Large Signal Gain @ 25ºC



[1] VR = 0.0V [2] Frequency = 1 GHz [3] Frequency = 5 GHz

Eye Diagram

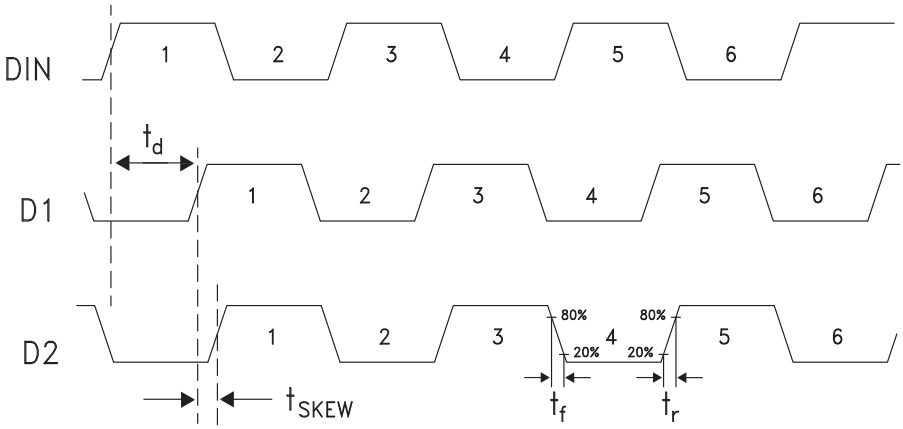


Parameter	Conditions
Bit Rate	10.00000 Gbps
Pattern Length	32767 Bits
DJ (δ-δ)	7.2 ps
Vertical Scale	100 mV / div
Time Scale	16.7 ps / div

[1] Test Conditions:
Pattern generated with an Agilent N4901B Serial BERT
Eye diagram data presented on an Infinium DCA 86100A
Rate = 10.0 GB/s
Pseudo Random Code = 2^{15} -1
Vin = 400 mVpp differential

[2] Vertical Scale = 100 mV/Div

Timing Diagram



Truth Table

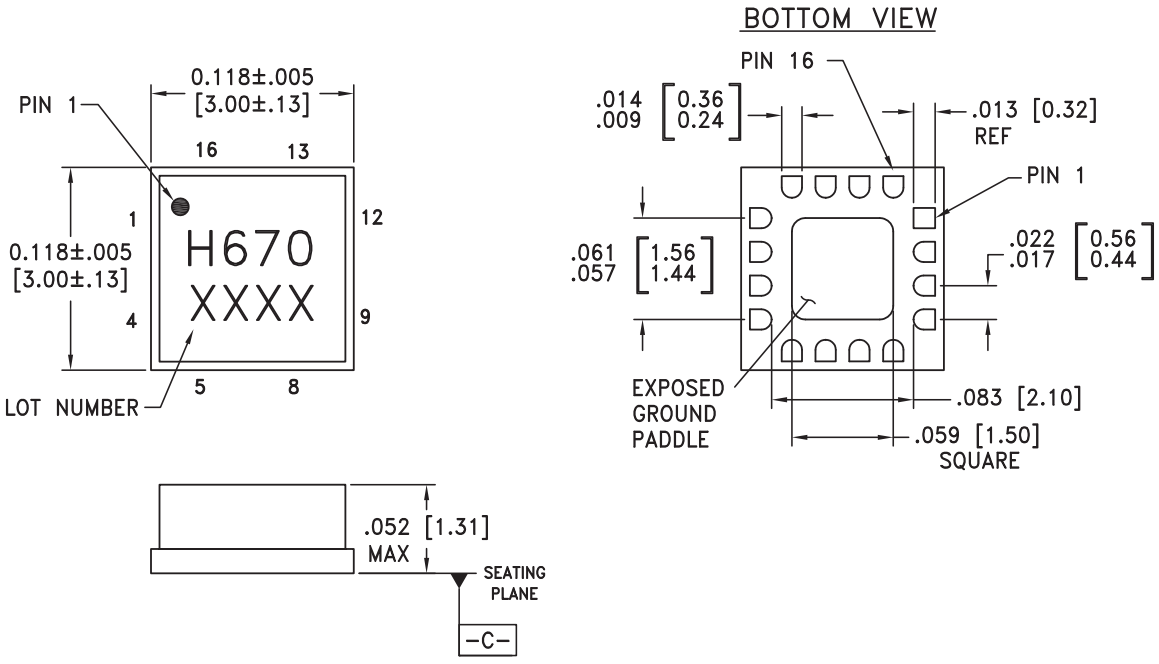
Input	Outputs	
DIN	D1	D2
L	L	L
H	H	H
Notes: DIN = DINP - DINN D1 = D1P - D1N D2 = D2P - D2N	H - Positive differential voltage L - Negative differential voltage	

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +1V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

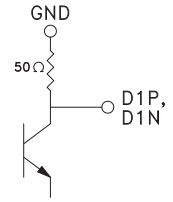
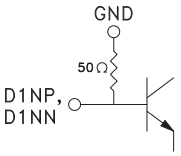
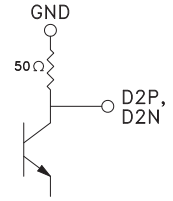
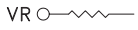
Outline Drawing



NOTES:

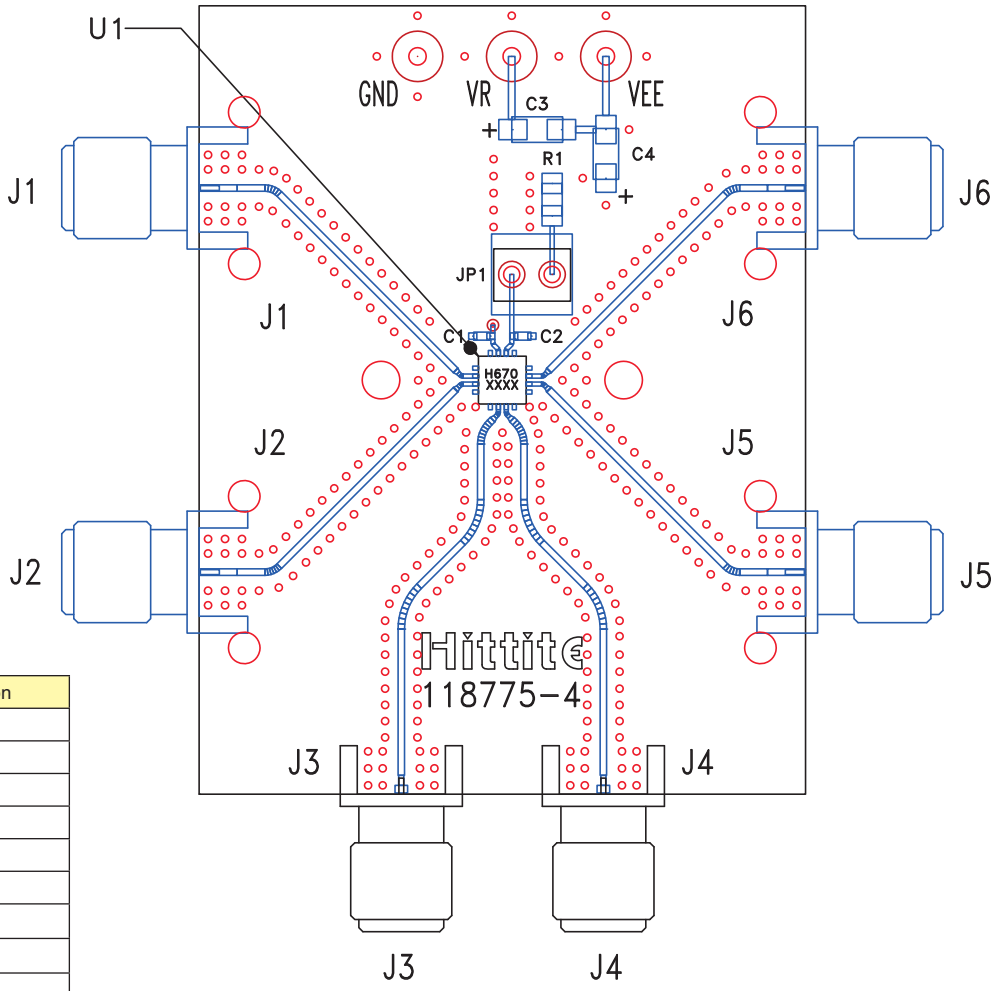
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO Vee.

Pin Descriptions [1]

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	D1P. D1N	Clock / Data Output Port 1	
6, 7	DINP, DINN	Clock / Data Inputs	
10, 11	D2N D2P	Clock / Data Output Port 2	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per “Output Differential vs. VR” plot, or by tying VR to GND with a resistor per the following equation: $V_0(R) = 1.2 / (2.1 + R)$, R in kΩ	
15, Package Base	Vee	Negative Supply	

[1] Contact HMC for alternate pinouts

Evaluation PCB



Item	Description
J1	DO1P
J2	DO1N
J3	DINP
J4	DINN
J5	DO2N
J6	DO2P
J7, J8, J12 - J14	GND
J10	VR
J11	Vee

List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J14	DC Pin
C1 - C3	100 pF Capacitor, 0402 pkg
C4 - C5	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC670LC3C High Speed Logic, Fanout Buffer
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit