OKI

OKI SEMICONDUCTOR

Dear customers,

About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008.　Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008
OKI Semiconductor Co., Ltd.

OKI SEMICONDUCTOR CO., LTD.

550-1 Higashiasakawa-cho, Hachioji-shi, Tokyo 193-8550, Japan

http://www.okisemi.com/en/

OKI Semiconductor

ML6190B

Longwave Time Code RF Receiver LSI

GENERAL DESCRIPTION

The ML6190B receives and detects standard low-frequency radio waves and outputs time codes indicating time and calendar information as digital signals. Using the time codes allows clocks built in various devices to be corrected automatically. The ML6190B is provided with a built-in antenna switch to allow reception of two radio frequencies. A CMOS amplifier circuit, which has extremely high impedance input, can capture antenna output signal voltage effectively, so it can have higher radio wave sensitivity than a bipolar amplifier ciucuit.

Features

- High sensitivity (1.0 µVrms typ.)
- Low supply current (17 µA typ.)
- Low standby current (0.01 µA max.)
- Low voltage drive (V_{DD} = 1.1 V to 3.6 V)
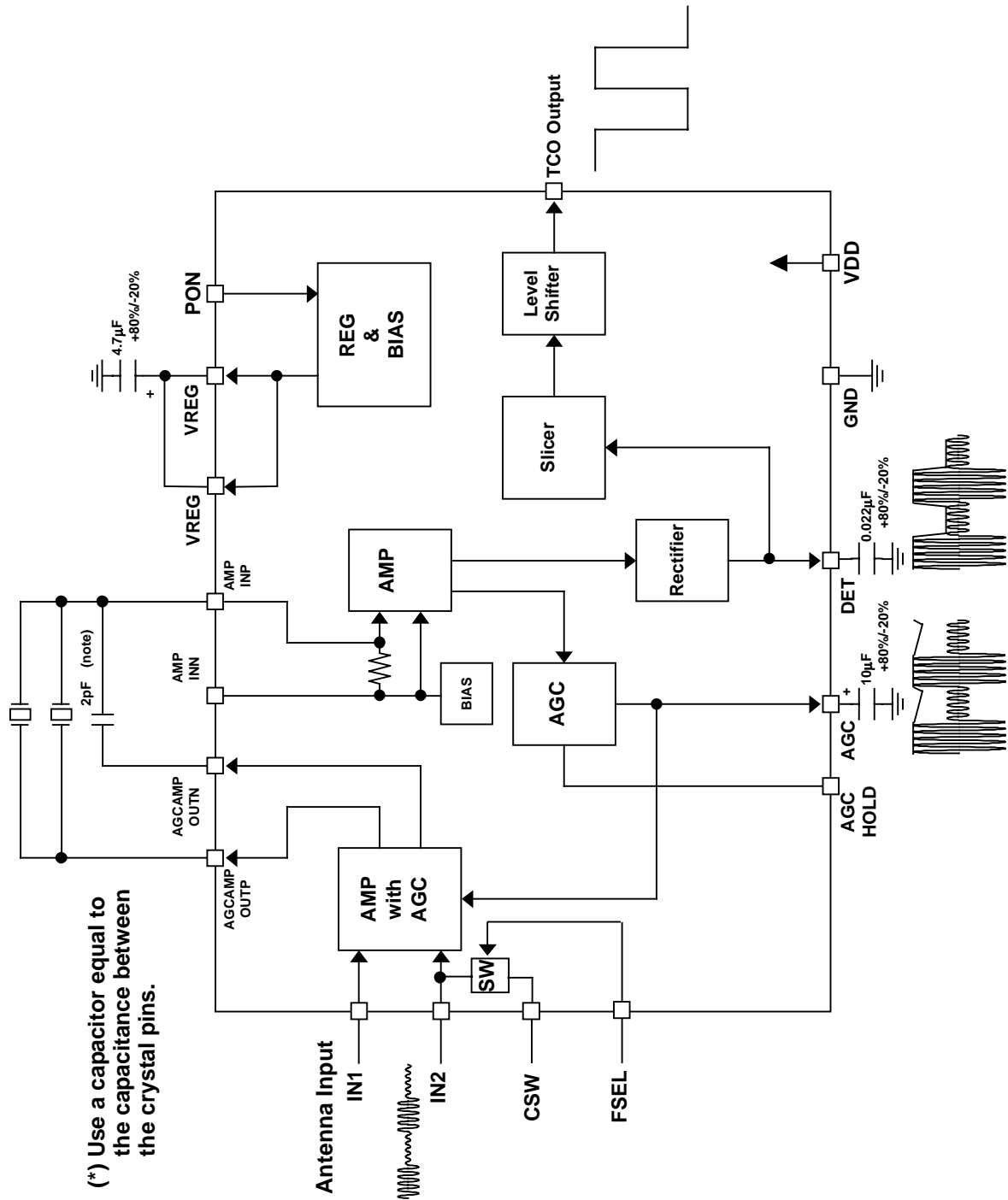- Built-in antenna switch (frequency switching)

Functions
- RF amplifier
- AGC circuit
- Rectifier
- Slicer
- Time code output
- Antenna switch

Package
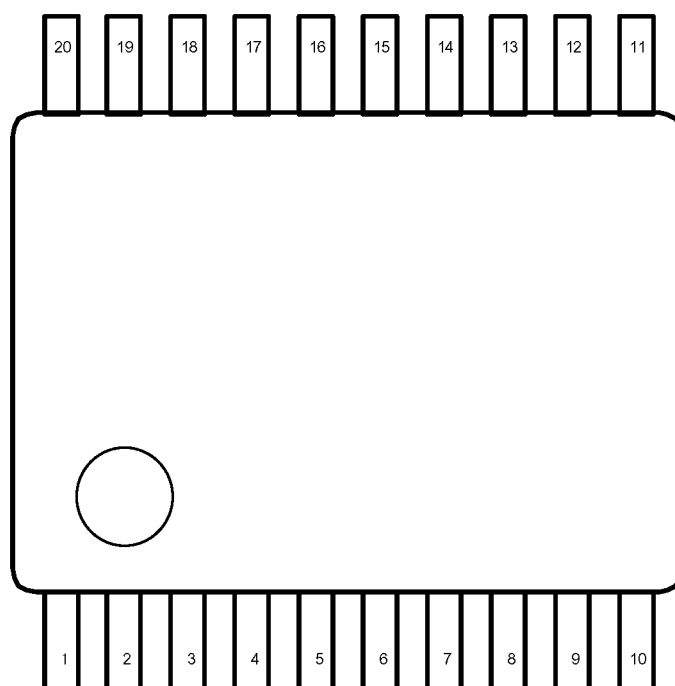20-pin SSOP (SSOP20-P-44-0.65-K) (ML6190BMB)

BLOCK DIAGRAM

(*) Use a capacitor equal to the capacitance between the crystal pins.

PIN SPECIFICATIONS

• Package

20-pin SSOP (0.65 mm pitch)

• Pin configuration

Pin	Symbol	Function	Pin	Symbol	Function
1	VREG	Regulator output pin	11	AMPINP	AMP input pin
2	VDD	External power supply pin	12	AMPINN	AMP input pin
3	GND	Ground pin	13	AGCAMPOUTN	AGCAMP output pin
4	FSEL	Antenna switch control pin	14	AGCAMPOUTP	AGCAMP output pin
5	PON	Power-on input pin	15	GND	Ground pin
6	TCO	Time code output pin	16	VREG	Regulator output pin
7	AGC_HOLD	AGC hold input pin	17	GND	Ground pin
8	AGC	AGC pin for external capacitor	18	CSW	Antenna input pin
9	DET	DET pin for external capacitor	19	IN2	Antenna input pin
10	GND	Ground pin	20	IN1	Antenna input pin

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• Pin descriptions

Pin	Symbol	I/O	Description
1	VREG	—	Regulator output pin Connect a 4.7 μF capacitor between this pin and the GND pin. Either polar or non-polar capacitors can be used. When using polar capacitors, connect them as shown in the block diagram. This pin is connected to pin 16 internally but should also be connected externally.
2	VDD	—	External power supply pin
3	GND	—	Ground pin
4	FSEL	I	Antenna switch control pin
5	PON	O	Power-on input pin "H": Normal operation "L": Standby operation
6	TCO	I	Time code output pin The "H" output for the large amplitude signal, the "L" output for the small amplitude signal, and "H" output in the standby state.
7	AGC_HOLD	—	AGC hold input pin "H": AGC operation "L": AGC hold operation
8	AGC	—	AGC pin for an external capacitor Connect a 10 μF capacitor between this pin and the GND pin. Either polar or non-polar capacitors can be used. When using polar capacitors, connect them as shown in the block diagram.
9	DET		DET pin for an external capacitor Connect a 0.022μF capacitor between this pin and the GND pin.
10	GND	—	Ground pin
11	AMPINP	I	AMP input pin
12	AMPINN	I	AMP input pin Leave this pin open.
13	AGCAMPOUTN	O	Output pin for AMP with AGC
14	AGCAMPOUTP	O	Output pin for AMP with AGC
15	GND	—	Ground pin
16	VREG	—	Regulator output pin This pin is connected to pin 1 internally but should also be connected externally.
17	GND	—	Ground pin
18	CSW	I	Antenna input pin
19	IN2	I	Antenna input pin
20	IN1	I	Antenna input pin

RADIO WAVE RECEIVING IC SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{DD}	Ta = 25°C	−0.3 to +3.8	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Operating temperature*	Top	—	−40 to +85	°C
Storage temperature	T_{STG}	—	−55 to +125	°C

*: The temperature that does not cause permanent damage to the device (Performance may not be guaranteed)

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Operating voltage	V_{DD}	—	1.1 to 3.6	V
Operating temperature	T_{OP}	—	−25 to +85	°C

Electrical Characteristics

VDD = 1.5 V, GND = 0 V, Ta = 25 °C, f_{IN} = 60 kHz, and modulation factor = 90 %, unless otherwise specified.

• DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	—	—	17	38	µA
Standby current	I_{STB}	—	—	—	0.01	µA

• AC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage sensitivity	V_{INmin}	—	—	1.0	—	µVrms
Maximum signal input	V_{INmax}	—	100	—	—	mVrms
Input resistance	R_{in}	Between IN1 and IN2 pins	2	—	—	MΩ
		Between AMPINP and AMPINN pins		500		kΩ
Input capacitance	C_{in}	—	—	—	5	pF
Receiving frequency	f_{IN}	—	40	—	100	kHz

• TCO output characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage (high)	V_{OH}	—	V_{DD}−0.1	—	—	V
Output voltage (low)	V_{OL}	—	—	—	0.1	V
Output short current (high)	I_{OH}	V_{DD} = 3.6 V V_O = 0 V	—	−36	—	µA
Output short current (low)	I_{OL}	V_{DD} = 3.6 V V_O = 3.6 V	—	36	—	µA
Output pulse width (500 ms input)	T_{500}	—	400	500	600	ms
Output pulse width (800 ms input)	T_{800}	—	700	800	900	ms
Output pulse width (200 ms input)	T_{200}	—	100	200	300	ms

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• AGC hold characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AGC_HOLD "H" input voltage	V_{IHAH}	During normal operation	$0.9*V_{DD}$	—	—	V
AGC_HOLD "L" input voltage	V_{ILAH}	During AGC hold	—	—	$0.1*V_{DD}$	V
AGC_HOLD "H" input current	$|I_{IHAH}|$	VI = V_{DD}	—	0.01	—	μA
AGC_HOLD "L" input current	$|I_{ILAH}|$	VI = 0.0V	—	0.01	—	μA

• PON characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PON "H" input voltage	V_{IHPON}	During normal operation	$0.9*V_{DD}$	—	—	V
PON "L" input voltage	V_{ILPON}	During standby mode	—	—	$0.1*V_{DD}$	V
PON "H" input current	$|I_{IHPON}|$	VI = V_{DD}	—	0.01	—	μA
PON "L" input current	$|I_{ILPON}|$	VI = 0.0V	—	0.01	—	μA

• FSEL characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FSEL "H" input voltage	V_{IHFSEL}	Antenna switch ON	$0.9*V_{DD}$	—	—	V
FSEL "L" input voltage	V_{ILFSEL}	Antenna switch OFF	—	—	$0.1*V_{DD}$	V
FSEL "H" input current	$|I_{IHFSEL}|$	VI = V_{DD}	—	0.01	—	μA
FSEL "L" input current	$|I_{ILFSEL}|$	VI = 0.0V	—	0.01	—	μA
Switching ON resistance	R_{SWH}	HSEL = "H"	350	—	—	kΩ
Switching OFF resistance	R_{SWL}	FSEL = "L"	—	20	100	Ω

• Delay characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AGC setup time	T_{AGC}	At the time of PON	—	3	—	sec
Response delay	T_{TCO}	Phase delay relative to input signal	—	50	—	ms

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## DESCRIPTION OF EACH BLOCK

(1) AMP Block

Radio waves received by the antenna will be amplified by AMP with AGC. Signals output from AMP with AGC will go through an external quartz resonator, which serves as a band-pass filter, and will be amplified again at AMP.
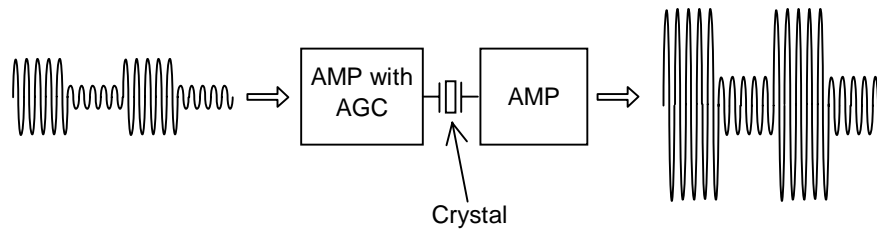
(2) AGC Block

Output signals from AMP will be input to the AGC block and the rectifier block. After signals are input to the AGC block, their high side peak amplitudes are detected. As AGC signals, they will be fed back to AMP with AGC.

The AGC block has the AGC hold function. When the AGC hold signal is "H," the block performs the regular AGC operation. The AGC block performs the AGC hold operation when the AGC hold signal is "L."
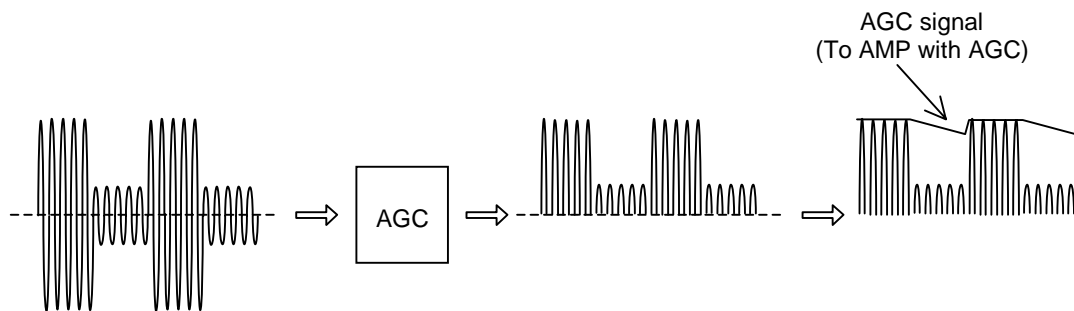
(3) Rectifier Block

After signals are input to the rectifier block, their high side peak amplitudes are detected. As DET signals, they will be transferred to the slicer block.
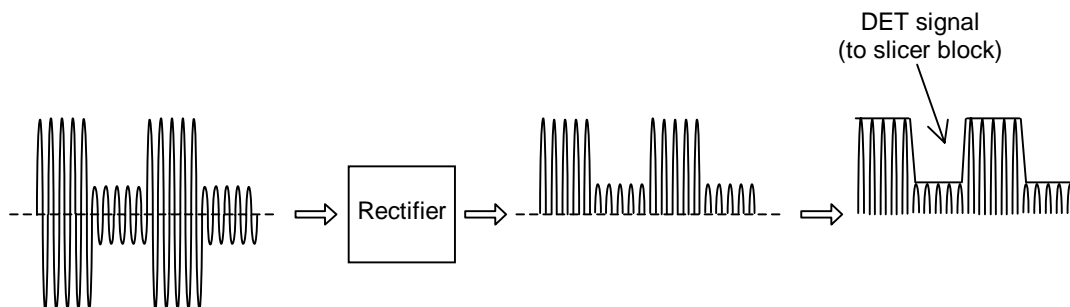
(4) Slicer Block

Signals output from the rectifier block are input to the slicer block and will be shaped to V_{DD} as "1" and GND as "0". Then, these outputs will be output as time codes (TCO).

This LSI has the standby function. When the PON signal is "H," the LSI will perform the regular operation. When the PON signal is "L," the LSI will be in standby state. The TCO during the standby state is "H."
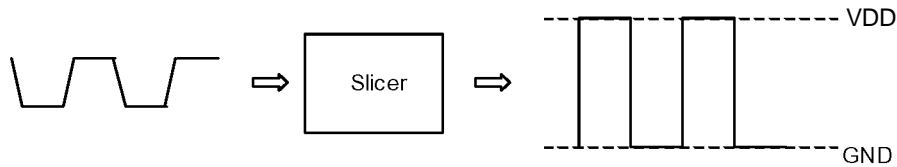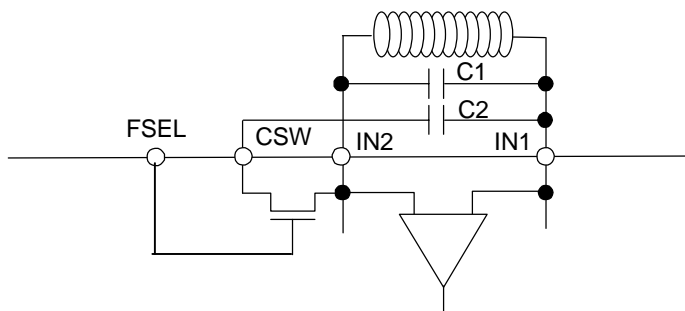

(5) Time Code Output

The time code output (TCO) of the ML6190B is in phase with actual time codes input from the antenna. A "H" level is output for the large amplitude signal and a "L" level is output for the small amplitude signal.

Antenna Input Signal   Time Code Output (TCO)
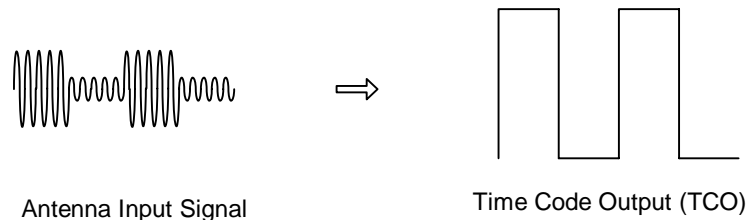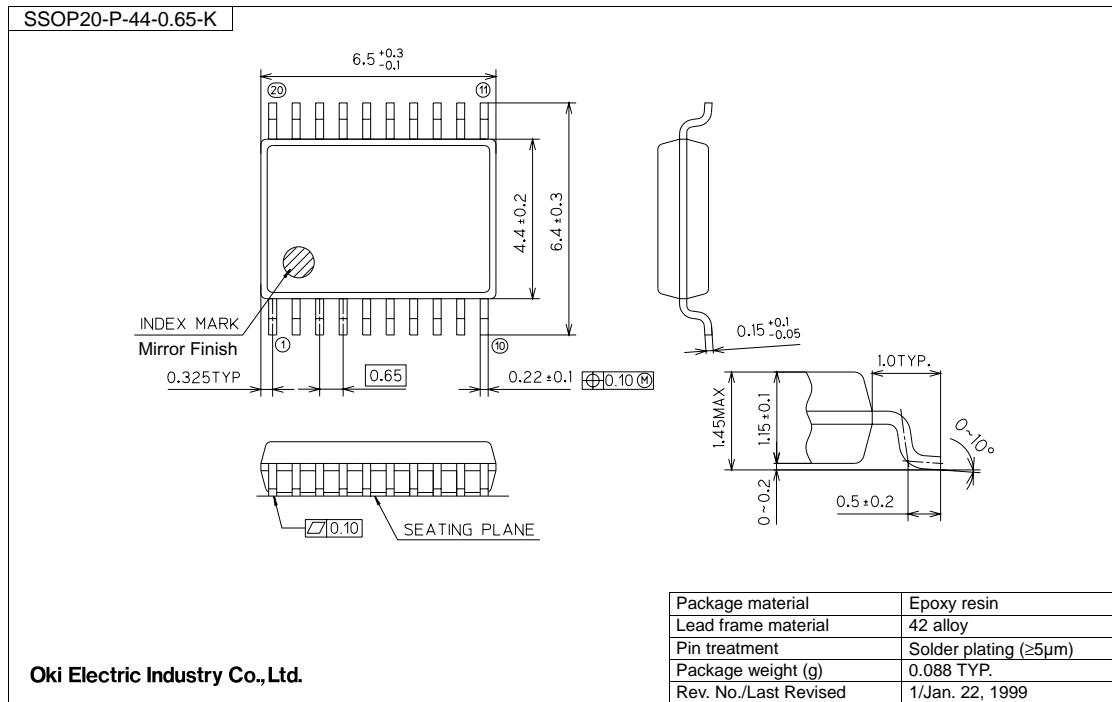
(6) Connecting the Antenna

The ML6190B has a built-in antenna switch to allow reception of two receive frequencies. When receiving only one frequency, connect both the antenna and C1 across IN1 and IN2. When receiving two frequencies, add C2 across CSW and IN1 to enable frequency switching.

40 kHz/60 kHz Antenna Connection Example

PACKAGE DIMENSIONS

(Unit: mm)

SSOP20-P-44-0.65-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.088 TYP.
Rev. No./Last Revised	1/Jan. 22, 1999

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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REVISION HISTORY

Document No.	Date	Page Previous Edition	Current Edition	Description
PEDL6190B-01	Jan. 7, 2005	–	–	Preliminary edition 1
FEDL6190B-01	Mar. 3, 2005	–	–	Final edition 1
		1	1	Modified contents in the "GENERAL DESCRIPTION" Section.
		2	2	Modified the block diagram and eliminated "Note".
		4	4	Partially added contents of the descriptions of Pins 1, 8, and 16.
		5, 6	5, 6	Partially changed contents in the "Electrical characteristics" Section.

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