Low Voltage, 2.5V and 3.3V LVCMOS PLL Clock Driver

MPC9600

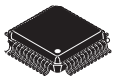
NRND

DATASHEET

NRND – Not Recommend for New Designs

The MPC9600 is a low voltage 2.5 V or 3.3 V compatible, 1:21 PLL based clock driver and fanout buffer. With output frequencies up to 200 MHz and output skews of 150 ps, the device meets the needs of the most demanding clock tree applications.

3.3 V OR 2.5 V
LOW VOLTAGE CMOS
PLL CLOCK DRIVER



AE SUFFIX
48-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 932-03

Features

- Multiplication of Input Frequency by 2, 3, 4, and 6
- Distribution of Output Frequency to 21 Outputs Organized in Three Output Banks: QA0-QA6, QB0-QB6, QC0-QC6, Each Fully Selectable
- Fully Integrated PLL
- Selectable Output Frequency Range Is 50 to 100 MHz and 100 to 200 MHz
- Selectable Input Frequency Range Is 16.67 to 33 MHz and 25 to 50 MHz
- LVCMOS Outputs
- Outputs Disable to High Impedance (Except QFB)
- LVCMOS or LVPECL Reference Clock Options
- 48-Lead QFP Packaging, Pb-Free
- ± 50 ps Cycle-to-Cycle Jitter
- 150 ps Maximum Output-to-Output Skew
- 200 ps Maximum Static Phase Offset Window
- **NRND – Not Recommend for New Designs**

Functional Description

The MPC9600 is a fully LVCMOS 2.5 V or 3.3 V compatible PLL clock driver. The MPC9600 has the capability to generate clock signals of 50 to 200 MHz from clock sources of 16.67 to 50 MHz. The internal PLL is optimized for this frequency range and does not require external loop filter components. QFB provides an output for the external feedback path to the feedback input FB_IN. The QFB divider ratio is configurable and determines the PLL frequency multiplication factor when QFB is directly connected to FB_IN. The MPC9600 is optimized for minimizing the propagation delay between the clock input and FB_IN.

Three output banks of 7 outputs each bank can be individually configured to divide the VCO frequency by 2 or by 4. Combining the feedback and output divider ratios, the MPC9600 is capable to multiply the input frequency by 2, 3, 4, and 6.

The reference clock is selectable either LVPECL or LVCMOS. The LVPECL reference clock feature allows the designer to use LVPECL fanout buffers for the inner branches of the clock distribution tree. All control inputs accept LVCMOS compatible levels. The outputs provide low impedance LVCMOS outputs capable of driving parallel terminated 50 Ω transmission to $V_{TT} = V_{CC}/2$. For series terminated lines the MPC9600 can drive two lines per output giving the device an effective total fanout of 1:42. With guaranteed maximum output-to-output skew of 150 ps, the MPC9600 PLL clock driver meets the synchronization requirements of the most demanding systems.

The V_{CCA} analog power pin doubles as a PLL bypass select line for test purpose. When the V_{CCA} is driven to GND the reference clock will bypass the PLL.

The device is packaged in a 48-lead LQFP package to provide optimum combination of board density and performance.

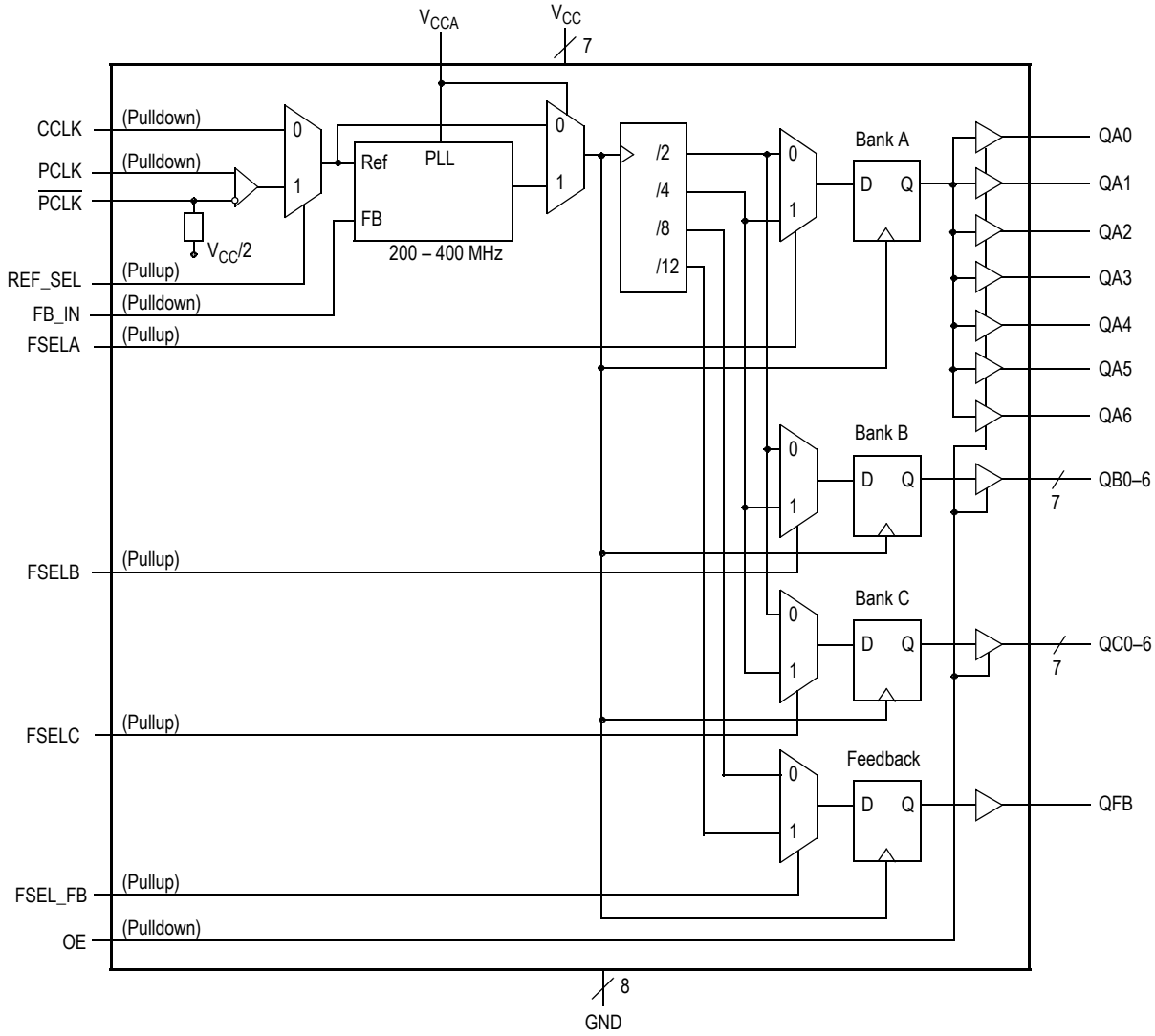


Figure 1. MPC9600 Logic Diagram

Table 1. Pin Configuration – 48 LQFP

Pin	I/O	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	PECL	Differential reference clock frequency input
CCLK	Input	LVCMOS	Reference clock input
FB_IN	Input	LVCMOS	PLL feedback clock input
QAn	Output	LVCMOS	Bank A outputs
QBn	Output	LVCMOS	Bank B outputs
QCn	Output	LVCMOS	Bank C outputs
QFB	Output	LVCMOS	Differential feedback output
REF_SEL	Input	LVCMOS	Reference clock input select
FSELA	Input	LVCMOS	Selection of bank A output frequency
FSELB	Input	LVCMOS	Selection of bank B output frequency
FSELC	Input	LVCMOS	Selection of bank C output frequency
FSEL_FB	Input	LVCMOS	Selection of feedback frequency
OE	Input	LVCMOS	Output enable
V_{CCA}		Power supply	Analog power supply and PLL bypass. An external V_{CC} filter is recommended for V_{CCA}
V_{CC}		Power supply	Core power supply
GND		Ground	Ground

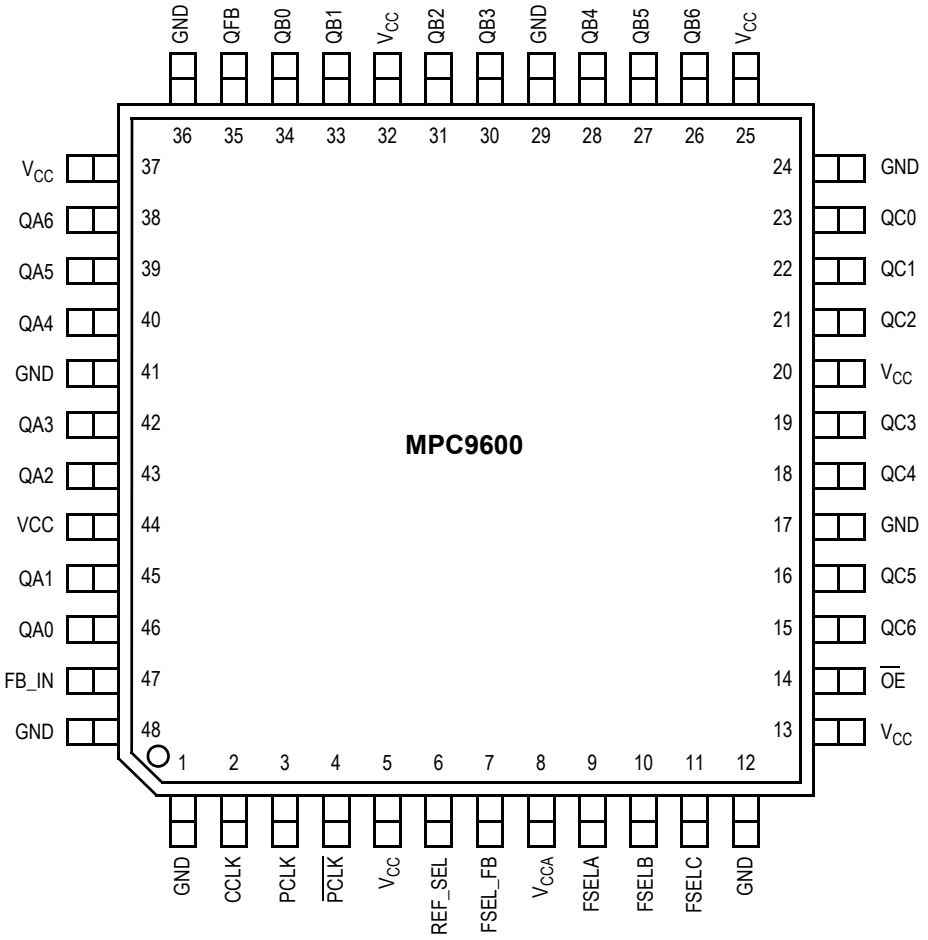


Figure 2. 48-Lead Package Pinout (Top View)

Table 2. Function Table (Controls)

Control Pin	0	1
REF_SEL	CCLK	PCLK
V_{CCA}	PLL Bypass(1)	PLL Power
OE	Outputs Enabled	Outputs Disabled (except QFB)
FSELA	Output Bank A at VCO/2	Output Bank A at VCO/4
FSELB	Output Bank B at VCO/2	Output Bank B at VCO/4
FSELC	Output Bank C at VCO/2	Output Bank C at VCO/4
FSEL_FB	Feedback Output at VCO/8	Feedback Output at VCO/12

1. V_{CCA} = GND, PLL off and bypassed for static test and diagnosis.

Table 3. Absolute Maximum Ratings(1)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_{Stor}	Storage Temperature Range	–65	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	400			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	1500			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = – 40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage (DC)	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}(1)	Common Mode Range (DC)	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA(2)
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance			14 – 17		W	
I_{IN}	Input Leakage Current				± 150	µA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = – 40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.7	V	LVCMOS
V_{PP}	Peak-to-Peak input voltage (DC)	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}(1)	Common Mode Range (DC)	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA(2)
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance			17 – 20		W	
I_{IN}	Input Leakage Current				± 150	µA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 7. AC Characteristics – 48 LQFP (V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, T_A = –40°C to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency					
	÷ 8 feedback (FSEL_FB = 0)	25		50	MHz	PLL locked
	÷ 12 feedback (FSEL_FB = 1)	16.67		33	MHz	PLL locked
	Static test mode (V_{CCA} = GND)	0		500	MHz	V_{CCA} = GND
f_{VCO}	VCO Frequency	200		400	MHz	
f_{MAX}	Maximum Output Frequency					
	÷ 2 outputs (FSELx = 0)	100		200	MHz	PLL locked
	÷ 4 outputs (FSELx = 1)	50		100	MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range					
	PCLK, $\overline{PCLK}$ (V_{CC} = 3.3 V ± 5%)	1.2		V_{CC} –0.8	V	LVPECL
	PCLK, $\overline{PCLK}$ (V_{CC} = 2.5 V ± 5%)	1.2		V_{CC} –0.6	V	LVPECL
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	see Figure 11
$t_{(\varnothing)}$	Propagation Delay (static phase offset)					
	CCLK to FB_IN	–60	+40	+140	ps	PLL locked
	PECL_CLK to FB_IN	+30	+130	+230	ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew					
	all outputs, single frequency		70	150	ps	Measured at coincident rising edge
	all outputs, multiple frequency		70	150	ps	
	within QAx output bank		30	75	ps	
	within QBx outputs		40	125	ps	
	within QCx outputs		30	75	ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	see Figure 11
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
BW	PLL Closed Loop Bandwidth					–3 dB point of PLL transfer characteristic
	÷ 8 feedback (FSEL_FB=0)		1.0 – 10		MHz	
	÷ 12 feedback (FSEL_FB=1)		0.6 – 4.0		MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[3]					Refer to application section for other configurations
	All outputs in ÷ 2 configuration					
	All outputs in ÷ 4 configuration		40	130	ps	
			40	180	ps	
$t_{JIT(PER)}$	Period Jitter[3]					Refer to application section for other configurations
	All outputs in ÷ 2 configuration		25	70	ps	
	All outputs in ÷ 4 configuration		20	100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter (1 σ)					RMS value at f_{VCO} = 400 MHz
	V_{CC} = 3.3 V			17[4]	ps	
	V_{CC} = 2.5 V			15[3]	ps	
t_{LOCK}	Maximum PLL Lock Time			5.0	ms	

1. AC characteristics are applicable over the entire ambient temperature and supply voltage range and are production tested. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
3. Cycle-to-cycle and period jitter depends on output divider configuration.
4. See Applications Information section for max I/O phase jitter versus frequency.

APPLICATIONS INFORMATION

Programming the MPC9600

The MPC9600 clock driver outputs can be configured into several divider modes. Additionally the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The selectable feedback divider of the three output groups allows the user to configure the device for 1:2, 1:3, 1:4 and 1:6 input:output frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 8 illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The feedback divider division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 50 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 8. Output Frequency Relationship(1) for QFB Connected to FB_IN

Configuration Inputs				Input Frequency Range CLK [MHz]	Output Frequency Ratio and Range		
FSEL_FB	FSELA	FSELB	FSELC		Ratio, QAx [MHz]	Ratio, QBx [MHz]	Ratio, QCx [MHz]
0	0	0	0	25.0–50.0	4•CLK (100–200)	4•CLK (100–200)	4•CLK (100–200)
0	0	0	1		4•CLK (100–200)	4•CLK (100–200)	2•CLK (50.0–100)
0	0	1	0		4•CLK (100–200)	2•CLK (50.0–100)	4•CLK (100–200)
0	0	1	1		4•CLK (100–200)	2•CLK (50.0–100)	2•CLK (50.0–100)
0	1	0	0		2•CLK (50.0–100)	4•CLK (100–200)	4•CLK (100–200)
0	1	0	1		2•CLK (50.0–100)	4•CLK (100–200)	2•CLK (50.0–100)
0	1	1	0		2•CLK (50.0–100)	2•CLK (50.0–100)	4•CLK (100–200)
0	1	1	1		2•CLK (50.0–100)	2•CLK (50.0–100)	2•CLK (50.0–100)
1	0	0	0	16.67–33.33	6•CLK (100–200)	6•CLK (100–200)	6•CLK (100–200)
1	0	0	1		6•CLK (100–200)	6•CLK (100–200)	3•CLK (50.0–100)
1	0	1	0		6•CLK (100–200)	3•CLK (50.0–100)	6•CLK (100–200)
1	0	1	1		6•CLK (100–200)	3•CLK (50.0–100)	3•CLK (50.0–100)
1	1	0	0		3•CLK (50.0–100)	6•CLK (100–200)	6•CLK (100–200)
1	1	0	1		3•CLK (50.0–100)	6•CLK (100–200)	3•CLK (50.0–100)
1	1	1	0		3•CLK (50.0–100)	3•CLK (50.0–100)	6•CLK (100–200)
1	1	1	1		3•CLK (50.0–100)	3•CLK (50.0–100)	3•CLK (50.0–100)

1. Output frequency relationship with respect to input reference frequency CLK. The VCO frequency range is always 200–400.

Table 9. Typical and Maximum Period Jitter Specification

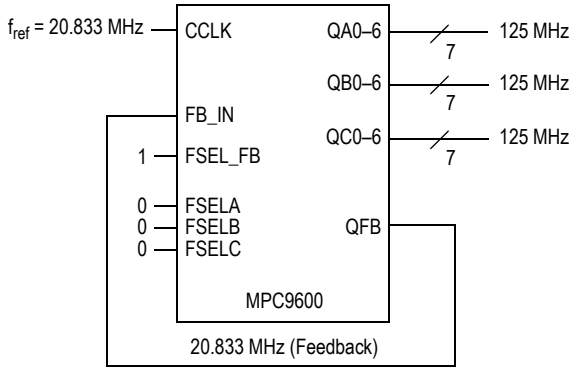
Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration(1)						
÷ 2 (FSELA = 0 and FESLB = 0 and FSELC = 0)	25	50	50	70	25	50
÷ 4 (FSELA = 1 and FESLB = 1 and FSELC = 1)	20	70	50	100	20	70
Mixed ÷ 2/÷ 4 divider configurations(2)						
for output banks in ÷ 2 divider configurations	80	130	100	150	80	130
for output banks in ÷ 4 divider configurations	25	70	60	100	25	70

1. In this configuration, all MPC9600 outputs generate the same clock frequency. See Figure 3 for an example configuration.
2. Multiple frequency generation. Jitter data are specified for each output divider separately. See Figure 7 for an example.

Table 10. Typical and Maximum Cycle-to-Cycle Jitter Specification

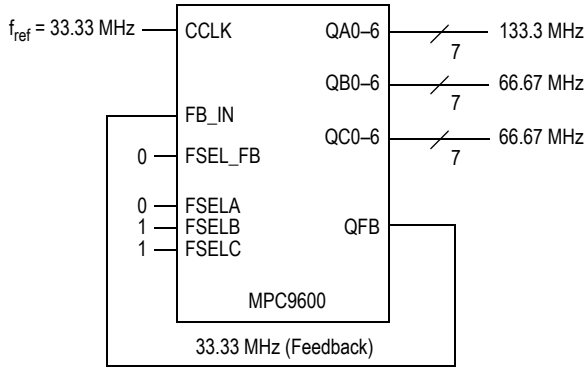
Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration(1)						
÷ 2 (FSELA = 0 and FESLB = 0 and FSELC = 0)	40	90	80	130	40	90
÷ 4 (FSELA = 1 and FESLB = 1 and FSELC = 1)	40	110	120	180	40	110
Mixed ÷2/÷ 4 divider configurations(2)						
for output banks in ÷ 2 divider configurations	150	250	200	280	150	250
for output banks in ÷ 4 divider configurations	30	110	120	180	30	110

1. In this configuration, all MPC9600 outputs generate the same clock frequency.
2. Multiple frequency generation. Jitter data are specified for each output divider separately.



Frequency Range	Min	Max
Input	16.67 MHz	33.33 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Figure 3. Configuration for 126 MHz Clocks



Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Figure 4. Configuration for 133.3/66.67 MHz Clocks

Power Supply Filtering

The MPC9600 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9600 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9600. Figure 5 illustrates a typical power supply filter scheme. The MPC9600 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 5, must have a resistance of 9–10 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria.

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 5, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

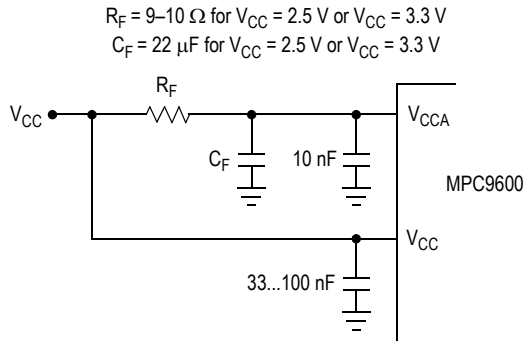


Figure 5. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9600 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9600 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9600. For these applications the MPC9600 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Freescale Semiconductor MC100ES6111 or MC100ES6226, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9600 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9600 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9600 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$) relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9600 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (CCLK or PCLK) of two or more MPC9600 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

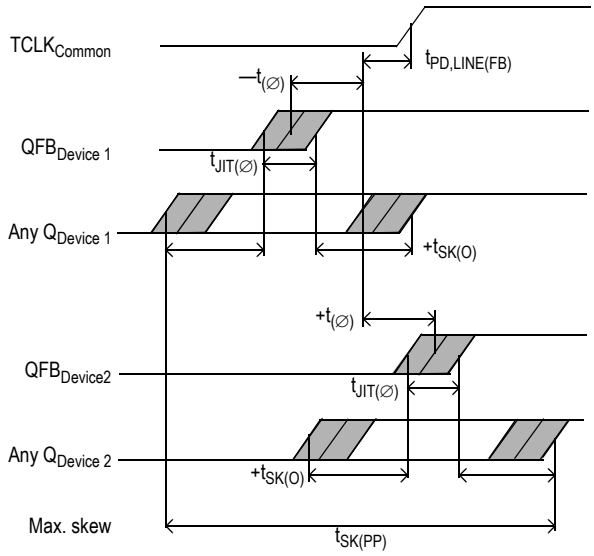


Figure 6. MPC9600 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11. Confidence Factor CF

CF	Probability of Clock Edge Within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –261 ps to 341 ps relative to CCLK (V_{CC} = 3.3 V and f_{VCO} = 200 MHz):

$t_{SK(PP)}$ = [–60 ps...140 ps] + [–150 ps...150 ps] + [(17 ps @ –3)...(17 ps @ 3)] + $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = [–261 ps...341 ps] + $t_{PD, LINE(FB)}$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9600). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 7 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

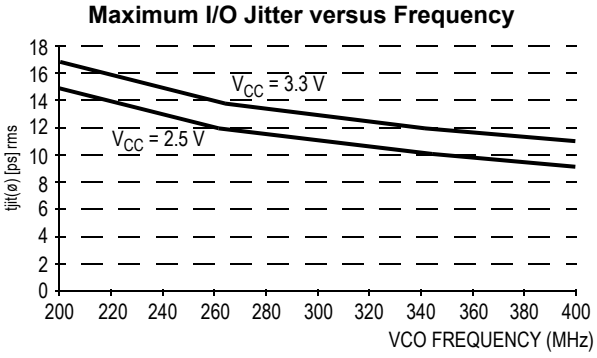


Figure 7. I/O Jitter versus VCO Frequency for V_{CC} = 2.5 V and V_{CC} = 3.3 V

Driving Transmission Lines

The MPC9600 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale Semiconductor application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC} ÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9600 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9600 clock driver is effectively doubled due to its capability to drive multiple lines.

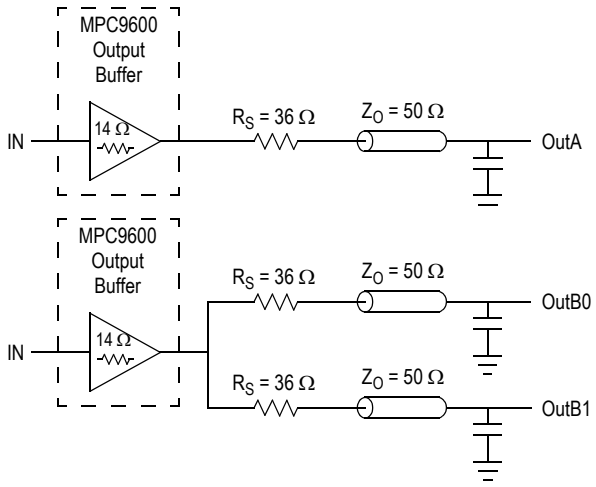


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 shows the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9600 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9600. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_0 = 14\ \Omega$

$V_L = 3.0 (25 \div (18 + 17 + 25)$

$= 1.31$ V

At the load end the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

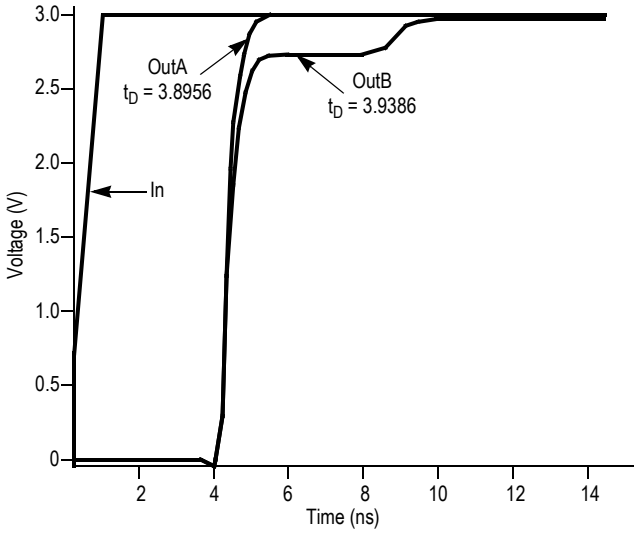
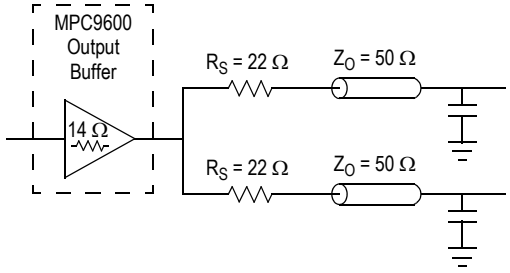


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 10. Optimized Dual Line Termination

The following figures illustrate the measurement reference for the MPC9600 clock driver circuit.

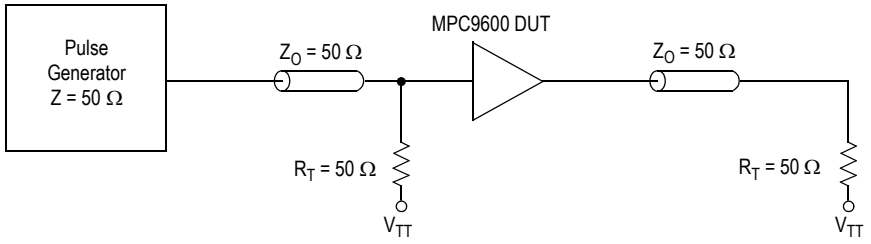


Figure 11. CCLK MPC9600 AC Test Reference

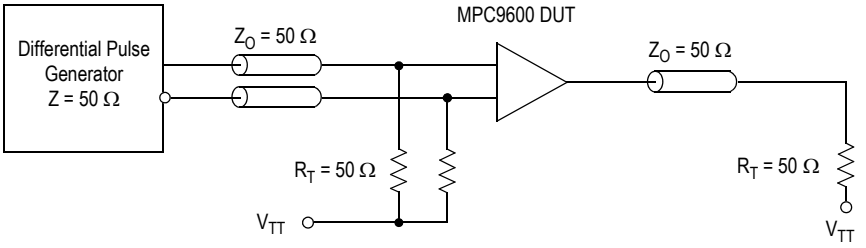


Figure 12. PCLK MPC9600 AC Test Reference

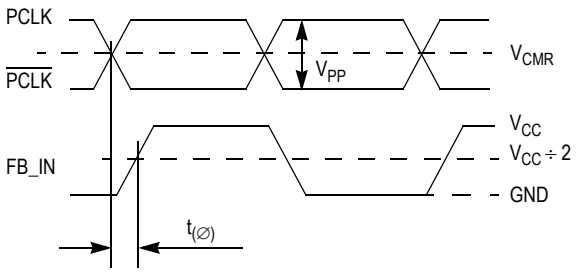


Figure 14. Propagation Delay ($t_{Ø}$, status phase offset) Test Reference

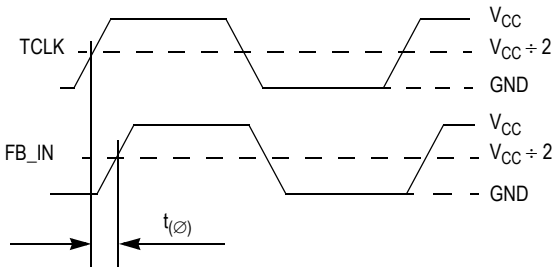
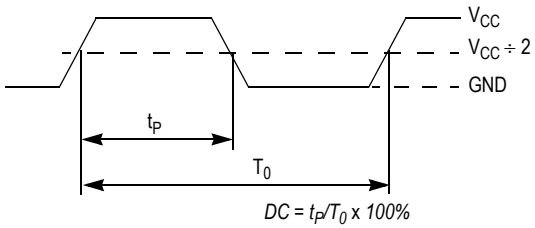
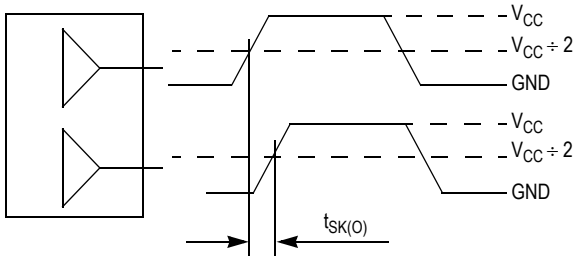


Figure 15. Propagation Delay ($t_{Ø}$) Test Reference



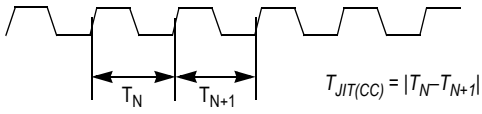
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



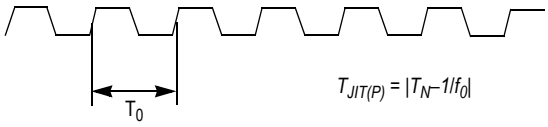
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$



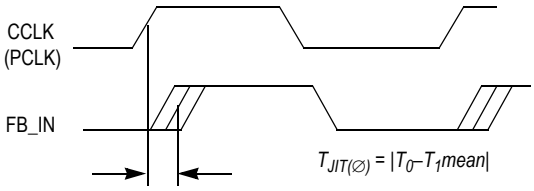
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter



The deviation in T_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 20. I/O Jitter

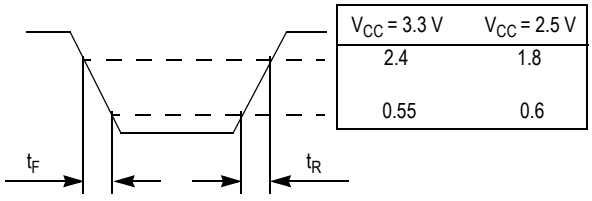
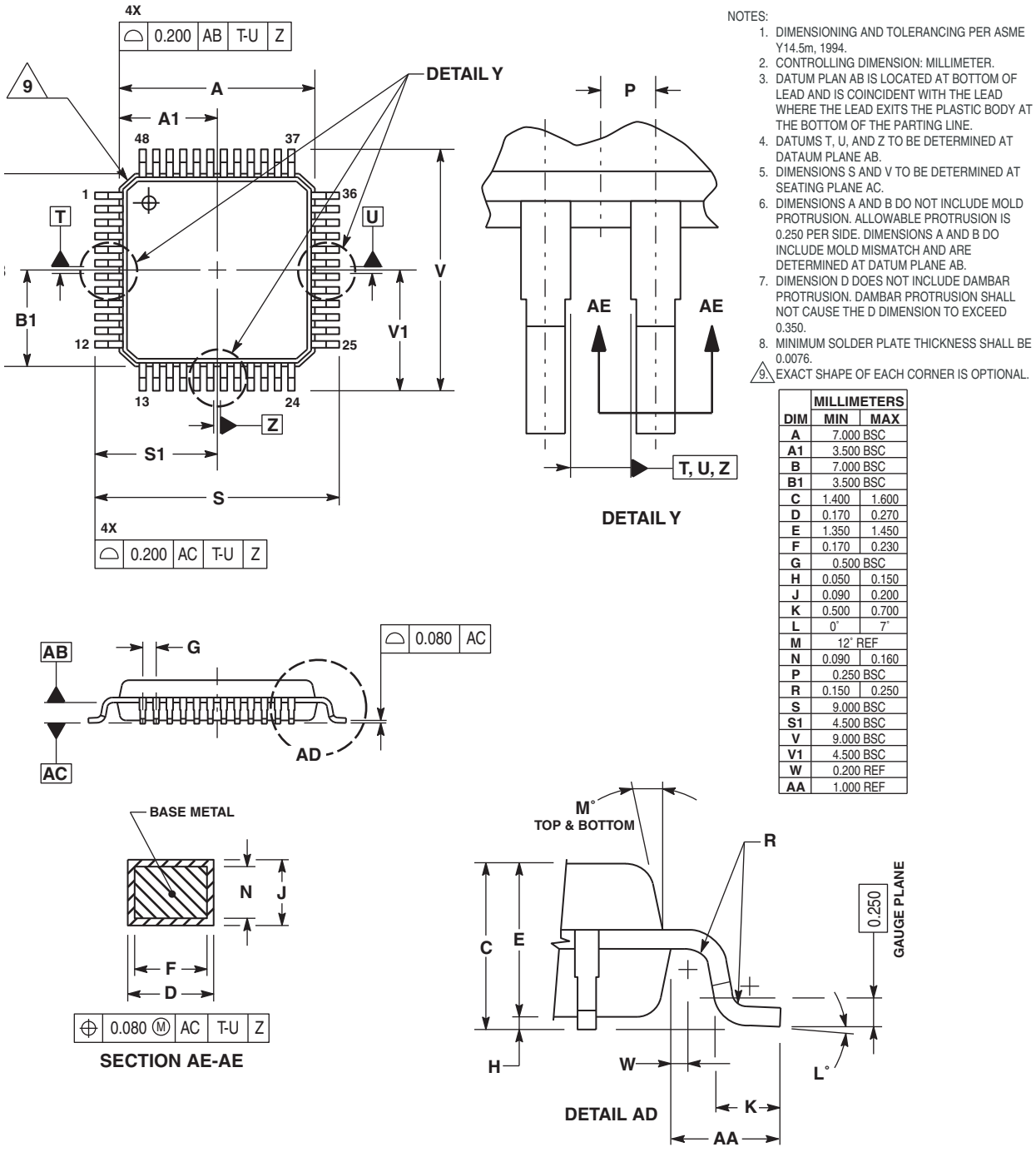


Figure 21. Transition Time Test Reference

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATAUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

CASE 932-03
ISSUE F
48-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
6		1	NRND – Not Recommend for New Designs	1/7/13

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