Low Noise, High-Speed Dual Operational Amplifier

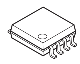
■ GENERAL DESCRIPTION

The NJM2719 is a dual high speed voltage feedback operational amplifier specifically optimized for low voltage noise.

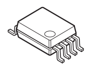
A voltage noise specification of 2.5nV/√Hz Typ. (at f =100kHz), a unity gain of 100MHz combine to make the NJM2719 an ideal choice for I/Q baseband amplifier, RFID reader application and other in wireless communication system desighns.

The NJM2719 is available in the 8-pin SO package (DMP8) with standard pinouts. For compact layouts, the dual is also available in a tiny dual fine pitch 8-pin package (SSOP8, TVSP8).

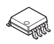
■PACKAGE OUTLINE



NJM2719M (DMP8)



NJM2719V (SSOP8)



NJM2719RB1 (TVSP8)

■ FEATURES

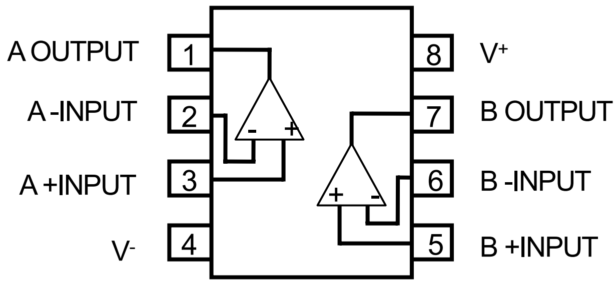
●**Low Noise**	**Vni = 2.5nV/√Hz typ. at f=100kHz** **Vni = 3nV/√Hz typ. at f=10kHz**
●**Unity Gain Bandwidth**	**fT = 100MHz typ. at V^+/V^- = ±5V** **fT = 90MHz typ. at V^+/V^- = ±2.5V**
●Phase Margin	Φm = 60deg typ.
●Slew Rate	60V/µs typ. at V^+/V^- = ±5V 35V/µs typ. at V^+/V^- = ±2.5V
●Output Rail-to-Rail	V_{OH} ≥ +4.7V, V_{OL} ≤ -4.8V at V^+/V^- = ±5V V_{OH} ≥ +2.4V, V_{OL} ≤ -2.4V at V^+/V^- = ±2.5V
●Operating Voltage	±2.5V ~ ±5V
●Bipolar Technology	
●Package Outline	DMP8 [NJM2719M] SSOP8 [NJM2719V] TVSP8 [NJM2719RB1]

■ APPLICATION

- ●Wireless Communication Equipment
- ●I/Q Baseband Application
- ●RFID Reader Application
- ●Active Filter
- ●ADC/DAC Buffer
- ●Ultrasound Amplifier

■ PIN CONFIGURATION

(Top View)



DMP8 [NJM2719M]
SSOP8 [NJM2719V]
TVSP8 [NJM2719RB1]

■ ABSOLUTE MAXIMUM RATINGS (Ta=25˚C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+5.5	V
Common Mode Input Voltage Range	V_{ICM}	±5.5 (Note1)	V
Differential Input Voltage Range	V_{ID}	±3	V
Power Dissipation	P_D	370 [DMP8],310 [SSOP8], 400[TVSP8]	mW
		470[DMP8](Note2),410[SSOP8](Note2), 510[TVSP8] (Note2)	mW
Operating Temperature Range	T_{opr}	-40 to +85	˚C
Storage Temperature Range	T_{stg}	-50 to +150	˚C

(Note 1) The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

(Note 2) On the PCB " EIA/JEDEC (76.2x114.3x1.6mm, two layers, FR-4) "

(Note 3) Do not exceed "Power dissipation: PD" in which power dissipation in IC is shown by the absolute maximum rating.
Refer to following Figure 1 for a permissible loss when ambient temperature (Ta) is Ta ≥25°C.

Figure1A: Power Dissipation – Ambient Temperature

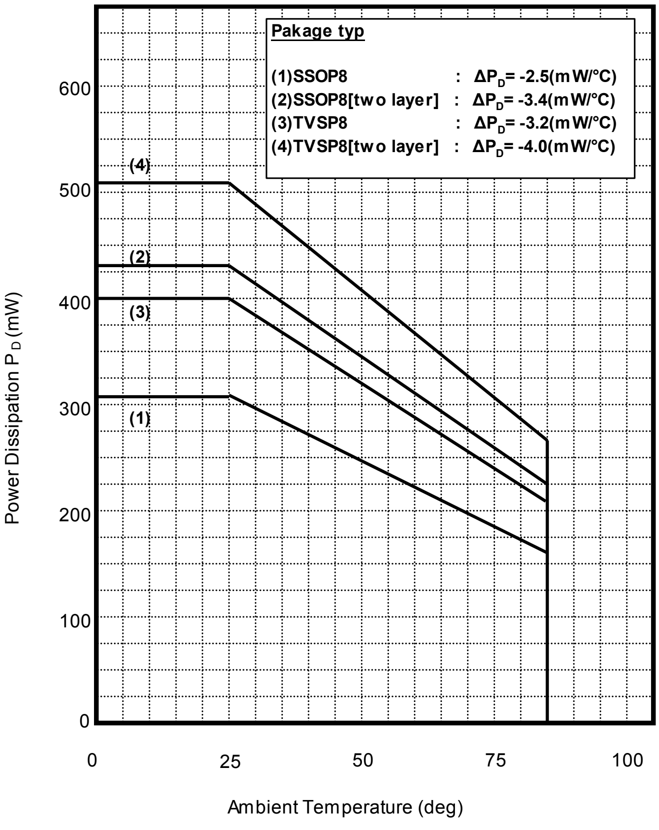
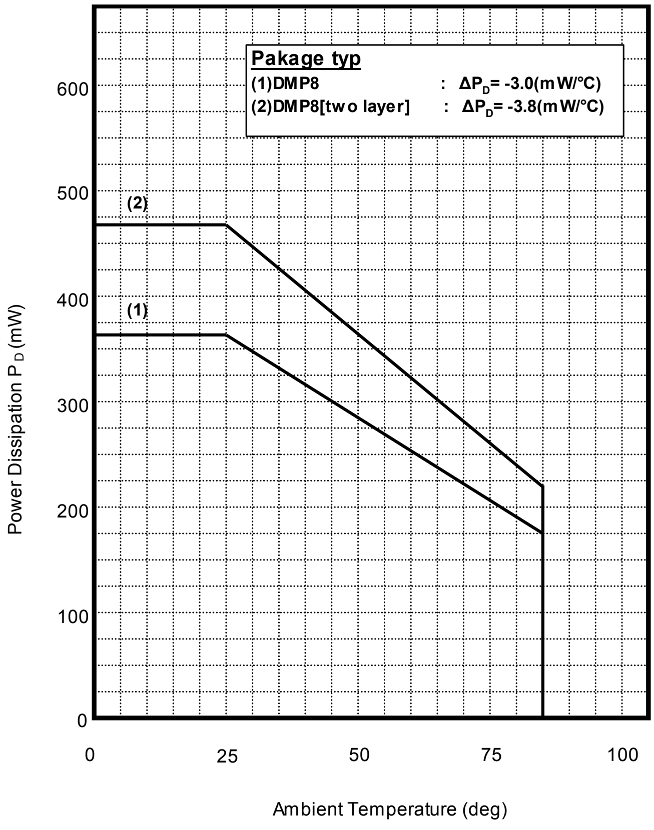


Figure1B: Power Dissipation – Ambient Temperature



■ OPERATING VOLTAGE (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+/V^-	(Note3)	±2.25	-	±5.5	V

■ ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V^+/V^-=±2.5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	Icc	No Signal	-	11	14	mA
Input Offset Voltage	V_{IO}	Rs=50Ω	-	1	9	mV
Input Offset Voltage Drift	ΔVio/ΔT	Rs=50Ω	-	10	-	μV/deg
Input Bias Current	I_B		-	2.9	25	μA
Input Offset Current	I_{IO}		-	0.2	2	μA
Voltage Gain	Av	R_L = 1kΩ to 0V, Vo = ±1V	68	91	-	dB
Common Mode Rejection Ratio	CMR	-2V ≤ V_{CM} ≤ +1.2V	82	92	-	dB
Supply Voltage Rejection Ratio	SVR	±2.25V ≤ V^+/V^- ≤ ±5V	84	97	-	dB
Maximum Output Voltage 1	V_{OH1}	R_L = 1kΩ to 0V	+2.3	+2.4	-	V
	V_{OL1}		-	-2.4	-2.3	
Maximum Output Voltage 2	V_{OH2}	Isource =4mA, +Input =+0.1V, -Input =-0.1V	+2.2	+2.3	-	V
	V_{OL2}	Isink =4mA, +Input =-0.1V, -Input =+0.1V	-	-2.3	-2.2	
Common Mode Input Voltage Range	V_{ICM}+	CMR≥82dB	+1.2	-	-	V
	V_{ICM}-		-	-	-2	

●AC CHARACTERISTICS (V^+/V^-=±2.5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Unity Gain	fT	Av=+40dB, Rf =1.98kΩ, Rg =20Ω, R_L =1kΩ to 0V, C_L =5pF	-	90	-	MHz
Phase Margin	φm		-	60	-	deg
Gain Margin	Gm		-	10	-	dB
Equivalent Input Noise Voltage	V_{NI1}	f =100kHz	-	2.5	-	nV/√Hz
	V_{NI2}	f =10kHz	-	3	-	
Equivalent Input Noise Current	I_{NI}	f =100kHz	-	3	-	pA/√Hz
Channel Separation	CS	f =1MHz, Vin =0.2Vpp, Av =+1, R_L =1kΩ to 0V, C_L =5pF	-	70	-	dB

●TRANSIENT CHARACTERISTICS (V^+/V^-=±2.5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate 1	+SR1	Av =0dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp	-	35	-	V/μs
	-SR1		-	35	-	
Slew Rate 2	+SR2	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp	-	30	-	V/μs
	-SR2		-	30	-	
Rise Time	tr	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =0.2Vpp, 10% to 90%	-	8.3	-	ns
Fall Time	tf		-	8.3	-	
Power Band Width	PBW	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp, HD2 ≤-40dB, HD3 ≤-40dB	-	3	-	MHz
Total Harmonic Distortion	THD	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, f =10kHz, Vout =2Vpp	-	0.1	-	%
Second Harmonic	HD2	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, f =1MHz, Vout =2Vpp	-	-50	-	dBc
Third Harmonic	HD3		-	-50	-	
Settling time (1%)	ts1	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp	-	100	-	ns
Settling time (0.1%)	ts2		-	110	-	

●DC CHARACTERISTICS (V^+/V^-=±5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	Icc	No Signal	-	14	17	mA
Input Offset Voltage	V_{IO}	Rs=50Ω	-	1	9	mV
Input Offset Voltage Drift	ΔVio/ΔT	Rs=50Ω	-	10	-	μV/deg
Input Bias Current	I_B		-	2.9	25	μA
Input Offset Current	I_{IO}		-	0.2	2	μA
Voltage Gain	Av	R_L = 1kΩ to 0V, Vo = ±1V	70	91	-	dB
Common Mode Rejection Ratio	CMR	-4.5V ≤ V_{CM} ≤ +3.7V	82	92	-	dB
Supply Voltage Rejection Ratio	SVR	±2.25V ≤ V^+/V^- ≤ ±5V	84	97	-	dB
Maximum Output Voltage 1	V_{OH1}	R_L = 1kΩ to 0V	+4.6	+4.7	-	V
	V_{OL1}		-	-4.8	-4.7	
Maximum Output Voltage 2	V_{OH2}	Isource =5mA, +Input =+0.1V, -Input =-0.1V	+4.5	+4.6	-	V
	V_{OL2}	Isink =5mA, +Input =-0.1V, -Input =+0.1V	-	-4.7	-4.6	
Common Mode Input Voltage Range	V_{ICM}+	CMR≥82dB	+3.7	-	-	V
	V_{ICM}-		-	-	-4.5	

●AC CHARACTERISTICS (V^+/V^-=±5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Unity Gain	fT	Av=+40dB, Rf =1.98kΩ, Rg =20Ω, R_L =1kΩ to 0V, C_L =5pF	-	100	-	MHz
Phase Margin	φm		-	60	-	deg
Gain Margin	Gm		-	10	-	dB
Equivalent Input Noise Voltage	V_{NI1}	f =100kHz	-	2.5	-	nV/√Hz
	V_{NI2}	f =10kHz	-	3	-	
Equivalent Input Noise Current	I_{NI}	f =100kHz	-	3	-	pA/√Hz
Channel Separation	CS	f =1MHz, Vin =0.2Vpp, Av =+1, R_L =1kΩ to 0V, C_L =5pF	-	70	-	dB

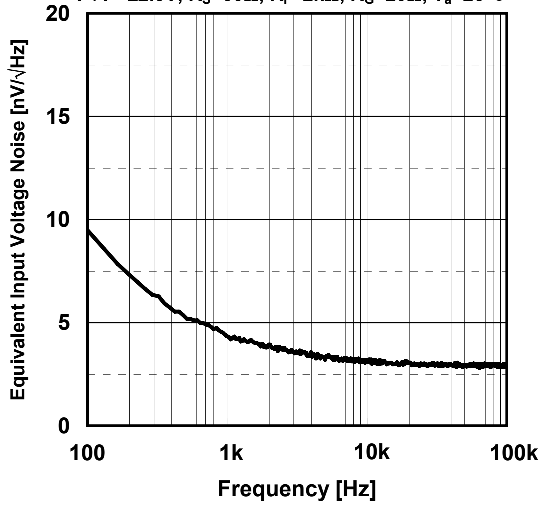
●TRANSIENT CHARACTERISTICS (V^+/V^-=±5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate 1	+SR1	Av =0dB, R_L =1kΩ to 0V, C_L =5pF, Vout =5Vpp	-	60	-	V/μs
	-SR1		-	60	-	
Slew Rate 2	+SR2	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =5Vpp	-	55	-	V/μs
	-SR2		-	55	-	
Rise Time	tr	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =0.2Vpp, 10% to 90%	-	8	-	ns
Fall Time	tf		-	8	-	
Power Band Width	PBW	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp, HD2 ≤-40dB, HD3 ≤-40dB	-	4	-	MHz
Total Harmonic Distortion	THD	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, f =10kHz, Vout =2Vpp	-	0.1	-	%
Second Harmonic	HD2	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, f =1MHz, Vout =2Vpp	-	-50	-	dBc
Third Harmonic	HD3		-	-50	-	
Settling time (1%)	ts1	Av =+6dB, R_L =1kΩ to 0V, C_L =5pF, Vout =2Vpp	-	90	-	ns
Settling time (0.1%)	ts2		-	110	-	

■ TYPICAL CHARACTERISTICS

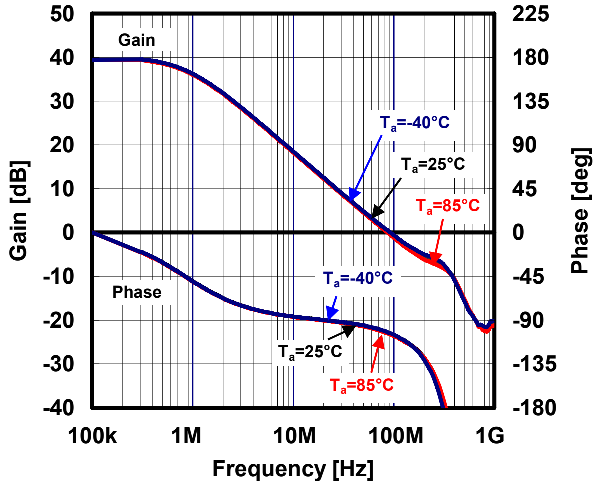
Equivalent Input Voltage Noise vs. Frequency

V^+/V^-=±2.5V, R_S=50Ω, R_F=2kΩ, R_G=20Ω, T_a=25°C



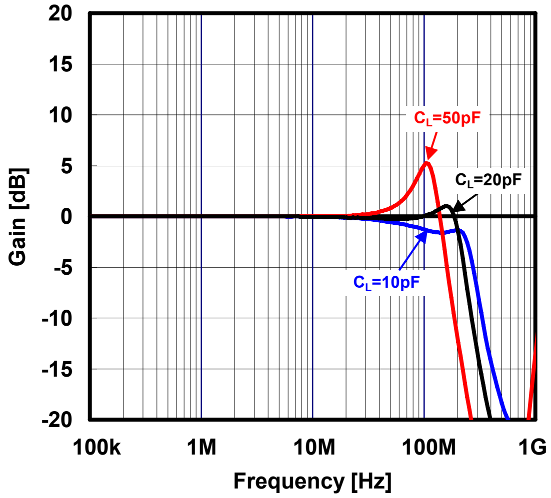
Closed-Loop Gain/Phase vs. Frequency (Temperature)

V^+/V^-=±2.5V, R_S=50Ω, R_F=2kΩ, R_G=20Ω,
R_L=1kΩ, C_L=5pF



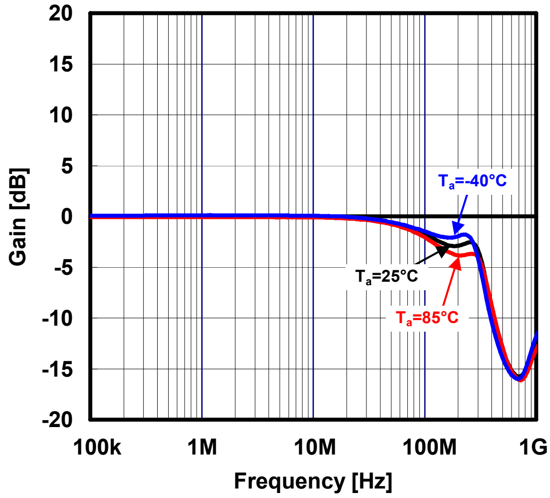
Unity Gain Frequency Response (Load Capacitance)

V^+/V^-=±2.5V, R_S=50Ω, R_L=1kΩ, Ta=25°C



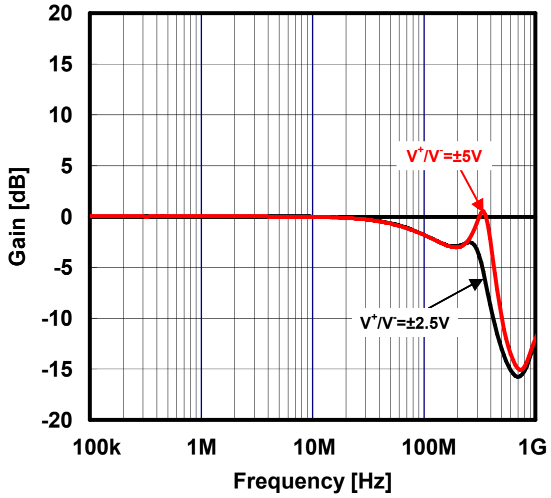
Unity Gain Frequency Response (Temperature)

V^+/V^-=±2.5V, R_S=50Ω, R_L=1kΩ, C_L=5pF



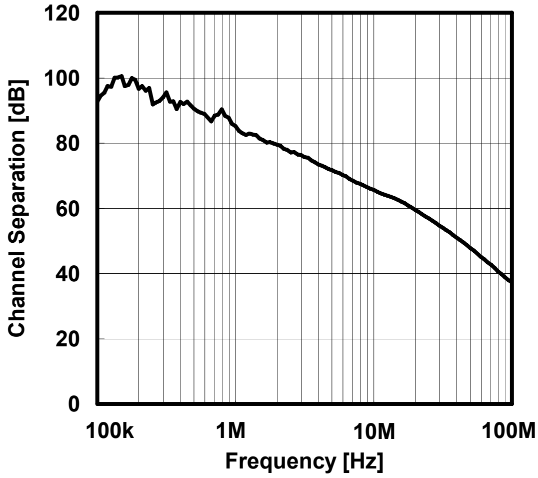
Unity Gain Frequency Response (Supply Voltage)

R_S=50Ω, R_L=1kΩ, C_L=5pF, Ta=25°C

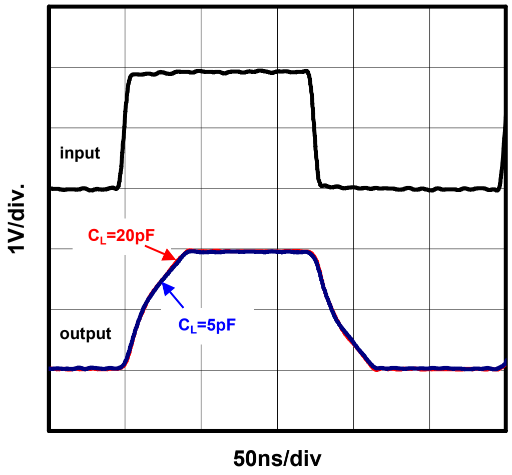


Channel Separation vs. Frequency

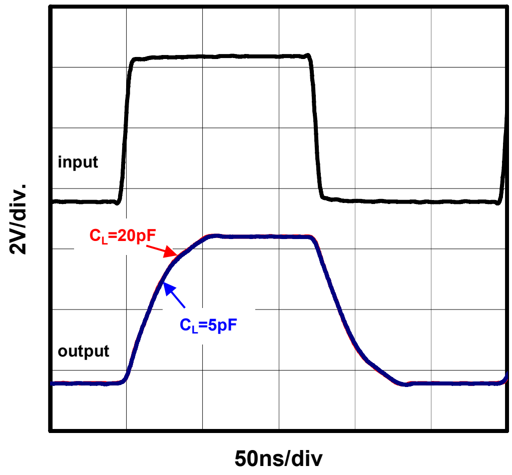
V^+/V^-=±2.5V, V_O=0.2Vpp, G_V=0dB,
R_L=1kΩ, C_L=5pF,



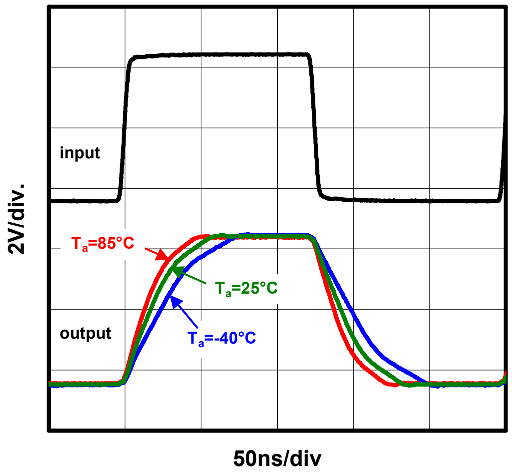
Transinet Response (Load Capacitance)
V^+/V^-=±2.5V,f=4MHz,V_O=2V_{PP},G_V=1,R_T=50Ω,
R_L=1kΩ,T_a=25°C



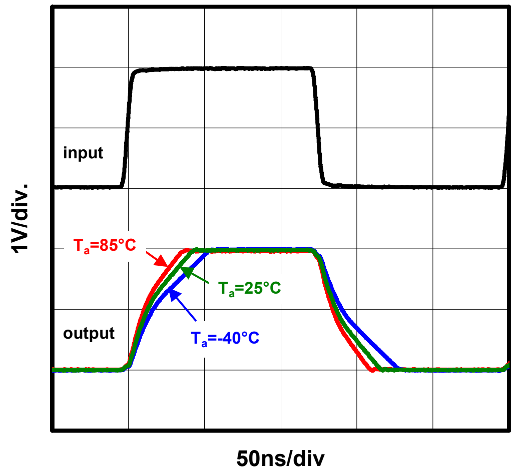
Transient Response (Load Capacitance)
V^+/V^-=±5V,f=4MHz,V_O=5V_{PP},G_V=1,R_T=50Ω,
R_L=1kΩ,T_a=25°C



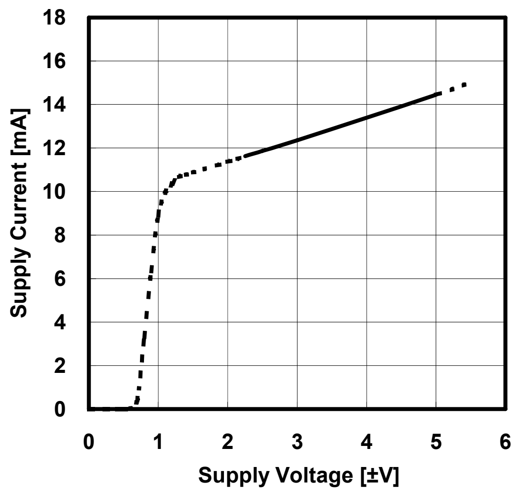
Transient Response (Temperature)
V^+/V^-=±5V,f=4MHz,V_O=5V_{PP},G_V=1,R_T=50Ω,
R_L=1kΩ, C_L=5pF



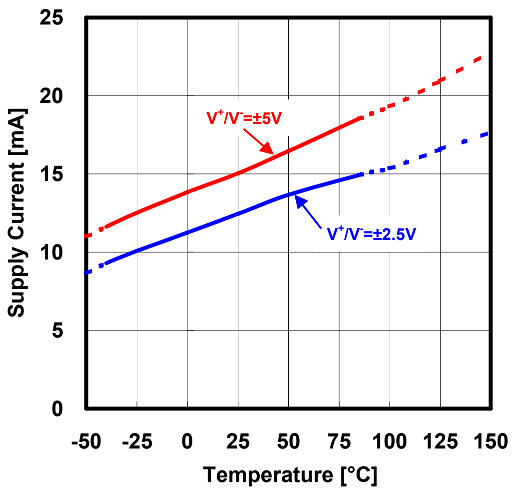
Transeint Response (Temperature)
V^+/V^-=±2.5V,f=4MHz,V_O=2V_{PP},G_V=1,R_T=50Ω,
R_L=1kΩ, C_L=5pF

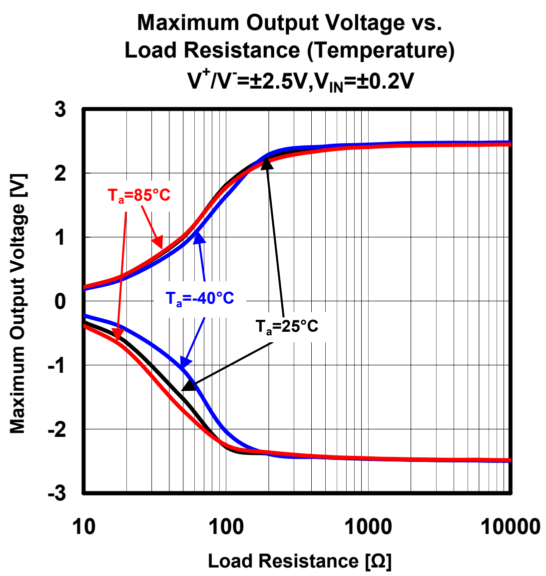


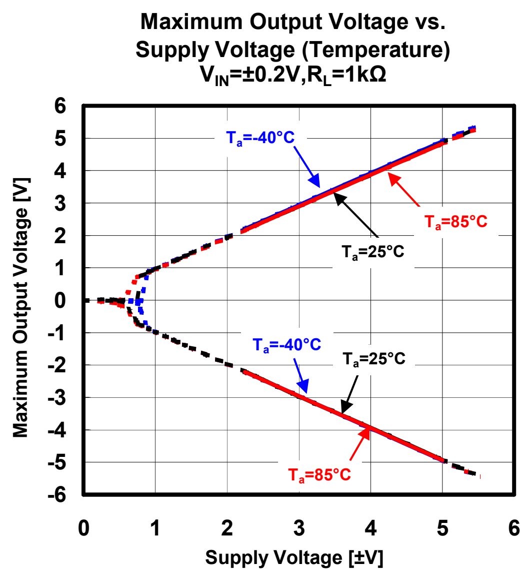
Supply Current vs. Supply Voltage
G_V=0dB, Ta=25°C

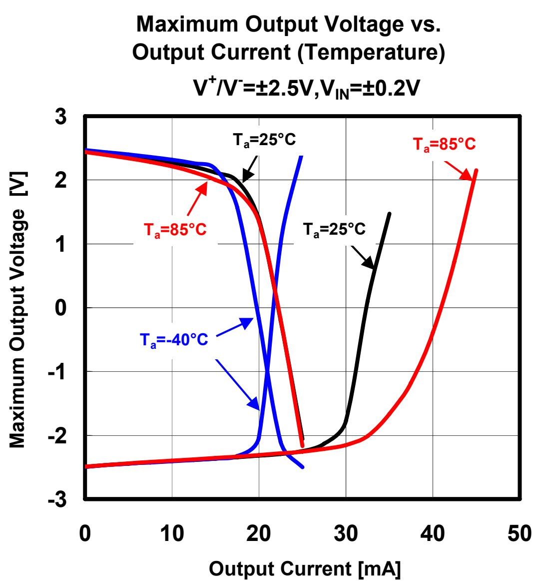


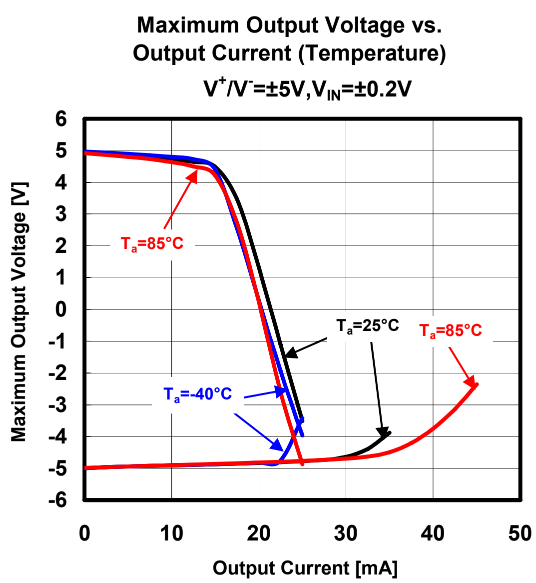
Supply Current vs. Temperature
G_V=0dB, V_{ICM}=0V

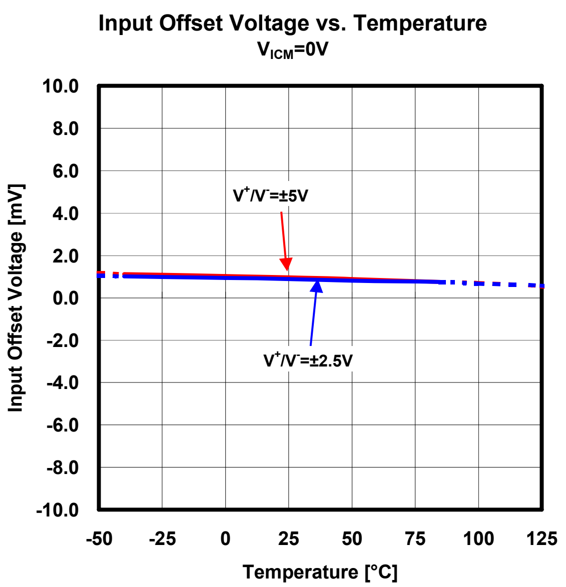


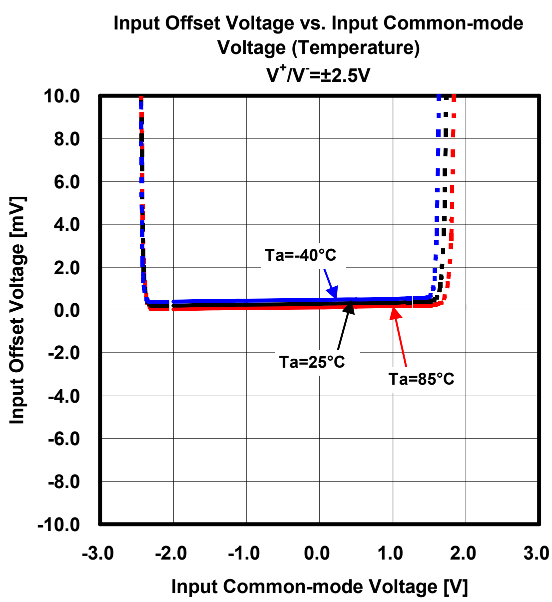

Maximum Output Voltage vs.
Load Resistance (Temperature)
V+/V-=±2.5V,VIN=±0.2V
Ta=85°C
Ta=-40°C
Ta=25°C
Maximum Output Voltage [V]
Load Resistance [Ω]
3
2
1
0
-1
-2
-3
10
100
1000
10000


Maximum Output Voltage vs.
Supply Voltage (Temperature)
VIN=±0.2V,RL=1kΩ
Ta=-40°C
Ta=85°C
Ta=25°C
Ta=-40°C
Ta=25°C
Ta=85°C
Maximum Output Voltage [V]
Supply Voltage [±V]
6
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
0
1
2
3
4
5
6

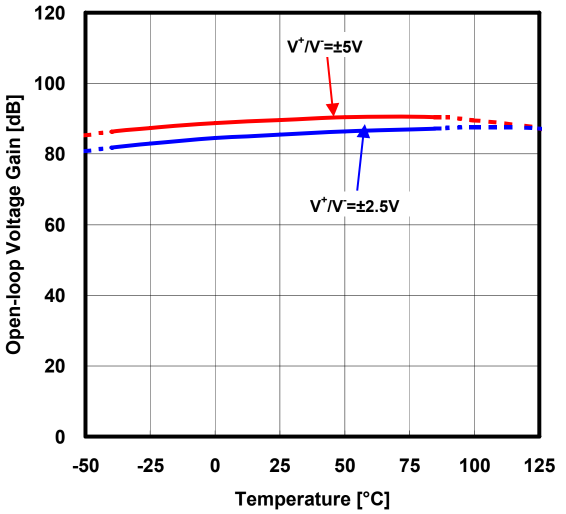

Maximum Output Voltage vs.
Output Current (Temperature)
V+/V-=±2.5V,VIN=±0.2V
Ta=25°C
Ta=85°C
Ta=85°C
Ta=25°C
Ta=-40°C
Maximum Output Voltage [V]
Output Current [mA]
3
2
1
0
-1
-2
-3
0
10
20
30
40
50


Maximum Output Voltage vs.
Output Current (Temperature)
V+/V-=±5V,VIN=±0.2V
Ta=85°C
Ta=25°C
Ta=85°C
Ta=-40°C
Maximum Output Voltage [V]
Output Current [mA]
6
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
0
10
20
30
40
50

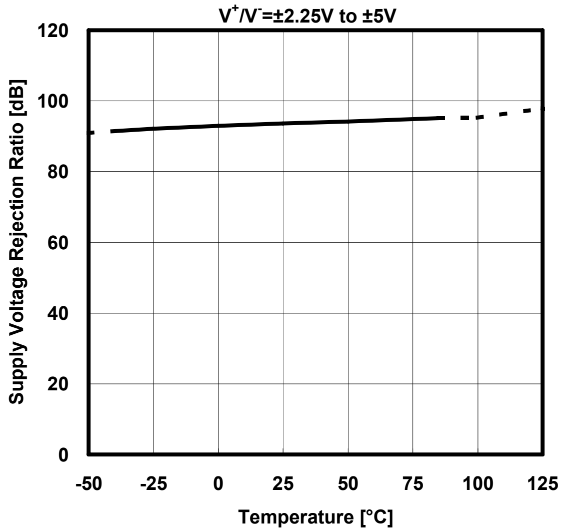

Input Offset Voltage vs. Temperature
VICM=0V
V+/V-=±5V
V+/V-=±2.5V
Input Offset Voltage [mV]
Temperature [°C]
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-50
-25
0
25
50
75
100
125


Input Offset Voltage vs. Input Common-mode
Voltage (Temperature)
V+/V-=±2.5V
Ta=-40°C
Ta=25°C
Ta=85°C
Input Offset Voltage [mV]
Input Common-mode Voltage [V]
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-3.0
-2.0
-1.0
0.0
1.0
2.0
3.0

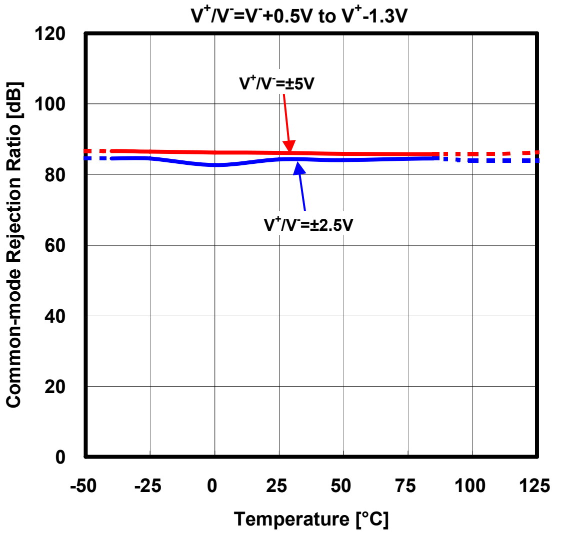
Open-loop Voltage Gain vs. Temperature
V_{OUT}=-1V to +1V, R_L=1kΩ



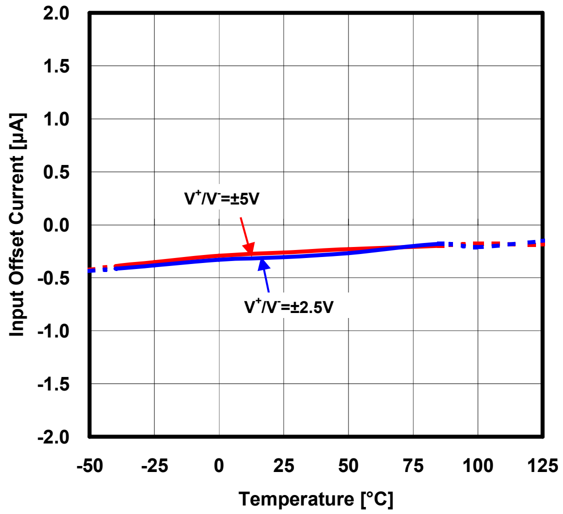
Supply Voltage Rejection Ratio vs. Temperature
V^+/V^-=±2.25V to ±5V



Common-mode Rejection Ratio vs. Temperature
$V^+/V^-=V^-+0.5V$ to $V^+-1.3V$



Input Offset Voltage vs. Temperature
V_{ICM}=0V



■ APPLICATION

●Stability

Generally, when driving a large capacitive load in low closed-loop gain or unity-gain configurations, circuit stability is reduced. In the case of using the NJM2719 for these configurations, it is necessary to care about unwanted oscillation.

An effective way to improve stability and to avoid oscillation is to add an isolation resistor as shown in Figure 1.

Figure 2 shows required resistor values (R_{ISO}) for stability versus load capacitances (C_L) in the unity-gain configuration (Figure 1). To ensure the stability, add a larger isolation resistor in Figure 2. (Resistor values in Figure2 are reference values when parasitic capacitance of an evaluation board is minimized.)

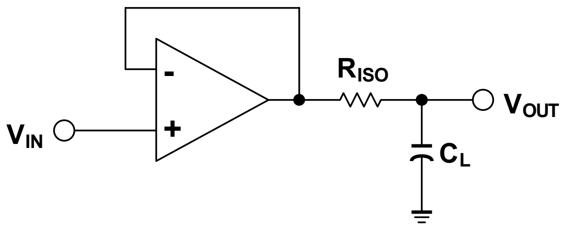


Figure 1.

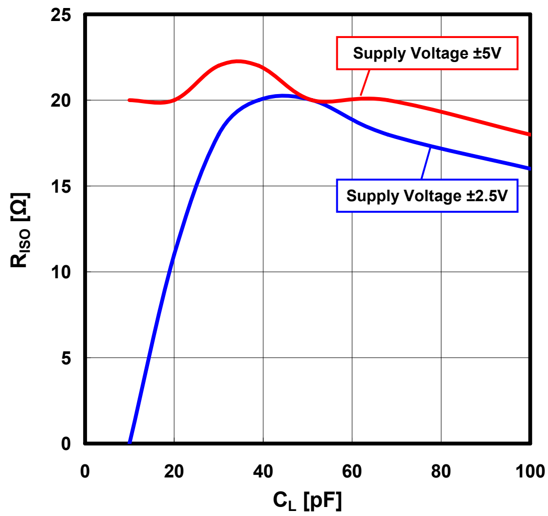


Figure 2. Required Isolation Resistor values for stability, R_{ISO}[Ω], versus Capacitive Loads, C_L[pF]. (G_V=0dB)

■ NOTE