



STD38NH02L - STD38NH02L-1

N-CHANNEL 20V - 0.011Ω - 38A DPAK/IPAK

STripFET™ III POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD38NH02L	20 V	<0.0135Ω	38 A
STD38NH02L-1	20 V	<0.0135Ω	38 A

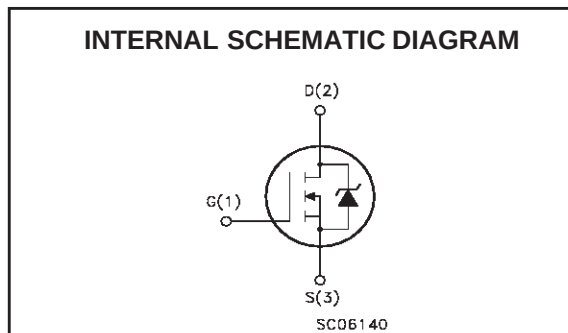
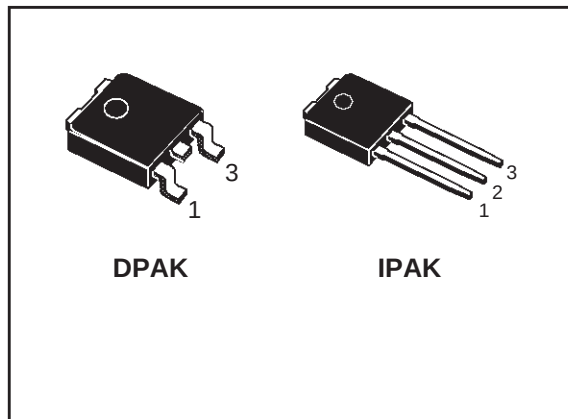
- TYPICAL R_{DS(on)} = 0.011Ω @ 10 V
- R_{DS(on)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

The **STD38NH02L** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	20	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	38	A
I _D	Drain Current (continuous) at T _C = 100°C	27	A
I _{DM} ()	Drain Current (pulsed)	152	A
P _{TOT}	Total Dissipation at T _C = 25°C	40	W
	Derating Factor	0.27	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	250	mJ
T _{stg}	Storage Temperature	- 55 to 175	°C
T _j	Max. Operating Junction Temperature		

● Pulse width limited by safe operating area

(1) Starting T_j=25°C, I_D=19A, V_{DD}=18V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	3.75	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
T _I	Maximum Lead Temperature for Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	20			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 19 A V _{GS} = 6.3 V, I _D = 19 A		0.011 0.013	0.0135 0.017	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 20V, I _D = 19A		6		S
C _{iss}	Input Capacitance	V _{DS} = 15V, f = 1 MHz, V _{GS} = 0		1070		pF
C _{oss}	Output Capacitance			305		pF
C _{rss}	Reverse Transfer Capacitance			45		pF
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 19\text{ A}$		7		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		62		ns
Q_g	Total Gate Charge	$0.44\text{ V} \leq V_{DD} \leq 10\text{ V}$, $I_D = 38\text{ A}$, $V_{GS} = 10\text{ V}$		18	24	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			2.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 19\text{ A}$,		25		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		12		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				38	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				152	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 38\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		27		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 18\text{ V}$, $T_j = 150^\circ\text{C}$		22		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		1.6		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

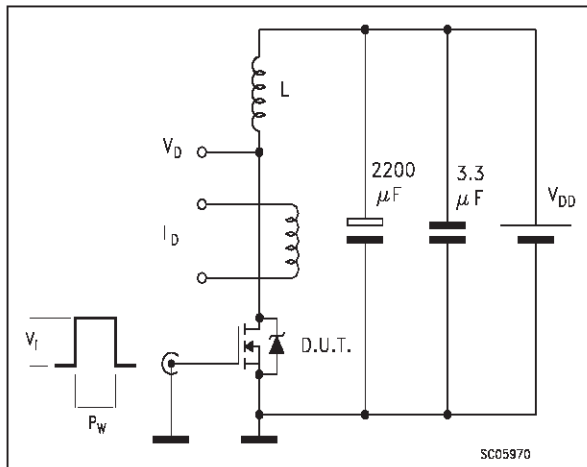


Fig. 2: Unclamped Inductive Waveform

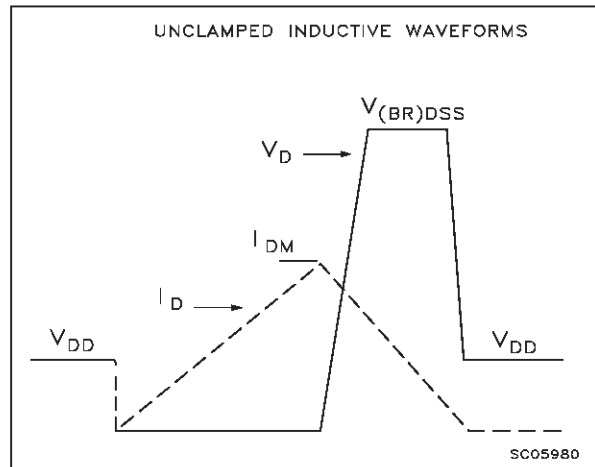


Fig. 3: Switching Times Test Circuit For Resistive Load

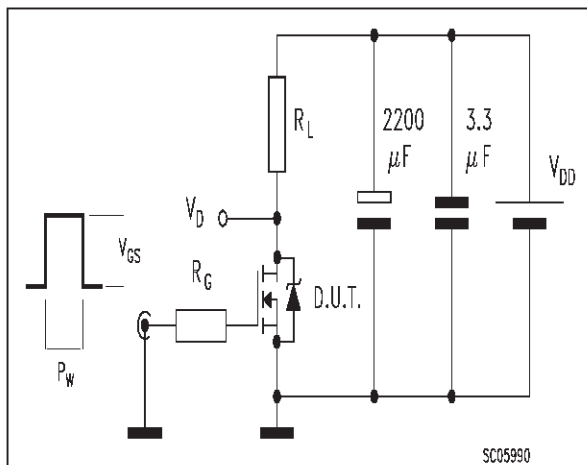


Fig. 4: Gate Charge test Circuit

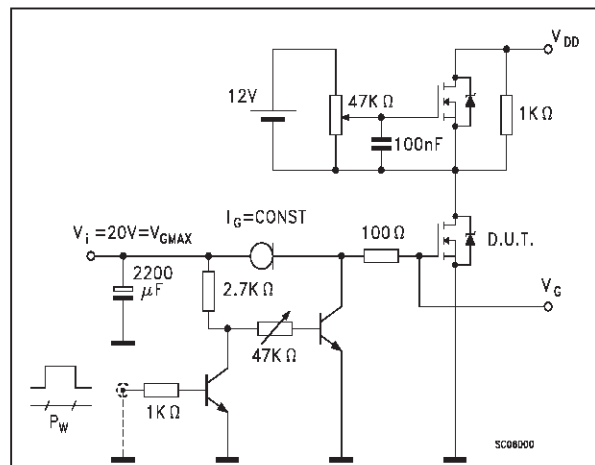
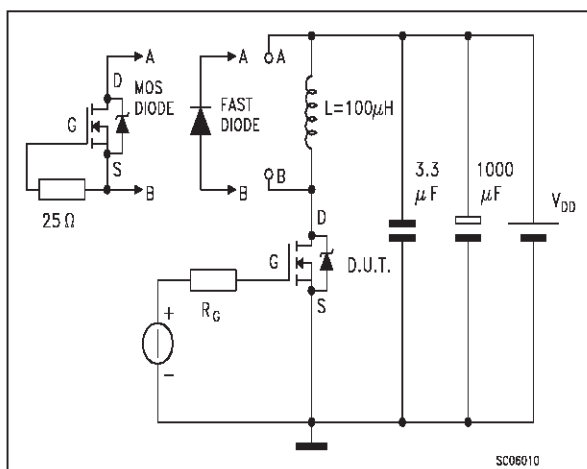
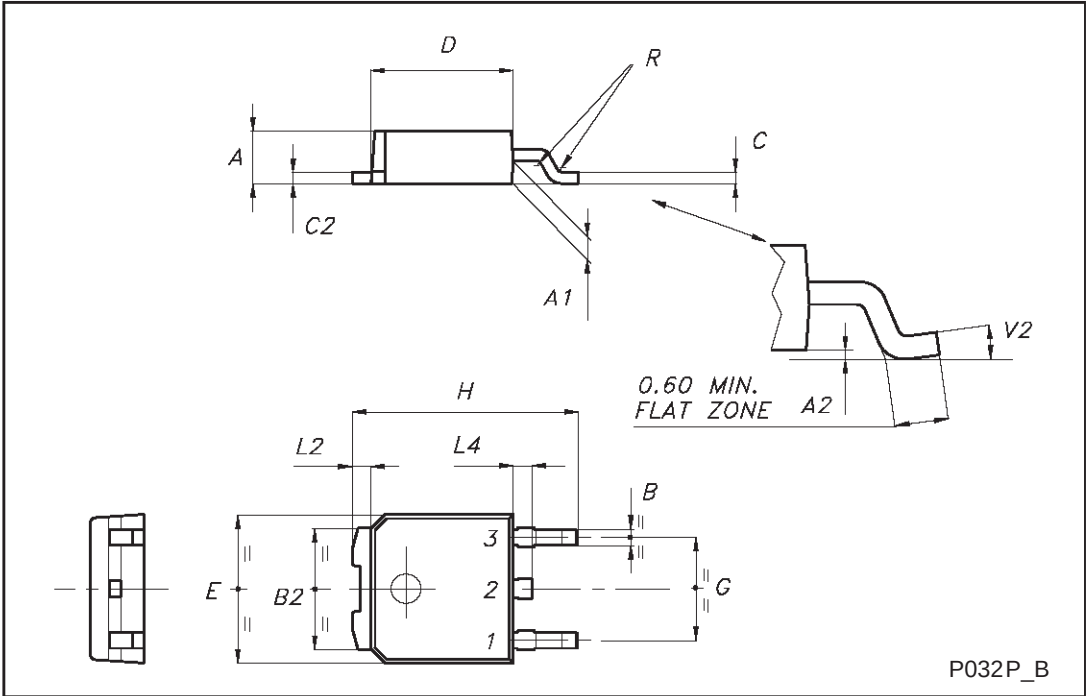


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

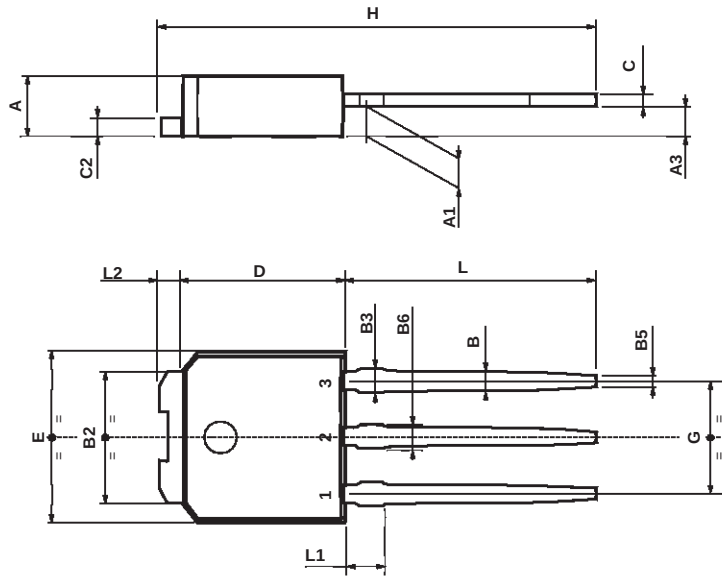
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P_B

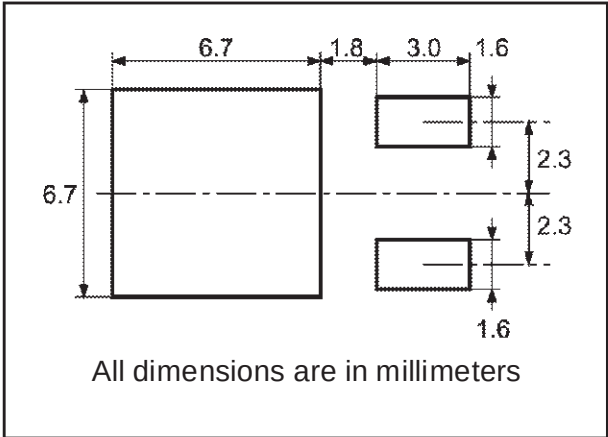
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

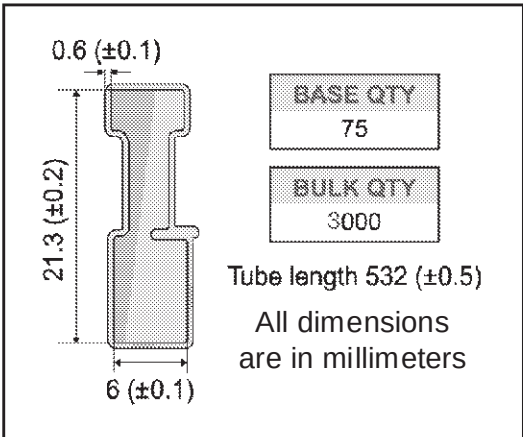


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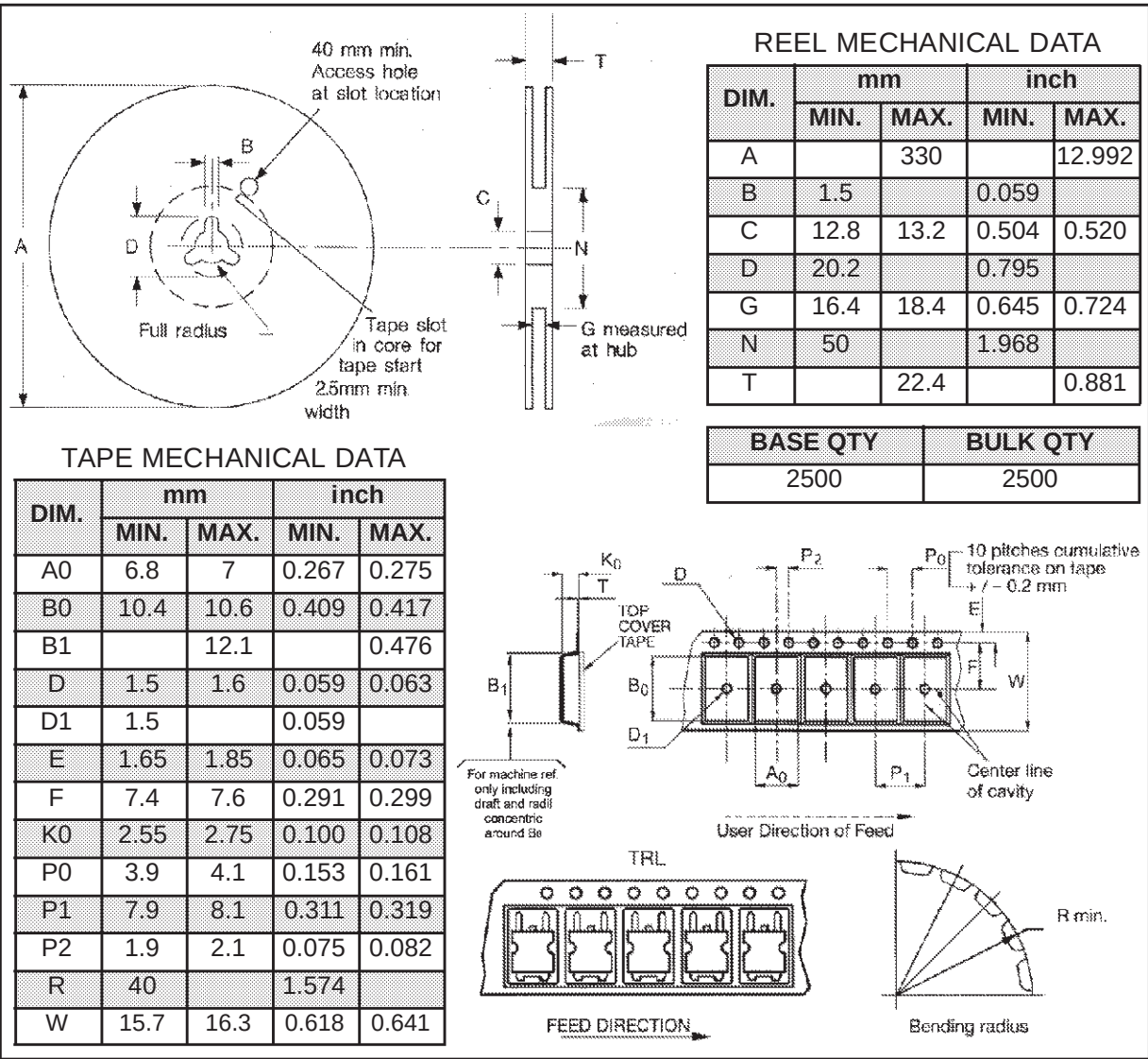
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



* on sales type
ST

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