



TO-252
(DPAK)



Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A)
100	13 @ V _{GS} =10V	70

Features

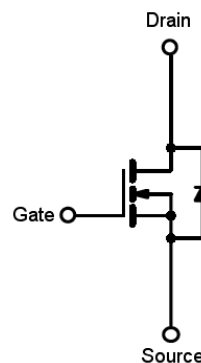
- Advanced Trench Technology
- Low R_{DS(ON)} 13mΩ (Max.)
- Low gate charge typical @ 145nC (Typ.)
- Low Crss typical @ 120pF (Typ.)

Ordering Information

Part No.	Package	Packing
TSM70N10CP ROG	TO-252	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _C =25°C	70
		T _C =70°C	61
		T _A =25°C	12
		T _A =70°C	9
Drain Current-Pulsed Note 1	I _{DM}	150	A
Avalanche Current, L=0.5mH	I _{AS} , I _{AR}	25	A
Avalanche Energy, L=0.5mH	E _{AS} , E _{AR}	156	mJ
Maximum Power Dissipation	P _D	T _C =25°C	120
		T _C =70°C	80
		T _A =25°C	8.3
		T _A =70°C	5.3
Storage Temperature Range	T _{STG}	-55 to +150	°C
Operating Junction Temperature Range	T _J	-55 to +150	°C

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	Rθ _{JC}	1	°C/W
Thermal Resistance - Junction to Ambient	Rθ _{JA}	40	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

Electrical Specifications (Ta = 25°C unless otherwise noted)

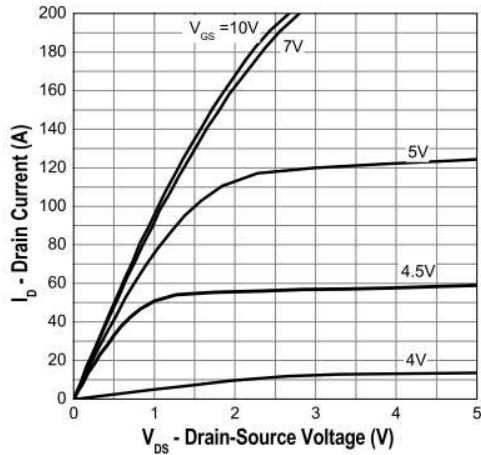
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250uA	BV _{DSS}	100	--	--	V
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 30A	R _{DS(ON)}	--	10	13	mΩ
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250uA	V _{GS(TH)}	2	3	4	V
Zero Gate Voltage Drain Current	V _{DS} = 80V, V _{GS} = 0V	I _{DSS}	--	--	1	uA
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Dynamic						
Total Gate Charge	V _{DS} = 50V, I _D = 30A, V _{GS} = 10V	Q _g	--	145	--	nC
Gate-Source Charge		Q _{gs}	--	25	--	
Gate-Drain Charge		Q _{gd}	--	43	--	
Input Capacitance	V _{DS} = 30V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	4300	--	pF
Output Capacitance		C _{oss}	--	300	--	
Reverse Transfer Capacitance		C _{rss}	--	120	--	
Switching						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 50V, R _G = 3Ω	t _{d(on)}	--	27	--	nS
Turn-On Rise Time		t _r	--	13	--	
Turn-Off Delay Time		t _{d(off)}	--	15	--	
Turn-Off Fall Time		t _f	--	42	--	
Drain-Source Diode Characteristics and Maximum Rating						
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	V _{SD}	--	0.8	1.3	V
Reverse Recovery Time	I _S = 30A, T _J =25°C dI/dt = 100A/us	t _{fr}	--	165	--	nS
Reverse Recovery Charge		Q _{fr}	--	175	--	nC

Notes:

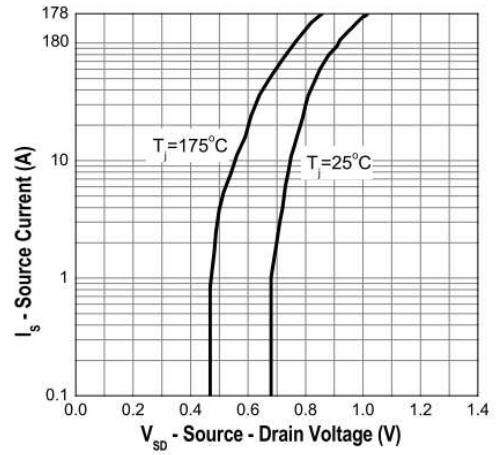
- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- Rθ_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Rθ_{JC} is guaranteed by design while Rθ_{CA} is determined by the user's board design. Rθ_{JA} shown below for single device operation on FR-4 in still air

Electrical Characteristics Curve ($T_c = 25^\circ\text{C}$, unless otherwise noted)

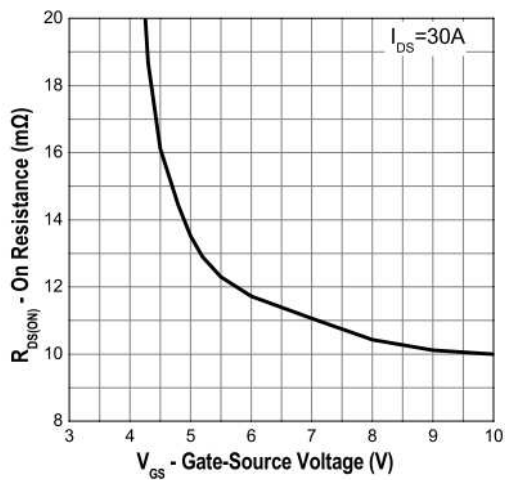
Output Characteristics



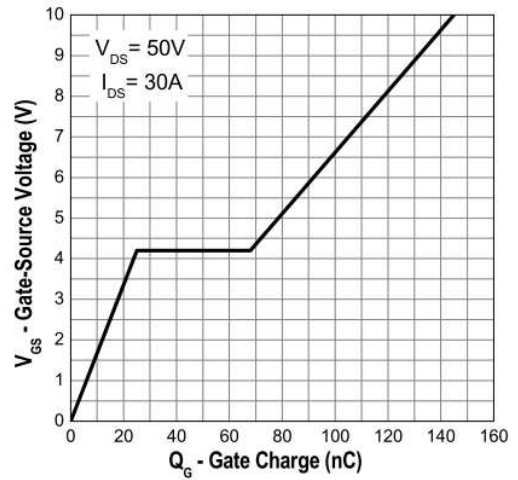
Transfer Characteristics



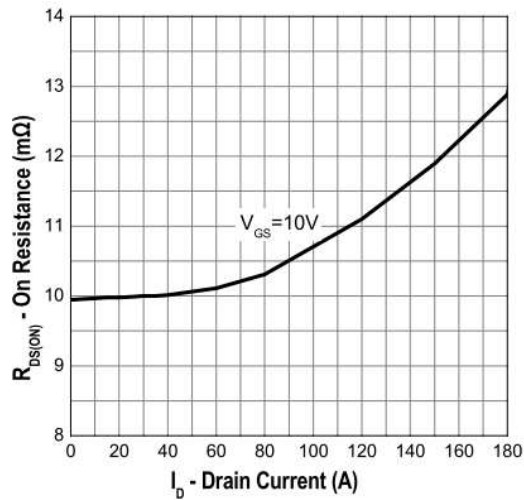
On-Resistance vs. Gate-Source Voltage



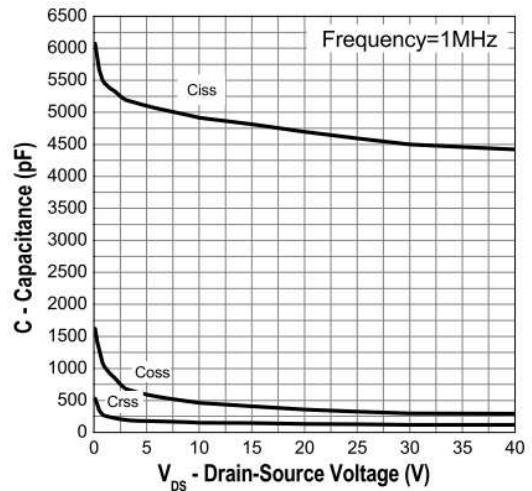
Gate Charge



On-Resistance vs. Junction Temperature

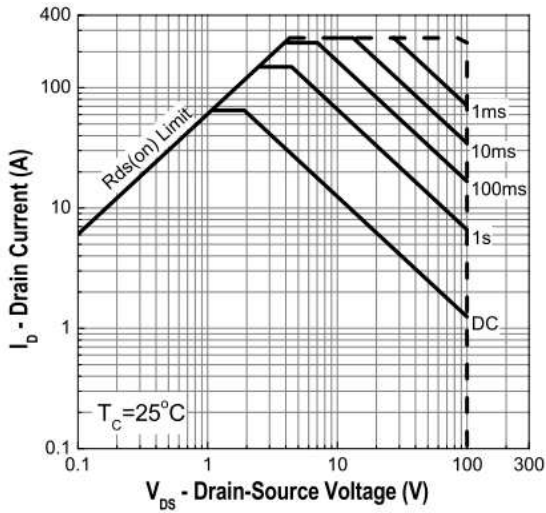


Capacitance

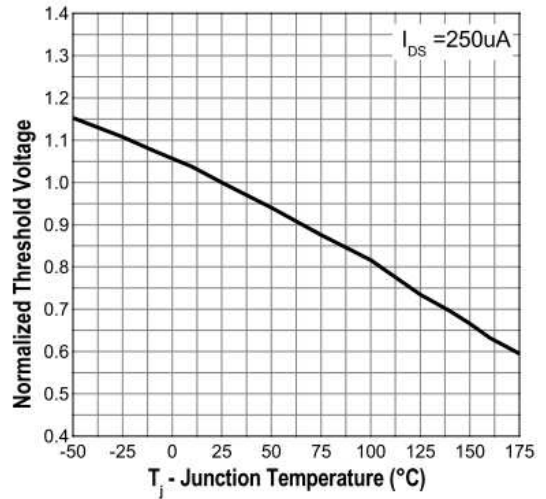


Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

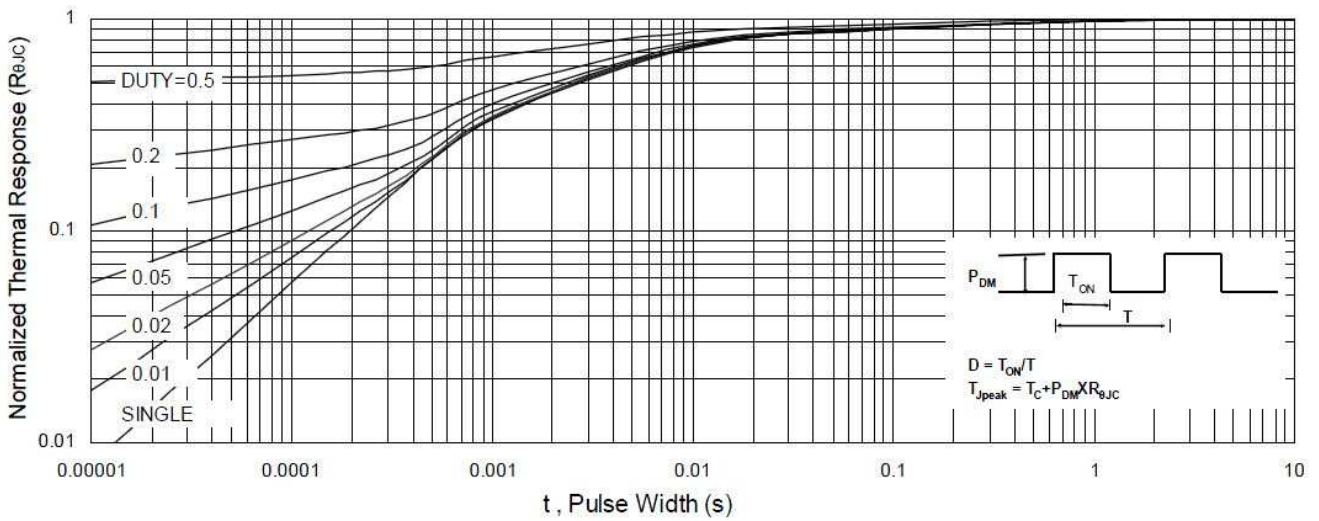
Maximum Safe Operating Area



Threshold Voltage vs. Temperature

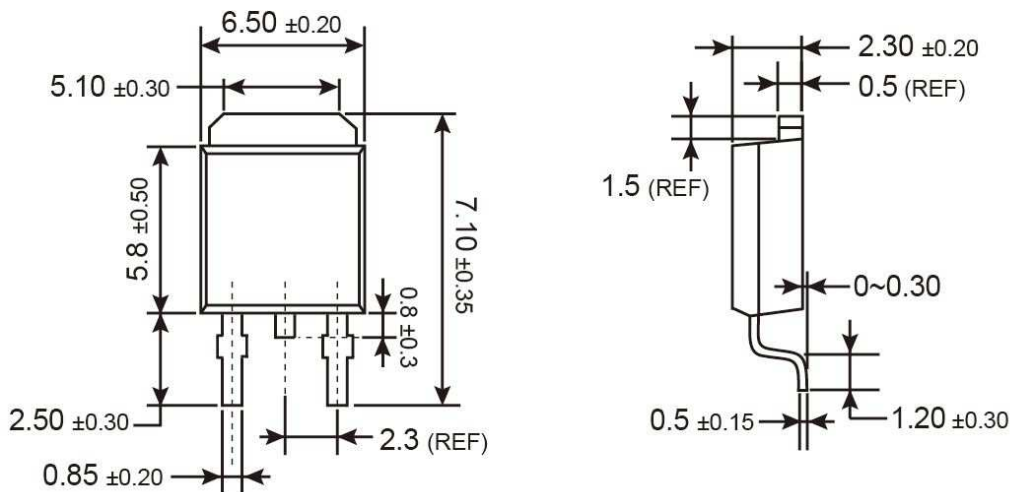


Normalized Thermal Transient Impedance, Junction-to-Ambient



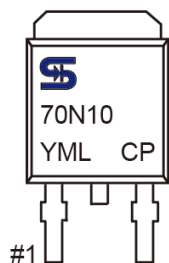


TO-252 Mechanical Drawing



Unit: Millimeters

Marking Diagram



- Y** = Year Code
- M** = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apr, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L** = Lot Code

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