

---

---

# SPECIFICATION

**CUSTOMER :** \_\_\_\_\_

**MODULE NO.:** **WG12232A-NGA-N**

---

<p><b>APPROVED BY:</b> ( FOR CUSTOMER USE ONLY )</p>	
--	--

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
<b>ISSUED DATE:</b>			

## Contents

- 1.Module Classification Information
- 2.Precautions in use of LCD Modules
- 3.General Specification
- 4.Absolute Maximum Ratings
- 5.Electrical Characteristics
- 6.Optical Characteristics
- 7.Interface Description

- 8. Contour Drawing & Block Diagram
- 9. Function Description
- 10. Commands Description
- 11. Timing Characteristics
- 12. Quality Assurance
- 13. Reliability

## 1. Module Classification Information

W G    1 2 2 3 2    A - N G A -    N  
 ① ②                    ③                    ④    ⑤ ⑥ ⑦                    ⑧

- ① Brand : WINSTAR DISPLAY CORPORATION
- ② Display Type : H→Character Type, G→Graphic Type
- ③ Display Font : 122 x 32 dot
- ④ Model serials no.
- ⑤ Backlight Type :
 

N→Without backlight	A→LED, Amber
B→EL, Blue green	R→LED, Red
D→EL, Green	O→LED, Orange
W→EL, White	G→LED, Green
F→CCFL, White	
Y→LED, Yellow Green	
- ⑥ LCD Mode :
 

B→TN Positive, Gray	T→FSTN Negative
N→TN Negative,	
G→STN Positive, Gray	
Y→STN Positive, Yellow Green	
M→STN Negative, Blue	
F→FSTN Positive	
- ⑦ LCD Polarize Type/ Temperature range/ View direction
 

A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00
G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00
E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00
- ⑧ Special Code
 

N : Without negative voltage
------------------------------

## **2.Precautions in use of LCD Modules**

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

## **3.General Specification**

<b>Item</b>	<b>Dimension</b>	<b>Unit</b>
Number of Characters	122 x 32 dot	—
Module dimension	84.0 x 44.0 x 10.2(MAX)	mm
View area	60.0 x 18.0	mm
Active area	53.64 x 15.64	mm
Dot size	0.4 x 0.45	mm
Dot pitch	0.44 x 0.49	mm
LCD type	STN, Positive, Reflective , Gray	
Duty	1/32	
View direction	6 o'clock	
Backlight Type	N/A	

## **4.Absolute Maximum Ratings**

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	$T_{OP}$	0	—	+50	°C
Storage Temperature	$T_{ST}$	-10	—	+60	°C
Input Voltage	$V_I$	0	—	$V_{DD}$	V
Supply Voltage For Logic	$V_{DD}$	0	—	6.7	V
Supply Voltage For LCD	$V_{DD}-V_{LCD}$	0	—	-10	V
Supply Voltage For LCD	VEE	—	—	-5	V

## 5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.75	5.0	5.25	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=0^{\circ}\text{C}$	—	—	4.9	V
		$T_a=25^{\circ}\text{C}$	—	4.6	—	V
		$T_a=+50^{\circ}\text{C}$	4.3	—	—	V
Input High Volt.	$V_{IH}$	—	$0.7V_{DD}$	—	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	—	0	—	$0.3V_{DD}$	V
Output High Volt.	$V_{OH}$	—	2.4	—	—	V
Output Low Volt.	$V_{OL}$	—	—	—	0.4	V
Supply Current	$I_{DD}$	—	—	1.0	—	mA

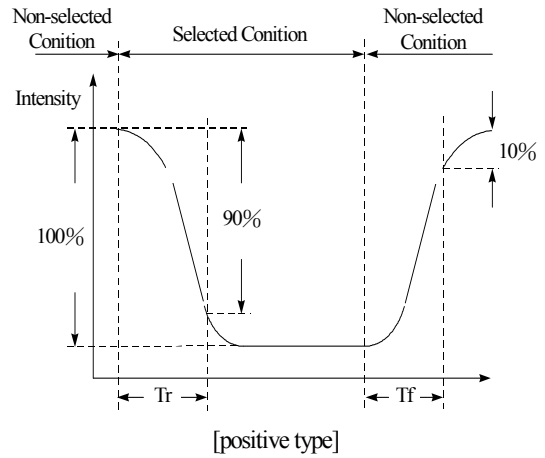
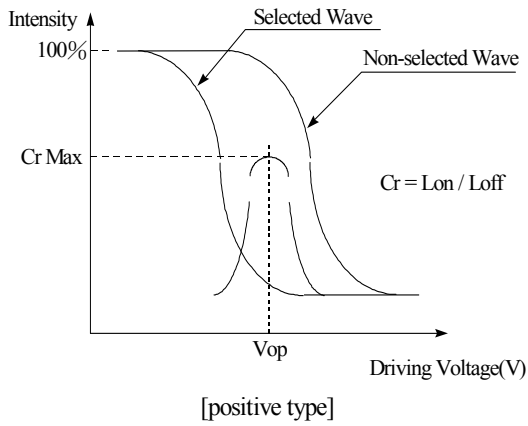
## 6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) $\theta$	$CR \geq 2$	10	—	105	deg
	(H) $\phi$	$CR \geq 2$	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	100	150	ms

	T fall	—	—	100	150	ms
--	--------	---	---	-----	-----	----

### Definition of Operation Voltage (Vop)

### Definition of Response Time (Tr, Tf)



#### Conditions :

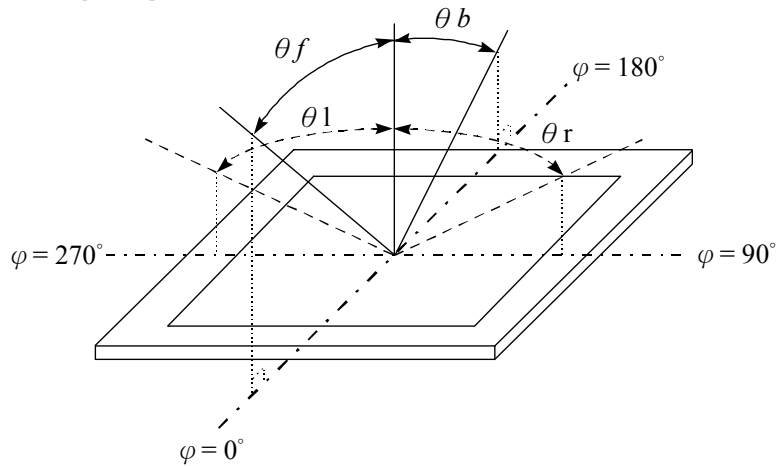
Operating Voltage : Vop

Viewing Angle( $\theta, \varphi$ ) :  $0^\circ, 0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty, 1/a bias

### Definition of viewing angle( $CR \geq 2$ )



## 7. Interface Description

Pin No.	Symbol	Level	Description
1	V <sub>ss</sub>	0V	Ground
2	V <sub>dd</sub>	5V	Power supply for logic
3	V <sub>o</sub>	(Variable)	Operating voltage for LCD
4	A0	H/L	H : Data L : Instruction
5	CS1	H/L	Chip select signal for IC1 ( left 61*32 dots ) active "H"
6	CS2	H/L	Chip select signal for IC2 ( right 61*32 dots ) active "H"
7	NC	—	NC
8	NC	—	NC

9	R/W	H/L	H : Read ; L : Write
10	DB0	H/L	Data bus
11	DB1	H/L	Data bus
12	DB2	H/L	Data bus
13	DB3	H/L	Data bus
14	DB4	H/L	Data bus
15	DB5	H/L	Data bus
16	DB6	H/L	Data bus
17	DB7	H/L	Data bus
18	RES	H/L	H -> L: The LCM be reset
19	NC	—	—
20	NC	—	—

## **8. Contour Drawing & Block Diagram**



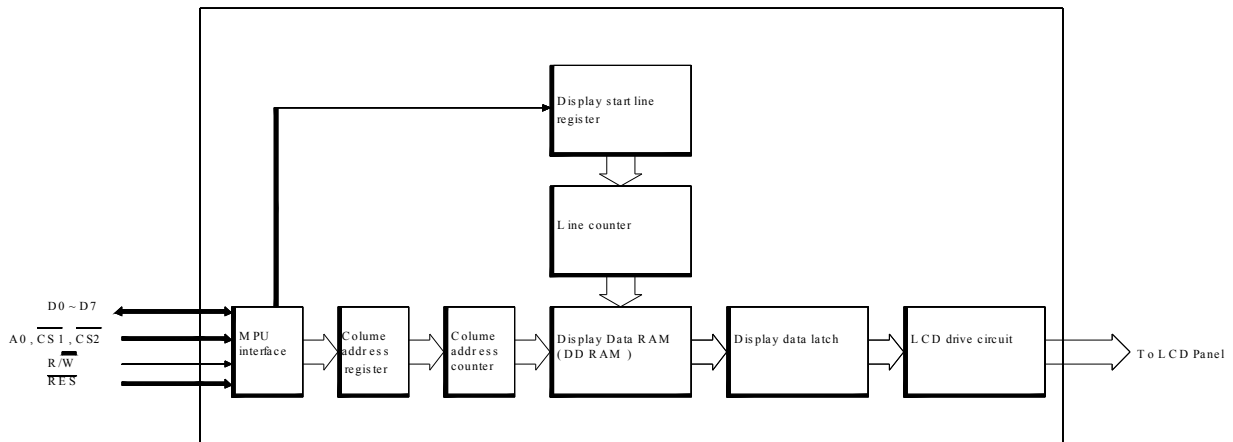
## **9.Function Description**

### **Block Diagram**

第 !! SEITE 7 頁，共 !! ANZSEITEN \\*Arabisch 錯誤! 引數選項無法識別。 頁

This 122×32 dots LCD Module built in two SED 1520 LSI controller.

## MPU interface



The SED 1520 controller transfers data via 8-bit bidirectional data buses (D0 to D7), it can fit any MPU if it corresponds to SED 1520 Read and Write Timing Characteristics.

## Data transfer

The SED1520 driver uses the A0, E and R/W signals to transfer data between the system MPU and internal registers, The combinations used are given in the table below.

A0	R/W	Function
1	1	Read display data
1	0	Write display data
0	1	Read status
0	0	Write to internal register (command)

## Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time ( $t_{CYC}$ ) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

## Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

## Column Address Counter

The column address counter is a 7-bit presentable counter that supplies the column address for



MPU access to the display data RAM. See Figure 1. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

### **Display Data RAM**

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 1

### **Page Register**

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 1. The contents of the page register are set by the Set Page Register command.



# 10. Commands Descriptions

## Summary

Command	Code											Function	
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0		
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1:ON, 0:OFF	
Display start line	0	1	0	1	1	0	Display start address (0 to 31)				0	Specifies RAM line corresponding to top line of display.	
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.	
Set column (segment) address	0	1	0	0	Column address (0 to 79)							0	Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY        1:Busy 0:Ready ADC         1:CCW output 0:CCW output ON/OFF     1:Display off 0: Display on RESET      1:Being reset 0:Normal	
Write display data	1	1	0	Write data								0	Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								0	Reads data from display RAM into data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0:CCW output, 1:CCW output	
Status drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1:Static drive, 0:Normal driving	
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD duty cycle 1:1/32, 0:1/16	
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON	
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF	
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset	

**Table 1**

Table 1 is the command table. The SED 1520 series identifies a data bus using a combination of A0 and R/W (RD or WR) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

### Display ON/OFF

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	1	0	1	1	1	D

AEH, AFH

This command turns the

display on and off.

D=1: Display ON

D=0: Display OFF

### Display Start Line

This command specifies the line address shown in Figure 1 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in

the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	0	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>

## C0H to DFH

This command loads display start line register.

A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 1.

### Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	1	1	1	0	A <sub>1</sub>	A <sub>0</sub>

## B8H to BBH

This command loads the page address register.

A <sub>1</sub>	A <sub>0</sub>	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 1

### Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>

00H to 4FH

This command loads the column address register.

A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

### Read Status

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A<sub>0</sub>=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.  
 Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.  
 Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.  
 ADC=1: Normal. Column address n→segment driver n.  
 ADC=0: Inverted. Column address 79-u→segment driver u.
- The ON/OFF bit indicates the current status of the display.  
 It is the inverse of the polarity of the display ON/OFF command.

ON/OFF=1: Display OFF

ON/OFF=0: Display ON

- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

RESET=1: Currently executing reset command.

RESET=0: Normal operation

### Write Display Data

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

### Read Display Data

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	Read data							

Read 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.

After loading a new address into the column address register one dummy read is required before valid data is obtained.

### Select ADC

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	1	0	0	0	0	D

### AOH A1H

This command selects the relationship between display data RAM column addresses and segment drivers.

D=1: SEG0←column address 4FH,.....(inverted)

D=0: SEG0←column address 00H,.....(normal)

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 1 for a table of segments and column addresses for the two values of D.

### Static Drive ON/OFF

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	1	0	0	1	0	D

### A4H A5H

Forces display on and all common outputs to be selected.

D=1: Static drive on

D=0: Static drive off

### Select Duty

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	1	0	1	0	0	D

A8H A9H

This command sets the duty cycle of the LCD drive, Please set D=1, LCD duty cycle is 1/32 duty.

### Read-Modify-Write

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	1	0	0	0	0	0

### E0H

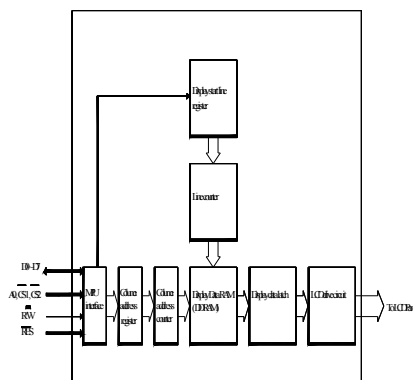
This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

\* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.

No.	Defect	Judgment Criterion	Partition																				
1	Spots	<p>A)Clear</p> <table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.1</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.1 &lt; d \leq 0.2</math></td> <td>6</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>0.3 &lt; d</math></td> <td>0</td> </tr> </tbody> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear</p> <table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.2</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.5</math></td> <td>6</td> </tr> <tr> <td><math>0.5 &lt; d \leq 0.7</math></td> <td>2</td> </tr> <tr> <td><math>0.7 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size: d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size: d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	6																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						
2	Bubbles in Polarize	<table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.3</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.3 &lt; d \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>1.0 &lt; d \leq 1.5</math></td> <td>1</td> </tr> <tr> <td><math>1.5 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size: d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor										
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.3$	Disregard																						
$0.3 < d \leq 1.0$	3																						
$1.0 < d \leq 1.5$	1																						
$1.5 < d$	0																						
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor																				
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor																				
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor																				



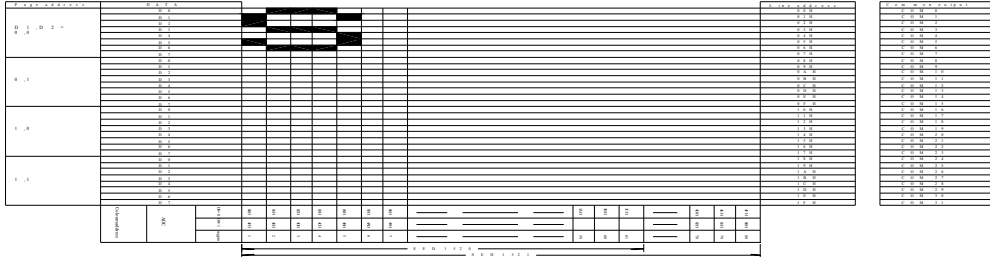
End



A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	1	0	1	1	1	0

## EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



## Reset

A <sub>0</sub>	R/W	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	1	0	0	0	1	0

## E2H

This command clears

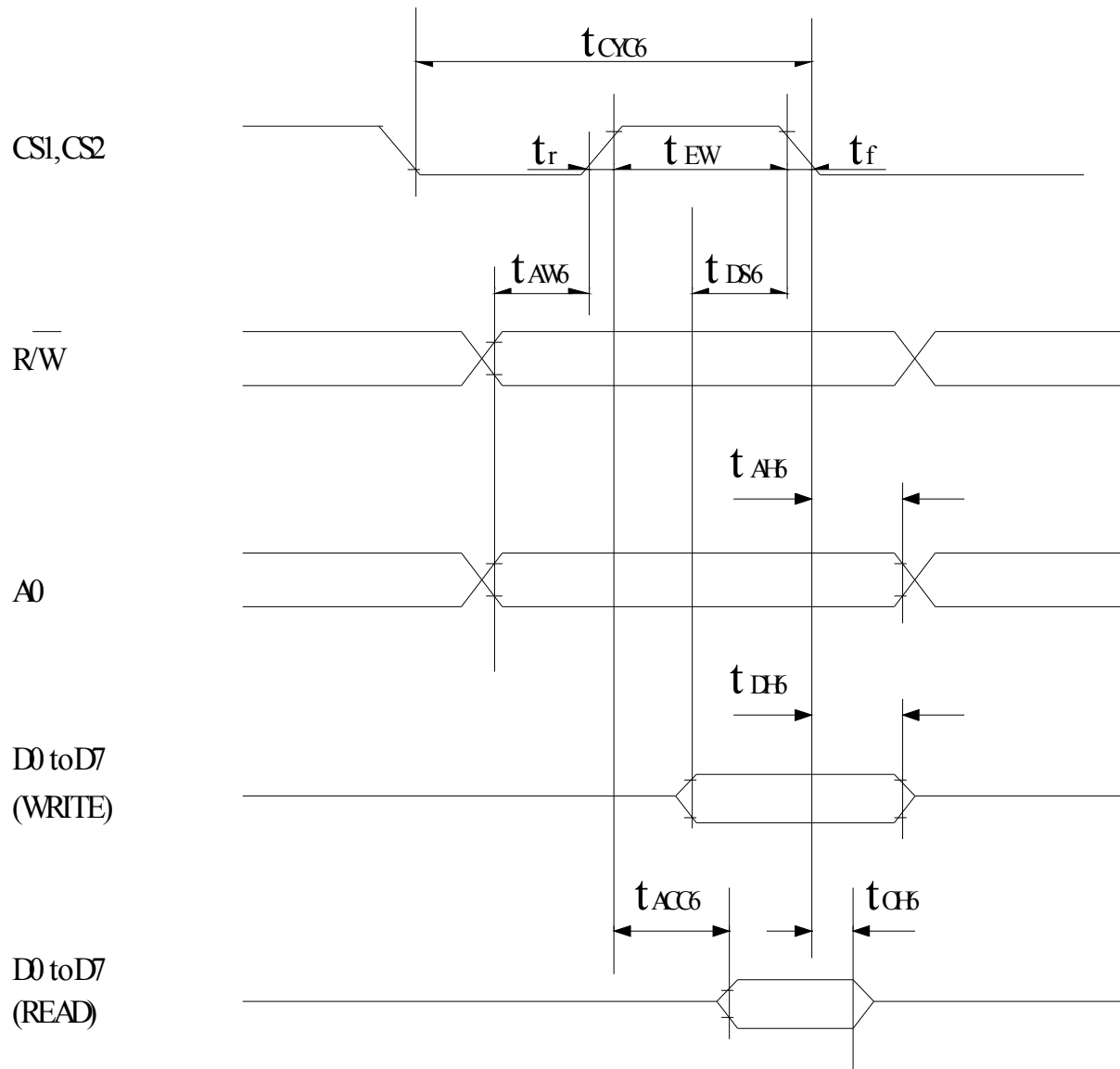
- the display start line register.
- And set page address register to 3 page.

It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the RES pin. The Reset command cannot be used instead of this Reset signal.

# 11. Timing Characteristics

MPU Bus Read/Write II (68-family MPU)



Ta=-20 to 75 deg. C, V<sub>dd</sub>=5V±10 unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
<b>System cycle time</b>	<b>t<sub>CYC6</sub></b>	—	<b>1000</b>	—	<b>ns</b>	<b>A0,R/W</b>
<b>Address setup time</b>	<b>t<sub>AW6</sub></b>	—	<b>20</b>	—	<b>ns</b>	
<b>Address hold time</b>	<b>t<sub>AH6</sub></b>	—	<b>10</b>	—	<b>ns</b>	

Data setup time	t <sub>DS6</sub>	—	80	—	ns	D0 to D7
Data hold time	t <sub>DH6</sub>	—	10	—	ns	
Output disable time	t <sub>OH6</sub>	CL=100pF	10	60	ns	
Access time	t <sub>ACC6</sub>		—	90	ns	
Enable pulsewidth	Read	t <sub>EW</sub>	—	100	—	CS
	Write		—	80	—	
Rise and fall time	tr, tf	—	—	15	ns	—

(V<sub>dd</sub>=2.7 to 4.5 V, Ta=-20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
System cycle time	t <sub>CYC6</sub>	—	2000	—	ns	A0,R/W
Address setup time	t <sub>AW6</sub>	—	40	—	ns	
Address hold time	t <sub>AH6</sub>	—	20	—	ns	
Data setup time	t <sub>DS6</sub>	—	160	—	ns	D0 to D7
Data hold time	t <sub>DH6</sub>	—	20	—	ns	
Output disable time	t <sub>OH6</sub>	CL=100pF	20	120	ns	
Access time	t <sub>ACC6</sub>		—	180	ns	
Enable pulsewidth	Read	t <sub>EW</sub>	—	200	—	CS
	Write		—	160	—	
Rise and fall time	tr, tf	—	—	15	ns	—

## 12. Quality Assurance

Screen Cosmetic Criteria

## 13. Reliability

Content of Reliability Test

Environmental Test

Test Item

Content of Test

Test Condition

Applicable

Standard

**High Temperature storage**

**Endurance test applying the high storage temperature for a long time.**

60°C

200hrs

—

**Low Temperature**

**storage**

**Endurance test applying the high storage temperature for a long time.**

-10°C

200hrs

—

**High Temperature**

**Operation**

**Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.**

50°C

200hrs

—

**Low Temperature**

**Operation**

**Endurance test applying the electric stress under low temperature for a long time.**

0°C

200hrs

—

**High Temperature/**

**Humidity Storage**

**Endurance test applying the high temperature and high humidity storage for a long time.**

60°C,90%RH

96hrs

—

**High Temperature/**

**Humidity Operation**

**Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.**

50°C,90%RH

96hrs

—

**Temperature Cycle**

**Endurance test applying the low and high temperature cycle.**

-10°C    25°C    60°C

30min    5min    30min

1 cycle

-10°C/60°C

10 cycles

—

\*\*\*Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C