1Gb DDR3 SDRAM

Lead-Free&Halogen-Free

(RoHS Compliant)

H5TQ1G63DFR

hynix

Revision History

Revision No.	History	Page	Date	Remark
0.01	Preliminary Initial Release	-	Apr. 2010	Preliminary
1.0	Corrected Features (added CWL 10) Corrected IDD Timing Added IDD value Added Input/output Capacitance Corrected Speed Bin data Corrected CWL value Corrected typo at table 32 Added value at table 40 Corrected AC timing values	3 13 23/24 25 26 ~ 28 48 129 134 151 ~ 156	Sep. 2010	
1.1	Corrected Features (added CL 12,13) Corrected IDD wording (Slow and Fast Exit)	3 23	Jan. 2011	

1. Description

The H5TQ1G63DFR-xxx series are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

1.1 Device Features and Ordering Information

1.1.1 FEATURES

- DQ Power & Power supply : VDD & VDDQ = 1.5V +/- 0.075V
- DQ Ground supply : VSSQ = Ground
- Fully differential clock inputs (CK, $\overline{CK}$) operation
- Differential Data Strobe (DQS, $\overline{DQS}$)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, 10, 11, 12 and 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8,9 and 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Programmable PASR(Partial Array Self-Refresh) for Digital consumer Applications.
- Programmable BL=4 supported (tCCD=2CLK) for Digital consumer Applications.
- Programmable ZQ calibration supported
- BL switch on the fly
- 8banks
- 8K refresh cycles/64ms
- JEDEC standard 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- Auto Self Refresh supported
- Write Levelization supported
- On Die Thermal Sensor supported
- 8 bit pre-fetch

*** This product in compliance with the RoHS directive.**

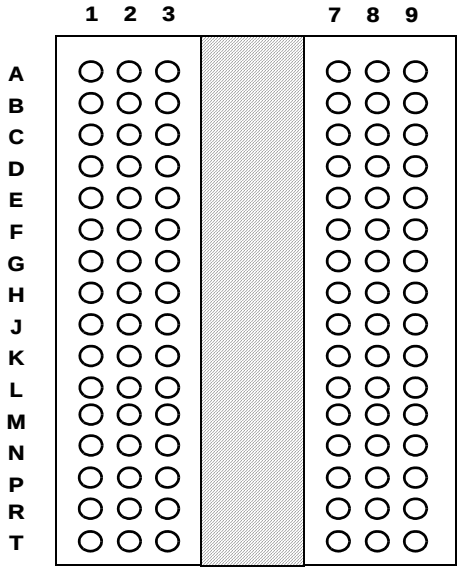
1.1.2 ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
H5TQ1G63DFR-12C	VDD/VDDQ=1.5 V	800MHz	1.6Gbps/pin	SSTL-15	96ball FBGA
H5TQ1G63DFR-11C		900MHz	1.8Gbps/pin		
H5TQ1G63DFR-N0C		1.0GHz	2.0Gbps/pin		

1.2 Package Ballout / Mechanical Dimension

x16 Package Ball out (Top view): 96ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				$\overline{\text{DQSU}}$	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	$\overline{\text{DQSL}}$				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	J
K	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				A15	VREFCA	VSS	M
N	VDD	A3	A0				A12/$\overline{\text{BC}}$	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	$\overline{\text{RESET}}$	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	



(Top View: See the balls through the Package)

○ Populated ball

+ Ball not populated

1.3 ROW AND COLUMN ADDRESS TABLE

1Gb

Configuration	64Mb x 16
# of Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BL switch on the fly	A12/$\overline{BC}$
Row Address	A0 - A12
Column Address	A0 - A9
Page size [1]	2 KB

Note1: Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS}$ * ORG ÷ 8

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

1.4 Pin Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$, ($\overline{CS0}$), ($\overline{CS1}$), ($\overline{CS2}$), ($\overline{CS3}$)	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{RAS}$. $\overline{CAS}$. $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.

Symbol	Type	Function
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{\text{TDQS}}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{\text{BC}}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{\text{BC}}$	Input	Burst Chop: A12 / $\overline{\text{BC}}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, $\overline{\text{DQS}}$, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, and DQSU are paired with differential signals $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, and $\overline{\text{DQSU}}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		No Connect: No internal electrical connection is present.
NF		No Function
V_{DDQ}	Supply	DQ Power Supply: 1.5V +/- 0.075V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5V +/- 0.075V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Symbol	Type	Function

Note:
Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, DM, and $\overline{RESET}$) do not supply termination.

2. Absolute Maximum Ratings

2.1 Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^{o}C	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

3. Operating Conditions

3.1 DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1,2
	Extended Temperature Range (Optional)	85 to 95	^{o}C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85^{o}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{o}C and 95^{o}C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

3.2 Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

4. IDD and IDDQ Specification Parameters and Test Conditions

4.1 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(min)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

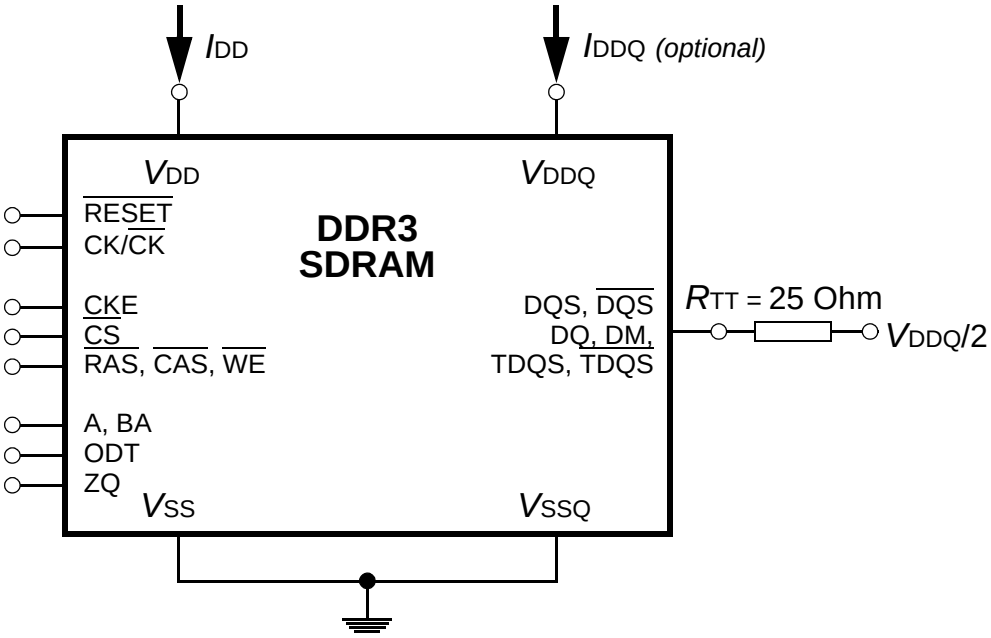


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above]

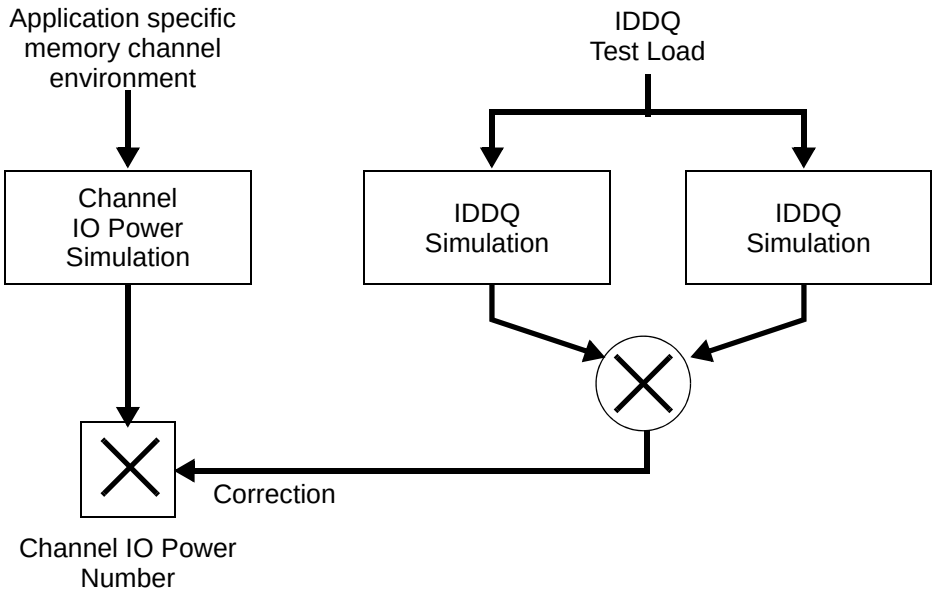


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol	800MHz	900MHz	1.0GHz	Unit
t_{CK}	1.25	1.1	1	ns
CL	10	12	13	nCK
n_{RCD}	12	14	16	nCK
n_{RC}	40	46	52	nCK
n_{RAS}	30	34	37	nCK
n_{RP}	12	14	16	nCK
n_{FAW}	34	38	40	nCK
n_{RRD}	7	7	7	nCK
n_{RFC}-1 Gb	88	100	110	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 3.
I_{DD1}	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 4.
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 5.

Symbol	Description
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DDQ2NT} (optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c)]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c)]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0
I_{DDQ4R} (optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nREC (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Normal[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID-LEVEL
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Extended[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID-LEVEL

Symbol	Description
I_{DD6TC}	Auto Self-Refresh Current T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a][f]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC+1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC+1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCD - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until 2* nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-27	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 7 - IDD4R and IDDQ24RMeasurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

4.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} Specification

Speed Grade Bin	800MHz	900MHz	1.0GHz	Unit
Symbol	**Max.**	**Max.**	**Max.**	
I_{DD0}	60	65	70	mA
I_{DD1}	70	75	80	mA
I_{DD2P} (0) slow exit	10	10	10	mA
I_{DD2P} (1) fast exit	20	20	20	mA
I_{DD2N}	30	30	30	mA
I_{DD2Q}	30	30	35	mA
I_{DD3P} (fast exit)	25	25	30	mA
I_{DD3N}	45	45	50	mA
I_{DD4R}	150	170	180	mA
I_{DD4W}	150	170	180	mA
I_{DD5}	130	150	160	mA
I_{DD6}	10	10	10	mA
I_{DD7}	200	220	240	mA

4.2.1 IDD6TC Specification

Symbol	Temperature Range	Value	Unit	Notes
		900MHz		
I_{DD6}	0 - 85 ^{o}C	**10**	mA	2,3
I_{DD6ET}	0 - 95 ^{o}C	**10**	mA	4,5
I_{DD6TC}	0 ^{o}C ~ T_a	**10**	mA	5,6,7

1. Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
2. Applicable for MR2 settings A6=0 and A7=0.
3. Supplier data sheets include a max value for IDD6.
4. Applicable for MR2 settings A6=0 and A7=1. IDD6ET is only specified for devices which support the Extended Temperature Range feature.
5. Refer to the supplier data sheet for the value specification method (e.g. max, typical) for IDD6ET and IDD6TC
6. Applicable for MR2 settings A6=1 and A7=0. IDD6TC is only specified for devices which support the Auto Self Refresh feature.
7. The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of TOPER. Refer to supplier data sheet for more information.

5. Input/Output Capacitance

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	C_{IO}	1.5	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input capacitance, CK and $\overline{CK}$	C_{CK}	0.8	1.4	0.8	1.3	0.8	1.3	pF	2,3
Input capacitance delta CK and $\overline{CK}$	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	C_I	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,6
Input capacitance delta, DQS and $\overline{DQS}$	C_{DDQS}	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9, 10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$,TDQS, $\overline{TDQS}$)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C_{ZQ}	-	3	-	3	-	3	pF	2,3,12

Notes:

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, $\overline{RESET}$ and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-$C_{\overline{CK}}$.
5. The minimum C_{CK} will be equal to the minimum C_I.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CTRL pins defined as ODT, CS and CKE.
8. C_{DI_CTRL}=C_I(CNTL) - 0.5 * C_I(CLK) + C_I($\overline{CLK}$))
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I($\overline{CLK}$))
11. C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}($\overline{DQS}$))
12. Maximum external load capacitance on ZQ pin: 5 pF.

6. Standard Speed Bins

DDR3L SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

800MHz Speed Bins

Speed Bin			800MHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	12.5	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	-	ns	
PRE command period		t_{RP}	15	-	ns	
ACT to ACT or REF command period		t_{RC}	50	-	ns	
ACT to PRE command period		t_{RAS}	37.5	9*tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3	3.3	ns	1,2,3,4,8
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7,8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL=11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,8
Supported CL Settings			5, 6, 7, 8, 9, 10,11		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

900MHz Speed Bins

Speed Bin			900MHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.2	20	ns	
ACT to internal read or write delay time		t_{RCD}	15.4	-	ns	
PRE command period		t_{RP}	15.4	-	ns	
ACT to ACT or REF command period		t_{RC}	50.6	-	ns	
ACT to PRE command period		t_{RAS}	37.4	9*tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 6, 7, 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL=11	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL=12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.1	1.25	ns	1,2,3,4
Supported CL Settings			6, 7, 8, 9, 10,11, 12		n_{CK}	
Supported CWL Settings			5, 6, 7,8,9		n_{CK}	

1.0GHz Speed Bins

Speed Bin			1.0GHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13	20	ns	
ACT to internal read or write delay time		t_{RCD}	16	-	ns	
PRE command period		t_{RP}	16	-	ns	
ACT to ACT or REF command period		t_{RC}	52	-	ns	
ACT to PRE command period		t_{RAS}	37	9*tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 6, 7, 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL=11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL=12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.0	1.25	ns	1,2,3,4
CL=13	CWL = 5,6,7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 10	$t_{CK(AVG)}$	0.935	1.0	ns	1,2,3,5,8
Supported CL Settings			6, 7, 8, 9, 10,11, 12, 13		n_{CK}	
Supported CWL Settings			5, 6, 7,8,9,10		n_{CK}	

Speed Bin Table Notes

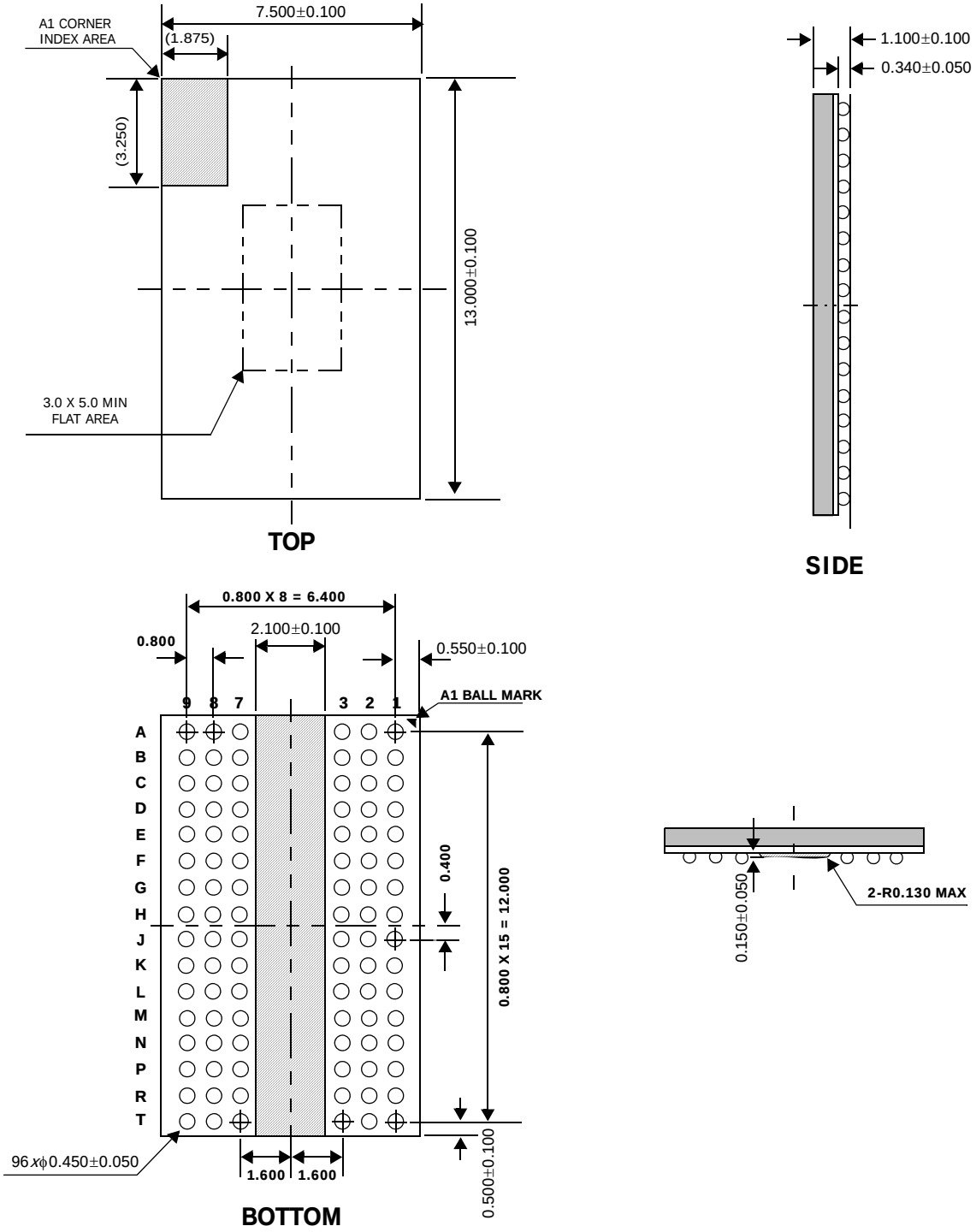
Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK (AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK (AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK (AVG) = tAA.MAX / CLSELECTED and round the resulting tCK (AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns or lower. SPD settings must be programmed to match.
   For example,
   DDR3-1333H9 devices supporting down binning to DDR3-1066G7 should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20).
   DDR3-1600PB devices supporting down binning to DDR3-1333H9 or DDR3-1066G7 should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accodingly.
   For example,
   49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H9 and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600PB.
10. DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
11. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.

Package Dimensions

Package Dimension(x16); 96Ball Fine Pitch Ball Grid Array Outline



hynix

DDR3 SDRAM

Device Operation

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1. Functional Description

1.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

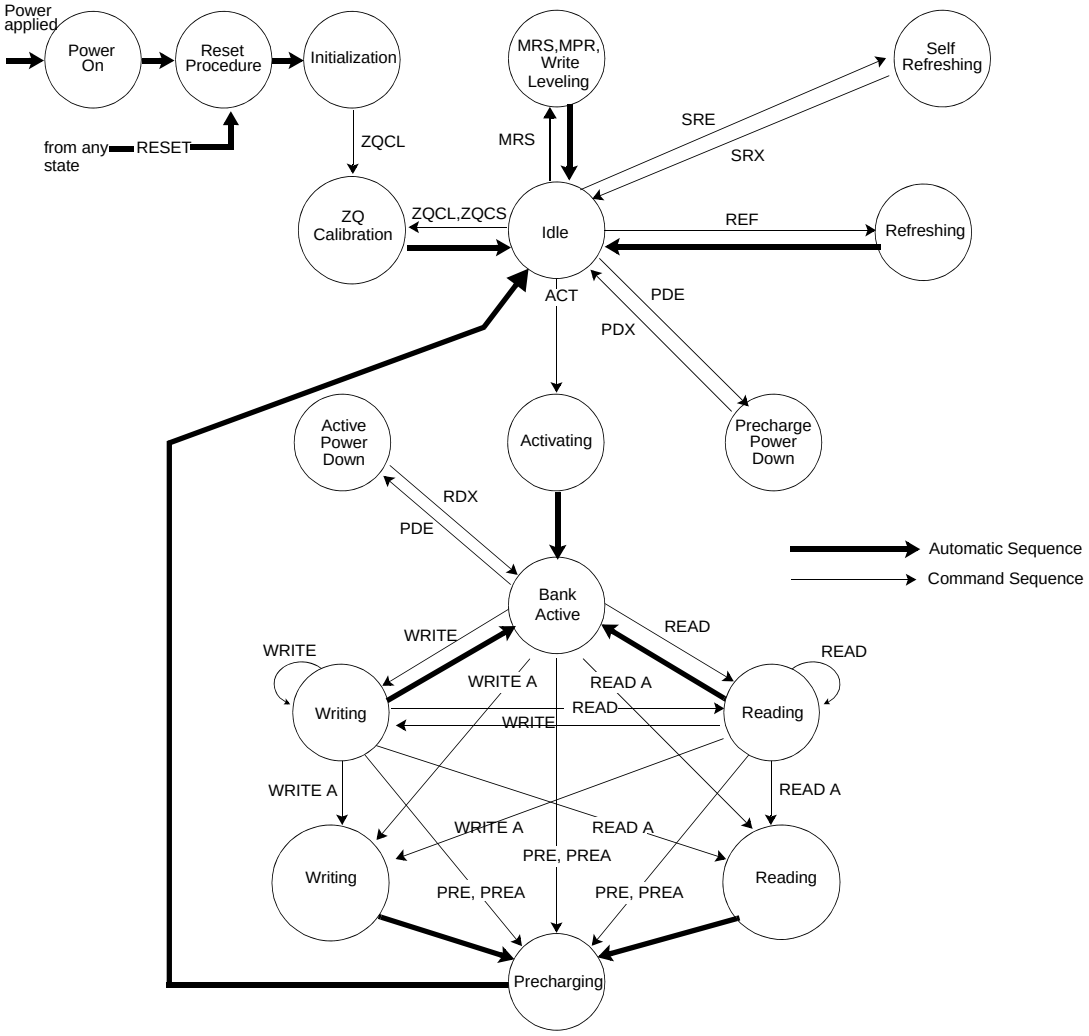


Figure 3. Simplified State Diagram

Table 11. State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

Note: See ?$paratext>? on page 50for more details.

1.2 Basic Functionality

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" in each datasheet for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

1.3 RESET and Initialization Procedure

1.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET is recommended to be maintained below 0.2x VDD, (all other inputs may be undefined). RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDD min must be no greater than 200 ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

     OR

   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be large than or equal to VSSQ and VSS on the other side.
2. After RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR = max (tXS; 5 x tCK)

6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)

7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)

8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-BA2).

9. Issue MRS Command to load MR0 with all application settings and "DLL reset" (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.

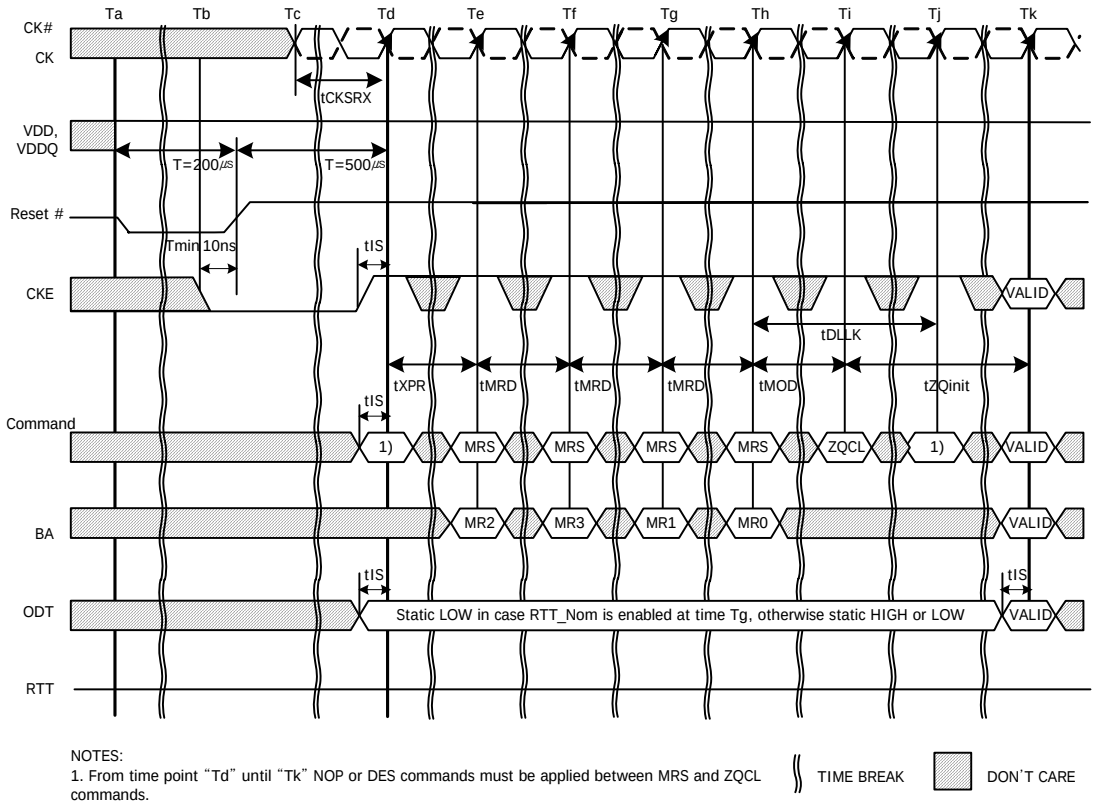


Figure 4. Reset and Initialization Sequence at Power-on Ramping

1.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2* VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled “LOW” before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

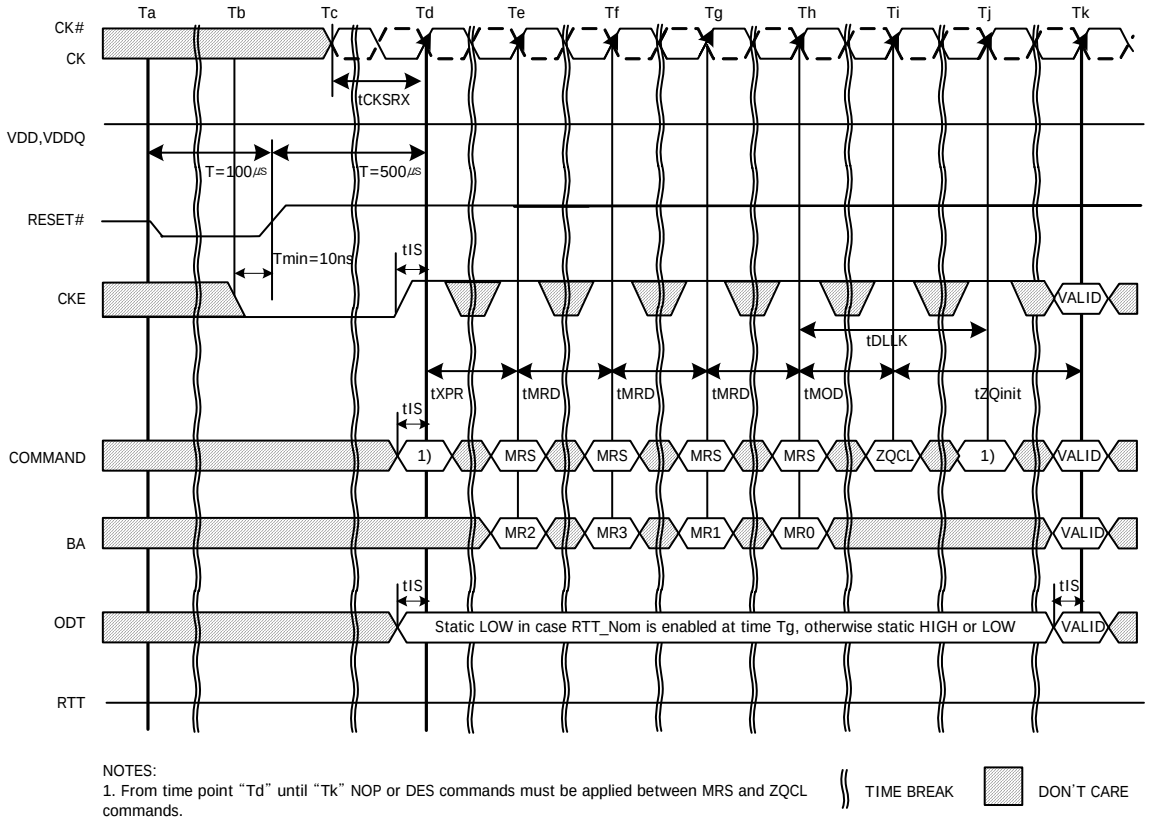


Figure 5. Reset Procedure at Power Stable Condition

1.4 Register Definition

1.4.1 Programming the Mode Registers

For application flexibility, various functions, features and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power-up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 6.

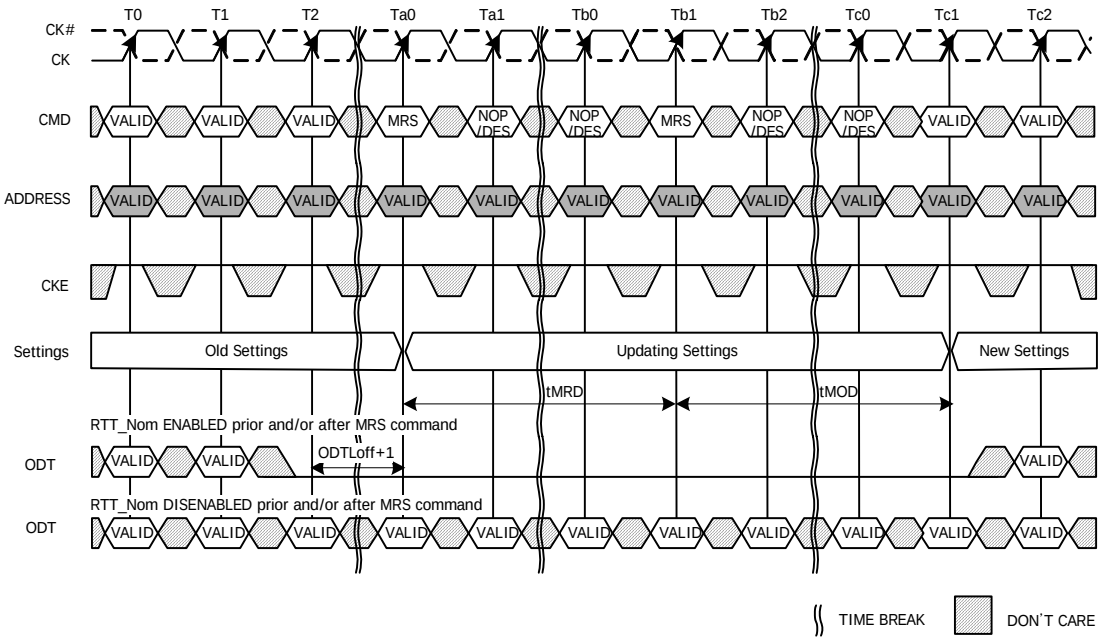


Figure 6. tMRD Timing

The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, except DLL reset, add is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 7.

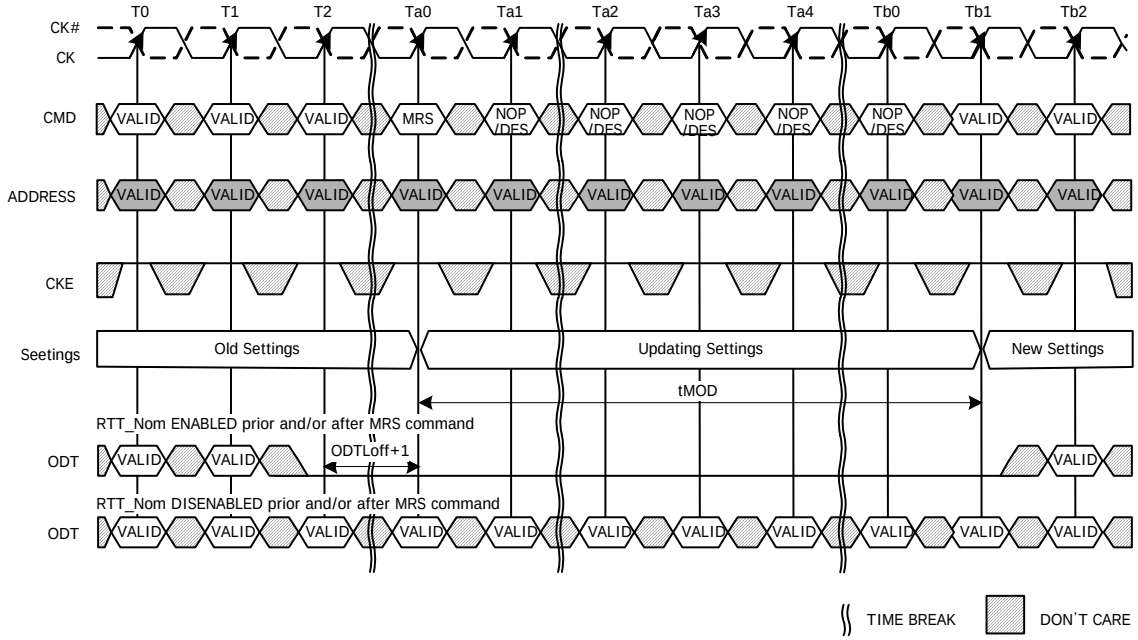
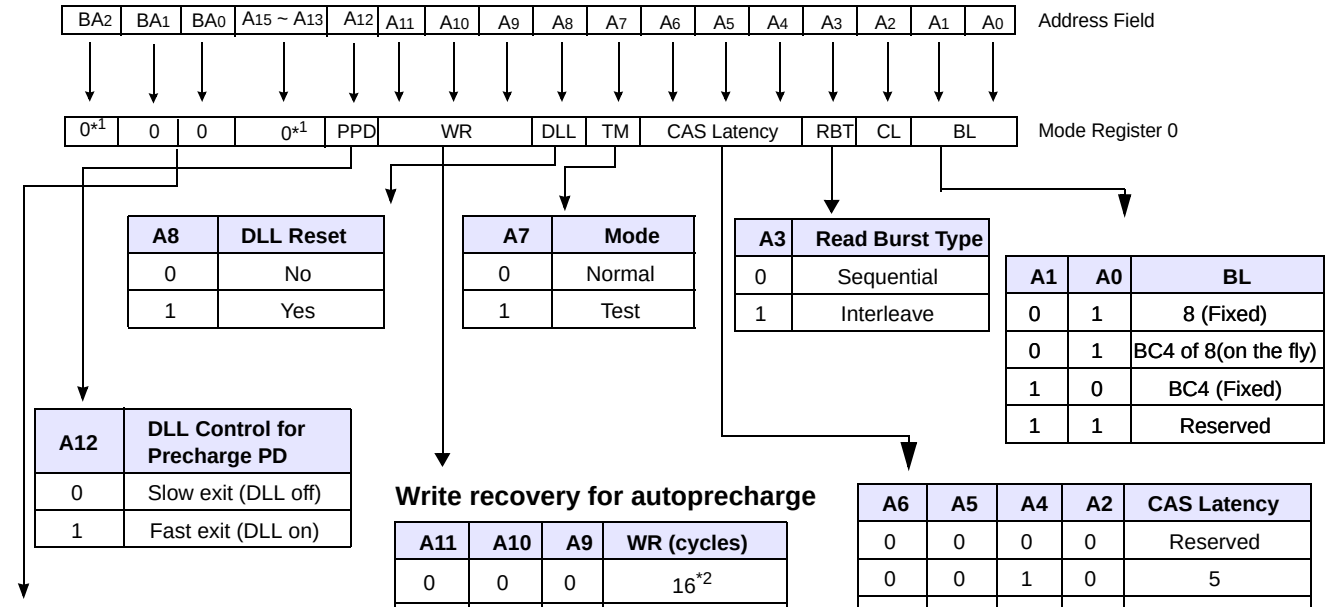


Figure 7. tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off Stated prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

1.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0, BA1, and BA2, while controlling the states of address pins according to Figure 8.



A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Sequential
1	Interleave

A1	A0	BL
0	1	8 (Fixed)
0	1	BC4 of 8(on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR (cycles)
0	0	0	16*2
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

*1: BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.
*2: WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
*3: The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency.
*4: The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timingtable.

Figure 8. DDR3 SDRAM mode register set (MR0)

1.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 8. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 12. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Table 12. Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

1.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 8. CAs Latency is the delay, is clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins” on each datasheet. For detailed Read operation refer to ?$paratext>? on page 74.

1.4.2.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 8. Programming bit A7 to a ‘1’ places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

1.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of ‘0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations).

1.4.2.5 Write Recovery

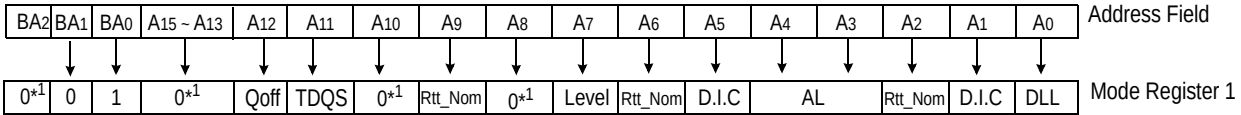
The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR must be programmed to be equal to or larger than tWR (min).

1.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or ‘slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

1.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 9.



A11	TDQS enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom*3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240Ω

A0	DLL Enable
0	Enable
1	Disable

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

*3: In Write leveling Mode (MR1[bit7]=1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7]=1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ4 and RZQ/6 are allowed.
*4: If RTT_Nom is used during Writes, only the values RZQ/2,RZQ/4 and RZQ/6 are allowed.

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled*2

*2: Outputs disabled - DQs, DQSs, $\overline{DQSs}$.

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note: RZQ= 240Ω

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1: BA2 and A8, A10, and A13~A15 are RFU and must be programmed to 0 during MRS.

Figure 9. MR1 Definition

1.4.3.1 DLL Enable/Disable

MR1 (A0=0), the DLL is automatically disabled when entering Sefl-Refresh operation and is automatically re-enabled upon eixt of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to ?$paratext>? on page 55.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering in the ODT pin low and/or by programming the RTT_Nom bits MR1 {A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10,A9} = {0,0}, to disable Dynamic ODT externally.

1.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 9.

1.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

1.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 13.

Table 13. Additive Latency (AL) Settings

A4	A3	AL
0	1	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note: AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register

1.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See ?$paratext>? on page 60 for more details.

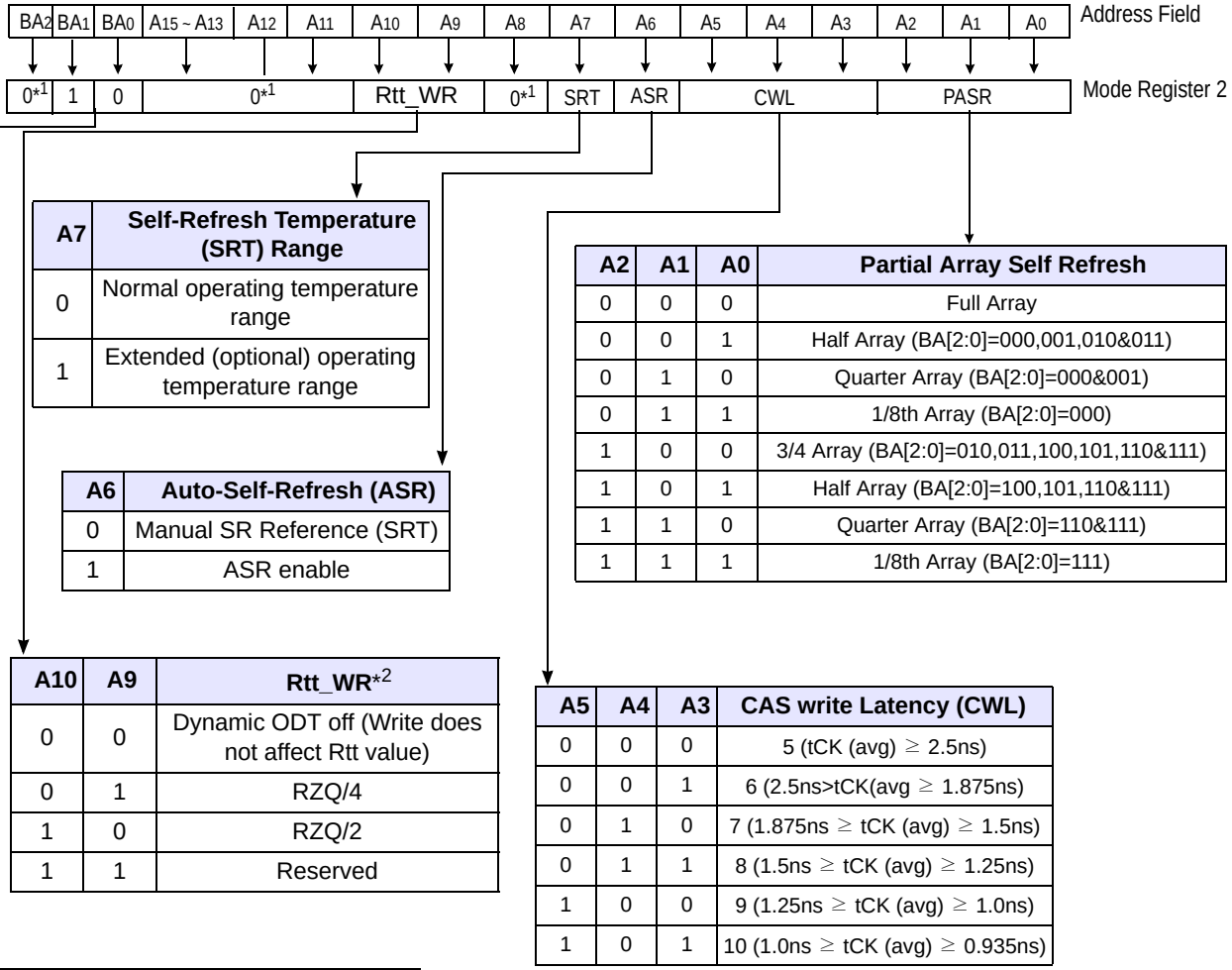
1.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 9. When this feature is enabled (A12=1), all output pins (DQs, DQS, DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

1.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS, RAS, CAS, We, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Programming:



A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A6	Auto-Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	A1	A0	Partial Array Self Refresh
0	0	0	Full Array
0	0	1	Half Array (BA[2:0]=000,001,010&011)
0	1	0	Quarter Array (BA[2:0]=000&001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110&111)
1	0	1	Half Array (BA[2:0]=100,101,110&111)
1	1	0	Quarter Array (BA[2:0]=110&111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK (avg) ≥ 2.5ns)
0	0	1	6 (2.5ns>tCK(avg ≥ 1.875ns)
0	1	0	7 (1.875ns ≥ tCK (avg) ≥ 1.5ns)
0	1	1	8 (1.5ns ≥ tCK (avg) ≥ 1.25ns)
1	0	0	9 (1.25ns ≥ tCK (avg) ≥ 1.0ns)
1	0	1	10 (1.0ns ≥ tCK (avg) ≥ 0.935ns)

*1: BA2, A5, A8, A11~A15 are RFU and must be programmed to 0 during MRS.
*2: The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Figure 10. MR2 Definition

1.4.4.1 Partial Array Self-Refresh (PASR)

For Hynix DDR3 SDRAM If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 10 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

1.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 10. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to “Standard Speed Bin” on each datasheet. For detailed Write operationrefer to ?$paratext>? on page 85.

1.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

For more details refer to ?$paratext>? on page 64. Hynix DDR3 SDRAMs support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

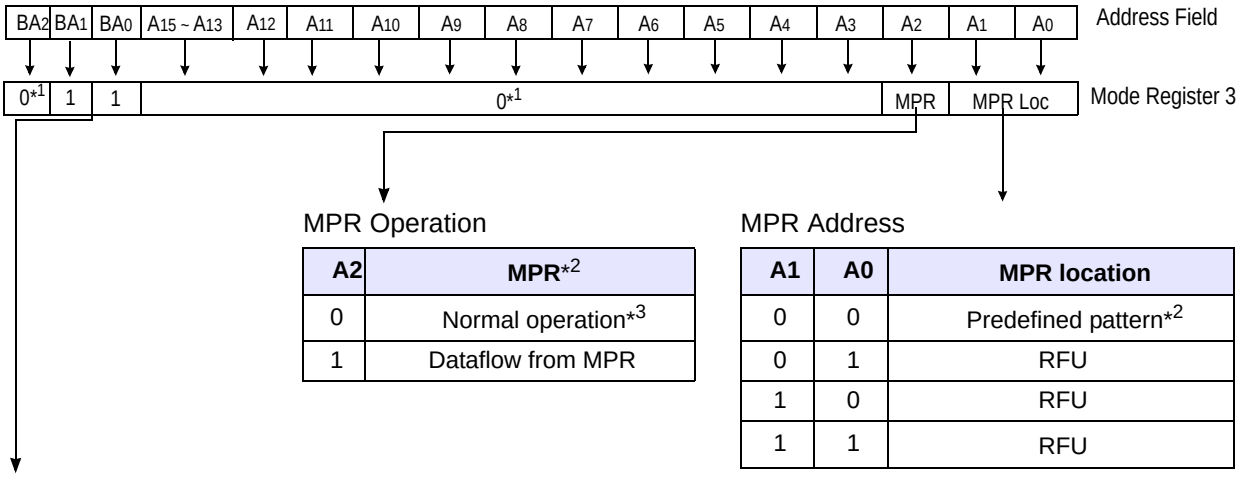
1.4.4.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to ?$paratext>? on page 112.

1.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming:



MPR Operation

A2	MPR*2
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1: BA2, A3-A15 are RFU and must be programmed to 0 during MRS.
*2: The predefined pattern will be used for read synchronization.
*3: When MPR control is set for normal operation (MR3 A[2]=0) then MR3 A[1:0] will be ignored.

Figure 11. MR3 Definition

1.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled(MR3 bit A2=0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to ?$paratext>? on page 66.

2. DDR3 SDRAM Command Description and Operation

2.1 Command Truth Table

(a) note 1,2,3,4 apply to the entire Command Truth Table
(b) Note 5 applies to all Read/Write commands
[BA = Bank Address, RA = Row Address, CA = Column Address, $\overline{BC}$ = Burst Chop, X = Don't Care, V = Valid]

Table 14. Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA2	A113-A15	A12-$\overline{BC}$	A10-AP	A10-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write(BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write(BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA2	A113-A15	A12-$\overline{BC}$	A10-AP	A10-A9, A11	Notes
		Previous Cycle	Current Cycle										
Write with Auto pre-charge (BC 4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto pre-charge (BL 8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8orBC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read(BC4, on the fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read(BL8, on the fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Pre-charge (BC4, on the fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Pre-charge (BL4, on the fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

2.2 CKE Truth Table

a) Notes 1-7 apply to the entire CKE Truth Table.
b) For Power-down entry and exit parameters See ?$paratext>? on page 98.
c) CKE low is allowed only if tMRD and tMOD are satisfied.

Table 15. CKE Truth Table

Current State[2]	CKE		Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11

1. CKE(N) is the logic state of CKE at clock edge N; CKE(N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after DESELECT only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See ?$paratext>? on page 96 and See ?$paratext>? on page 98.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operaion.VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self-Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self-Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Current State[2]	CKE		Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See ?$paratext>? on page 50.					10

1. CKE(N) is the logic state of CKE at clock edge N; CKE(N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after DESELECT only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See ?$paratext>? on page 96 and See ?$paratext>? on page 98.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operaion.VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self-Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self-Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

2.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{CS}$ LOW and $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

2.4 Deselect Command

The DESELECT function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

2.5 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit is set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to ?$paratext>? on page 58.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation are shown at following Timing Diagram (CL=6, BL=8):

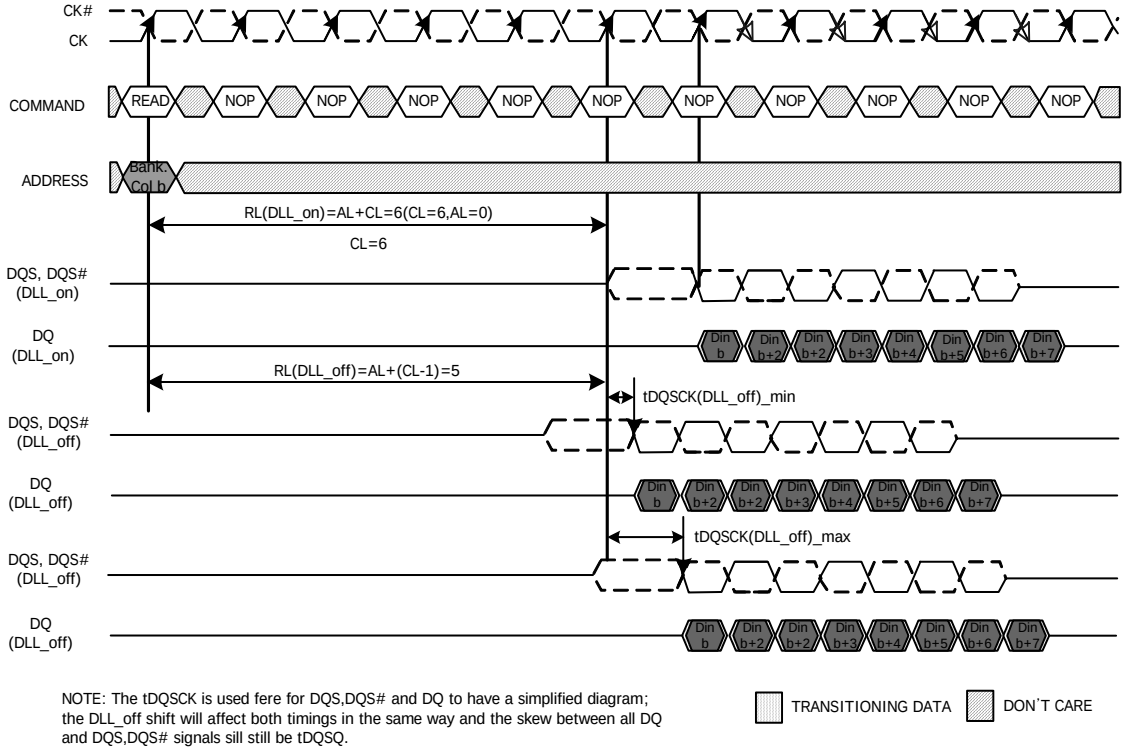


Figure 12. DLL_off mode READ Timing Operation

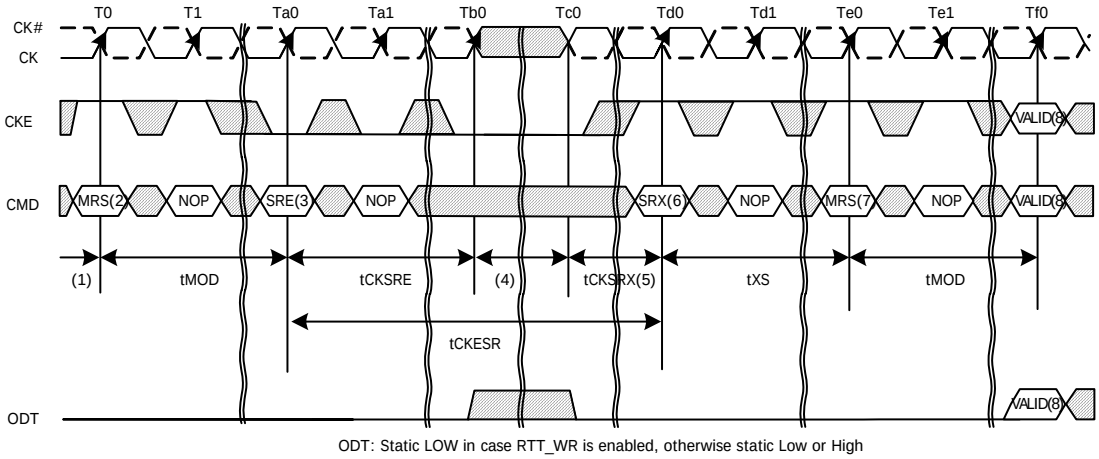
2.6 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit is set back to “0”.

2.6.1 DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).
2. Set MR1 bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with '2.7 Input clock frequency change' on page 58.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.



NOTES:
1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR1 Bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

Figure 13. DLL Switch Sequence from DLL-on to DLL-off

2.6.2 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required the frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with '2.7 Input clock frequency change' on page 58.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to “0” to enable the DLL.
7. Wait tMRD, then set MR1 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

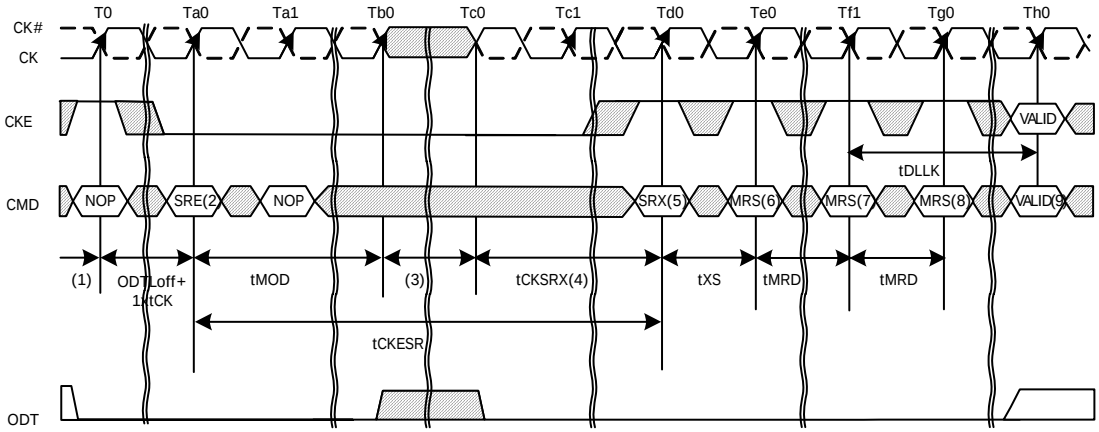


Figure 14. DLL Switch Sequence from DLL Off to DLL On

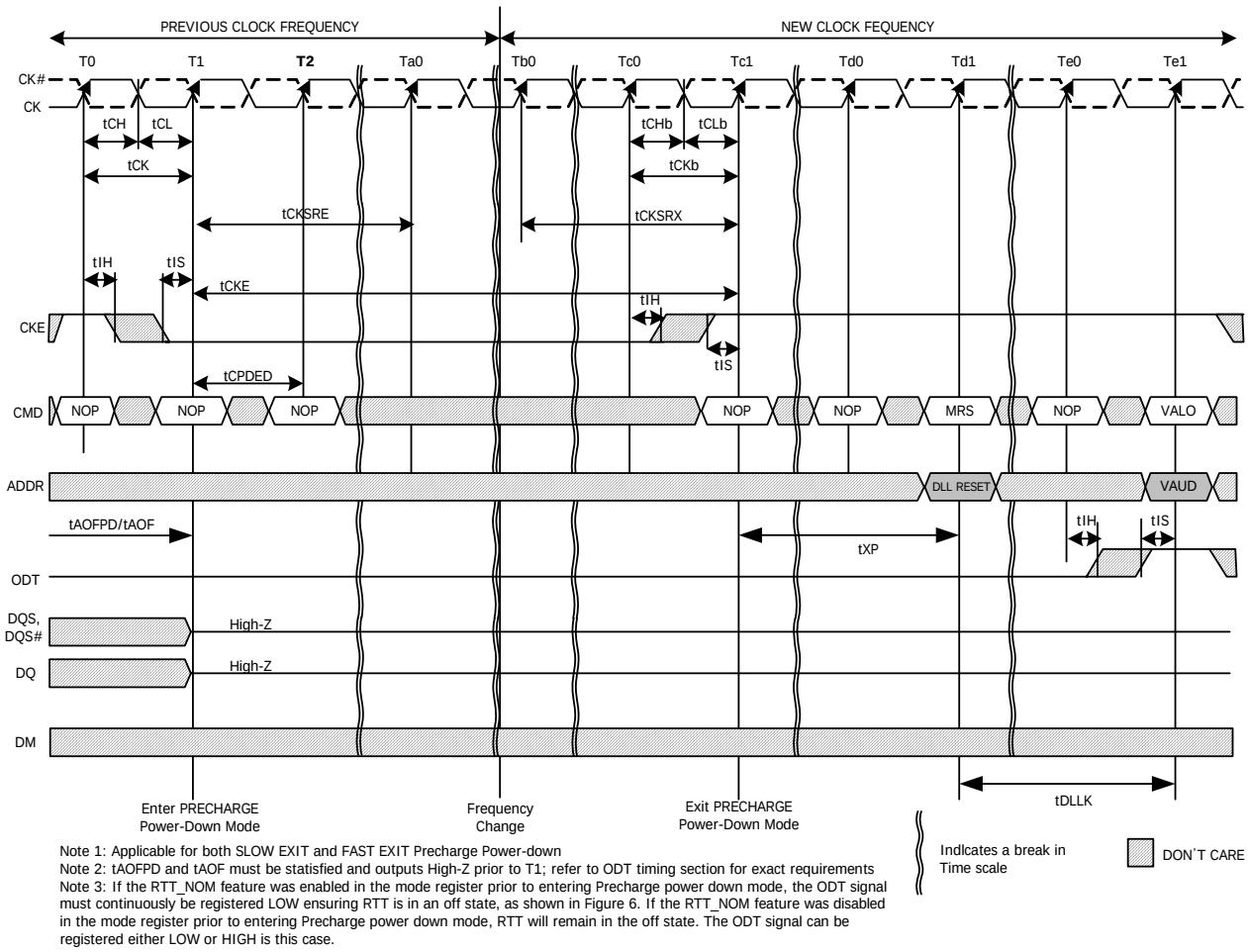
2.7 Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mod and (2) precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and ^{t}CKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See ?$paratext>? on page 96. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on-mode->DLL_off-mode transition sequence, refer to ?$paratext>? on page 56.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of ^{t}CKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM ^{t}CKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 15 on page 59.



Note 1: Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
Note 2: tAOFPD and tAOF must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements
Note 3: If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 6. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH is this case.

Figure 15. Change Frequency during Precharge Power-down

2.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS-DQS to CK-CK relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS-DQS to align the rising edge of DQS-DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK-CK, sampled with the rising edge of DQS-DQS, through the DQ bus. The controller repeatedly delays DQS-DQS until a transition from 0 to 1 is detected. The DQS-DQS delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS-DQS signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 16.

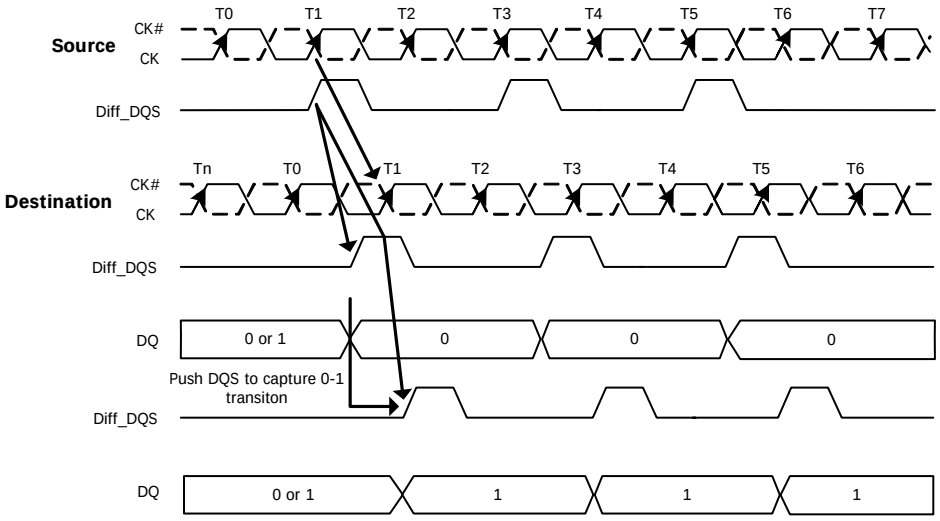


Figure 16. Write Leveling Concept

DQS-DQS driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4,X8 and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to clock relationship.

2.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 16). Note that in write leveling mode, only DQS/DQS terminations are activated and deactivated via ODT pin, unlike normal operation (Table 17).

Table 16. MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 17. DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/$\overline{\text{DQS}}$ termination	DQs Termination
De-asserted	Off	Off
Asserted	On	Off

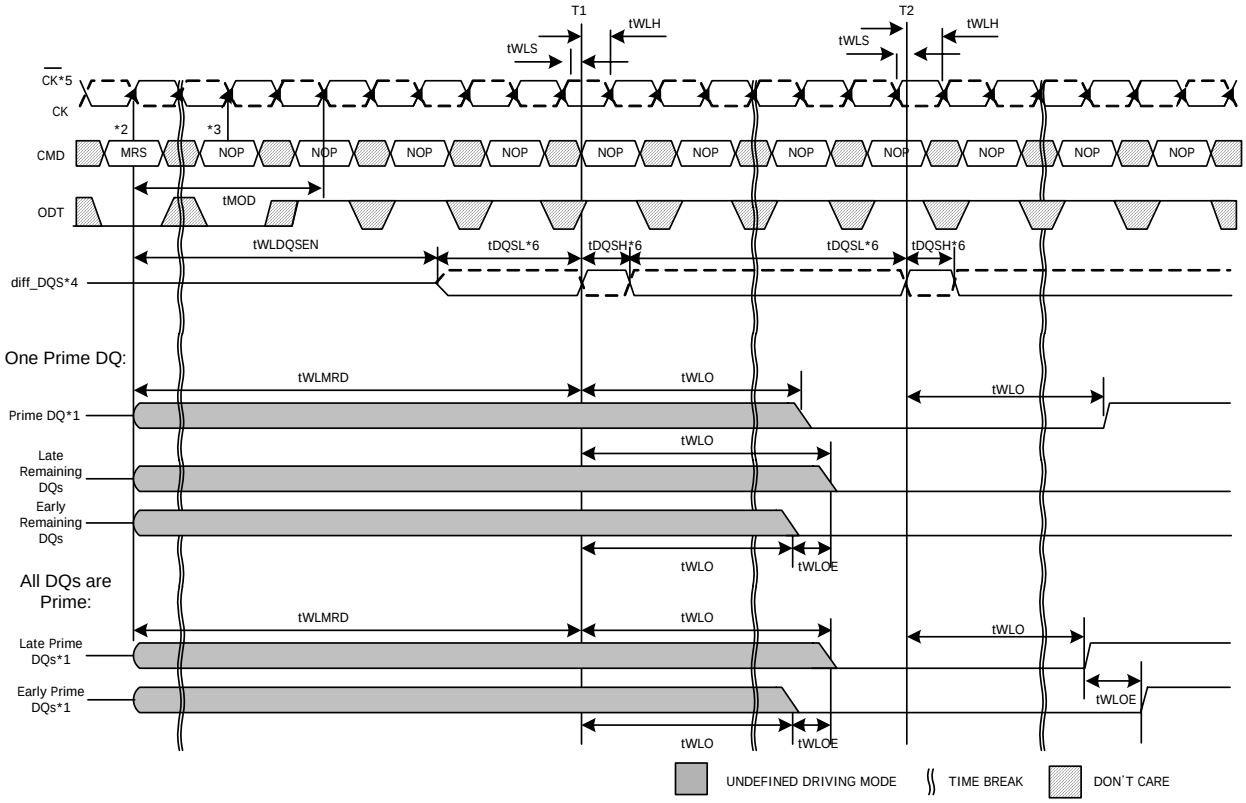
Note: In Write Leveling Mode with its output buffer disabled (MR1[bit7]=1 with MR1[bit12]=1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7]=1 with MR1[bit12]=0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

2.8.2 Procedure Description

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in underfined driving mode. During white leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR7[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5, and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and $\overline{\text{DQS}}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, controller provides a single DQS, DQS edge which is used by the DRAM to sample CK-CK driven from controller. tWLMRD (max) timing is controller dependent.

DRAM samples CK-$\overline{\text{CK}}$ status with rising edge of DQS-$\overline{\text{DQS}}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. Either one or all data bits (“prime DQ bit(s)”) provide the leveling feedback. The DRAM’s remaining DQ bit are driven Low statically after the first sampling procedure. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/$\overline{\text{DQS}}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS-$\overline{\text{DQS}}$ delay setting and launches the next DQS/$\overline{\text{DQS}}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS-$\overline{\text{DQS}}$ delay setting and write leveling is achieved for the device. Figure 17 describes the timing diagram and parameters for the overall Write Leveling procedure.



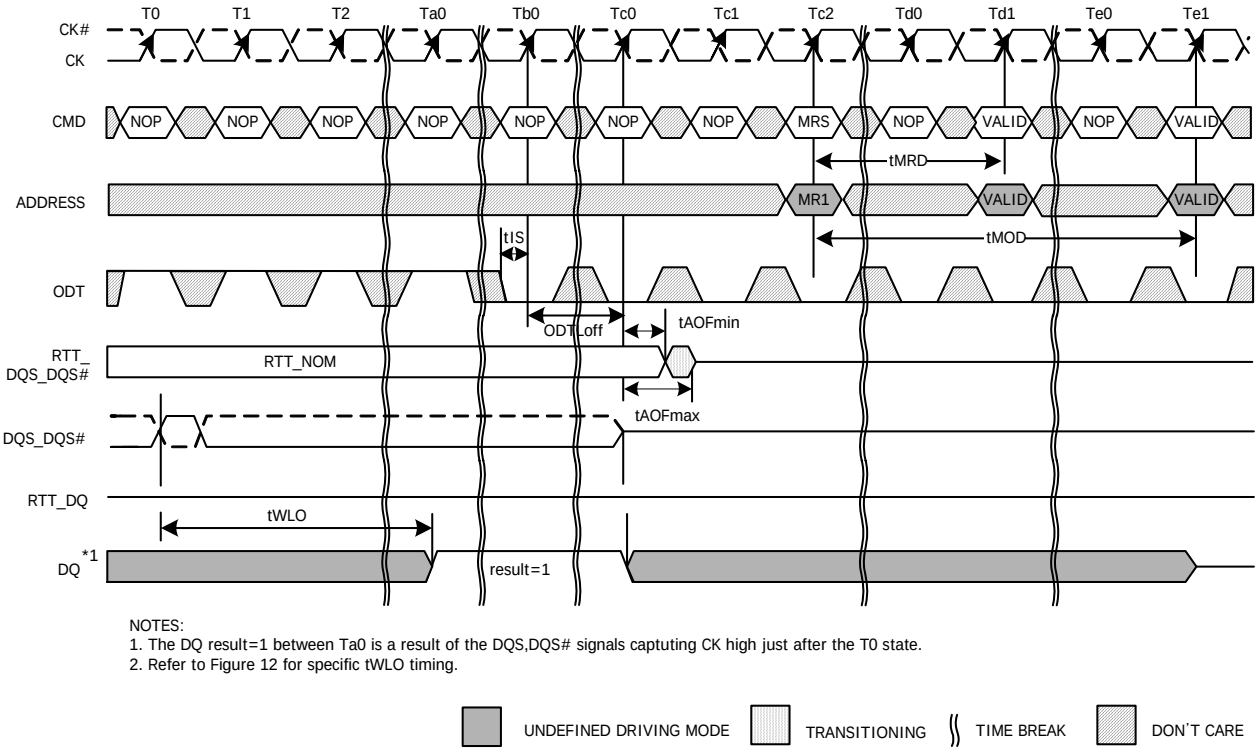
NOTES:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQS must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode
3. NOP: NOP or deselect
4. diff_DQS is the differential data strobe (DQS, DQS#). Tiiming reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line
5. CK,CK#: CK is shown with solid line, where as CK# is drawn with dotted line.
6. DQS,DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Figure 17. Timing details of Write leveling sequence [DQS-DQS is capturing CK-CK low at T1 and CK-CK high at T2

2.8.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command(Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied(Te1), any valid command may be registered. (MR commands may be issued after tMRD(Td1).



NOTES:
1. The DQ result=1 between Ta0 is a result of the DQS,DQS# signals captuting CK high just after the T0 state.
2. Refer to Figure 12 for specific tWLO timing.

Figure 18. Timing details of Write leveling exit

2.9 Extended Temperature Usage

Hynix DDR3 SDRAM devices support the following options or requirements referred to in this material:

a. Auto Self-refresh supported

b. Extended Temperature Range supported

c. Double refresh required for operation in the Extended Temperature Range

Table 18. Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	**Auto Self-Refresh (ASR)** When enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation 0=Manual SR Reference (SRT) 1=ASR enable
SRT	MR2(A7)	**Self-Refresh Temperature (SRT) Range** If ASR=0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation If ASR=1, SRT bit must be set to 0b 0=Normal operating temperature range 1=Extended operating temperature range

2.9.1 Auto Self-Refresh mode-ASR Mode

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6=1b and MR2 bit A7=0b. The DRAM will manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR mode is not enabled(MR2 bit. A6=0b), the SRT bit(MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

2.9.2 Self-Refresh Temperature Range-SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR=0b, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT=0b, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT=1b then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the STR bit can effect self-refresh power consumption, please refer to the IDD table for details.

Table 19. Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal(0-85℃)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended(0-95℃)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent	Normal(0-85℃)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent	Normal and Extended(0-95℃)
1	1	Same as MR2 A[6] = 0, MR2 A[7] = 1	

2.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 19.

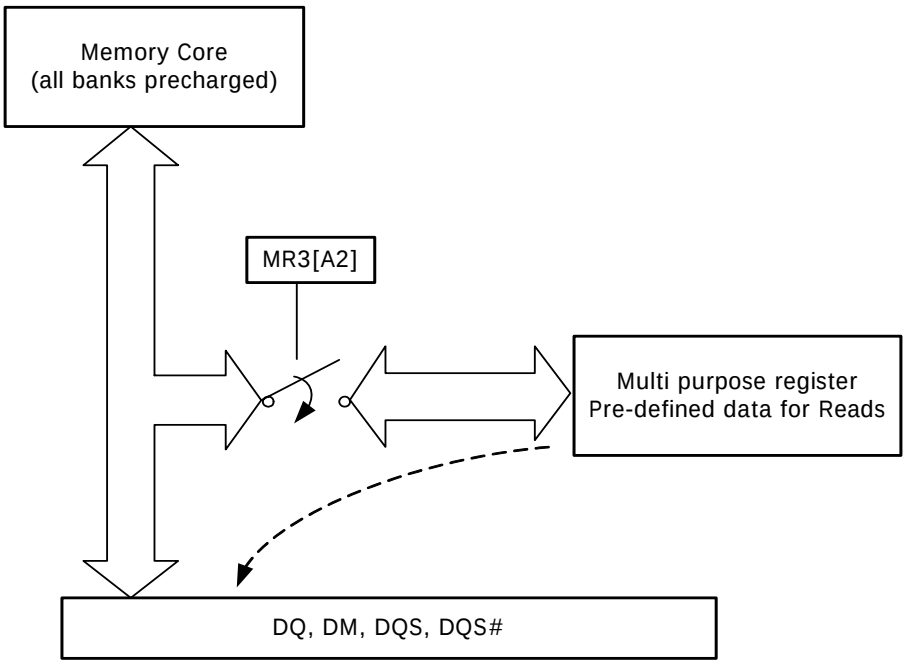


Figure 19. MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2=1, as shown in Table 20. Prior to issuing the MRS command, all banks must be in the idle in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 21. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled(MR3 bit A2=0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 20. MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See Table 21	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0]

2.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
  - DQ[0] drives information from MPR.
  - DQ[3:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x8:
  - DQ[0] drives information from MPR.
  - DQ[7:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x16:
  - DQL[0] and DQU[0] drive information from MPR.
  - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b.Data read burst order in nibble is fixed.
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7],* For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3* A[2]=1b, Burst order: 4,5,6,7*
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11,A13,...(if available): don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

Note: * Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

2.10.2 MPR Register Address Definition

Table 21 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

Table 21. MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
Note: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.					

2.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to ?$paratext>? on page 148.

2.10.4 Protocol Example

Protocol Example (This is one example):

Read out predetermined read-calibration pattern.

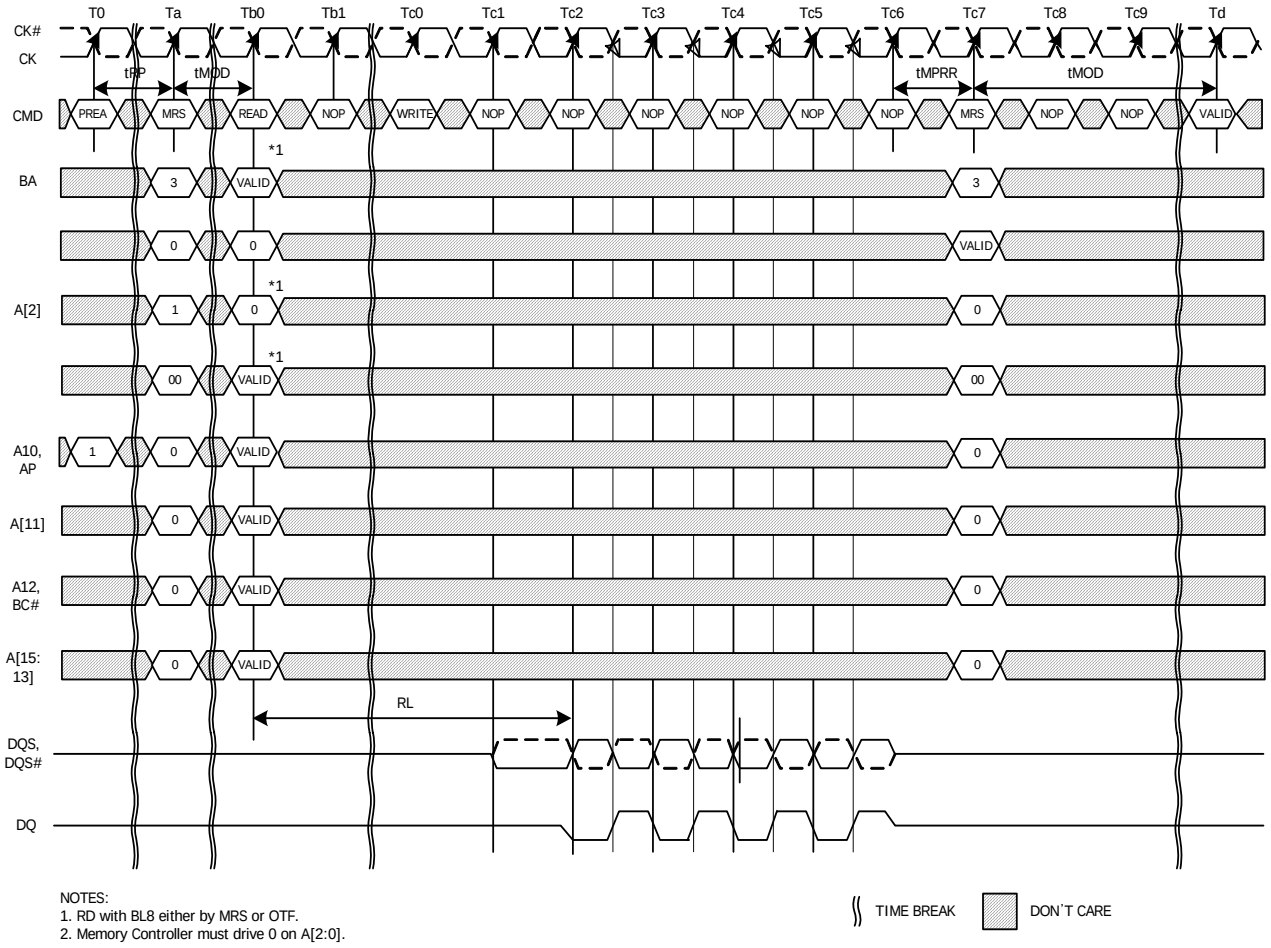
Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode “A2=1b” and “A[1:0]=00b”
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the

period MR3 A2=1, no data write operation is allowed.

- Read:
  - A[1:0]=‘00’b (Data burst order is fixed starting at nibble, always 00b here)
  - A[2]=’0’b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12/BC=1 (use regular burst length of 8)
  - All other address pins (including BA[2:0] and A10/AP): don’t care
- After RL=AL+CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode “A2=0b” and “A[1:0]=valid data but value are don’t care”
  - All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with “regular” DRAM commands, like activate a memory bank for regular read or write access,...
-



NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[2:0].

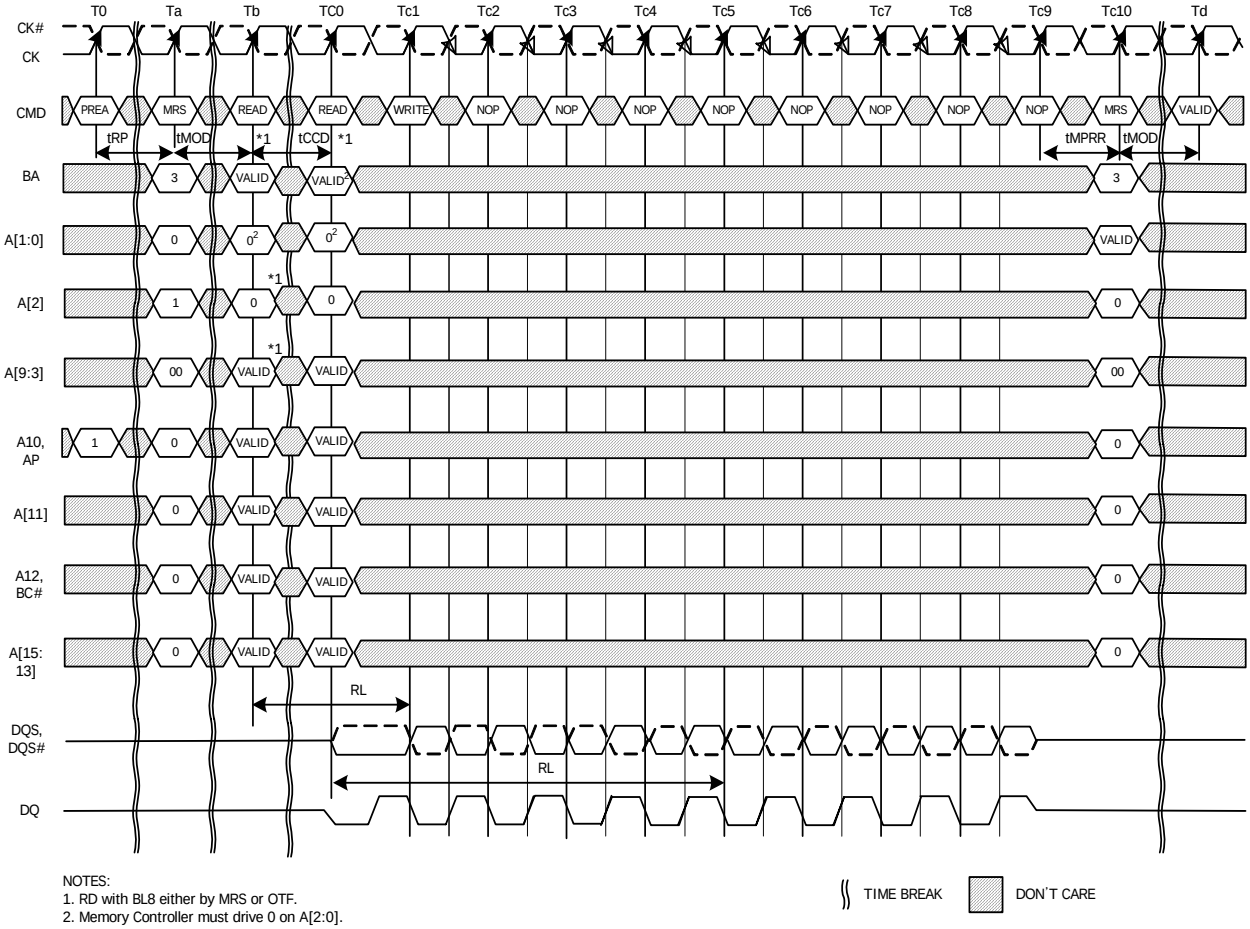
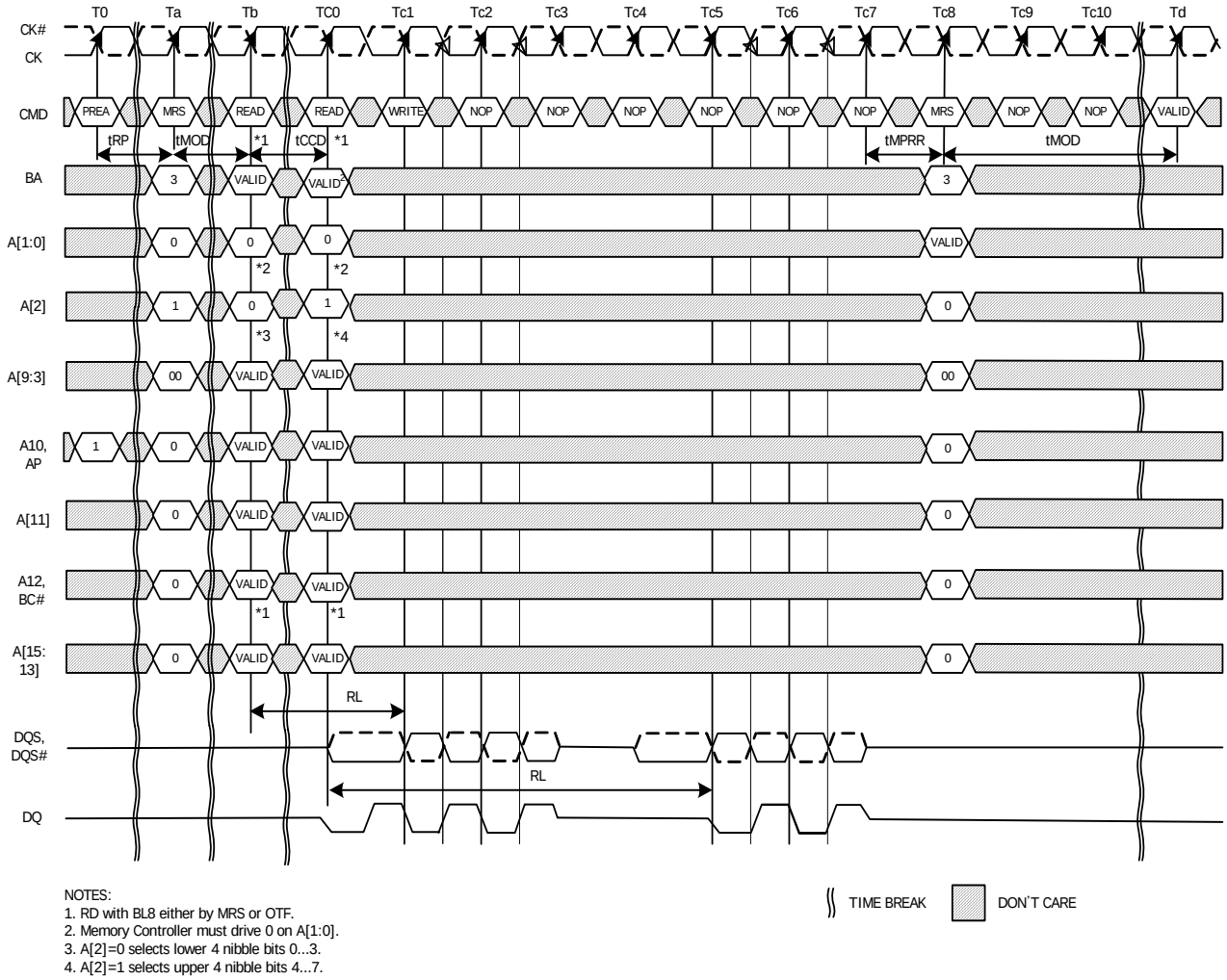
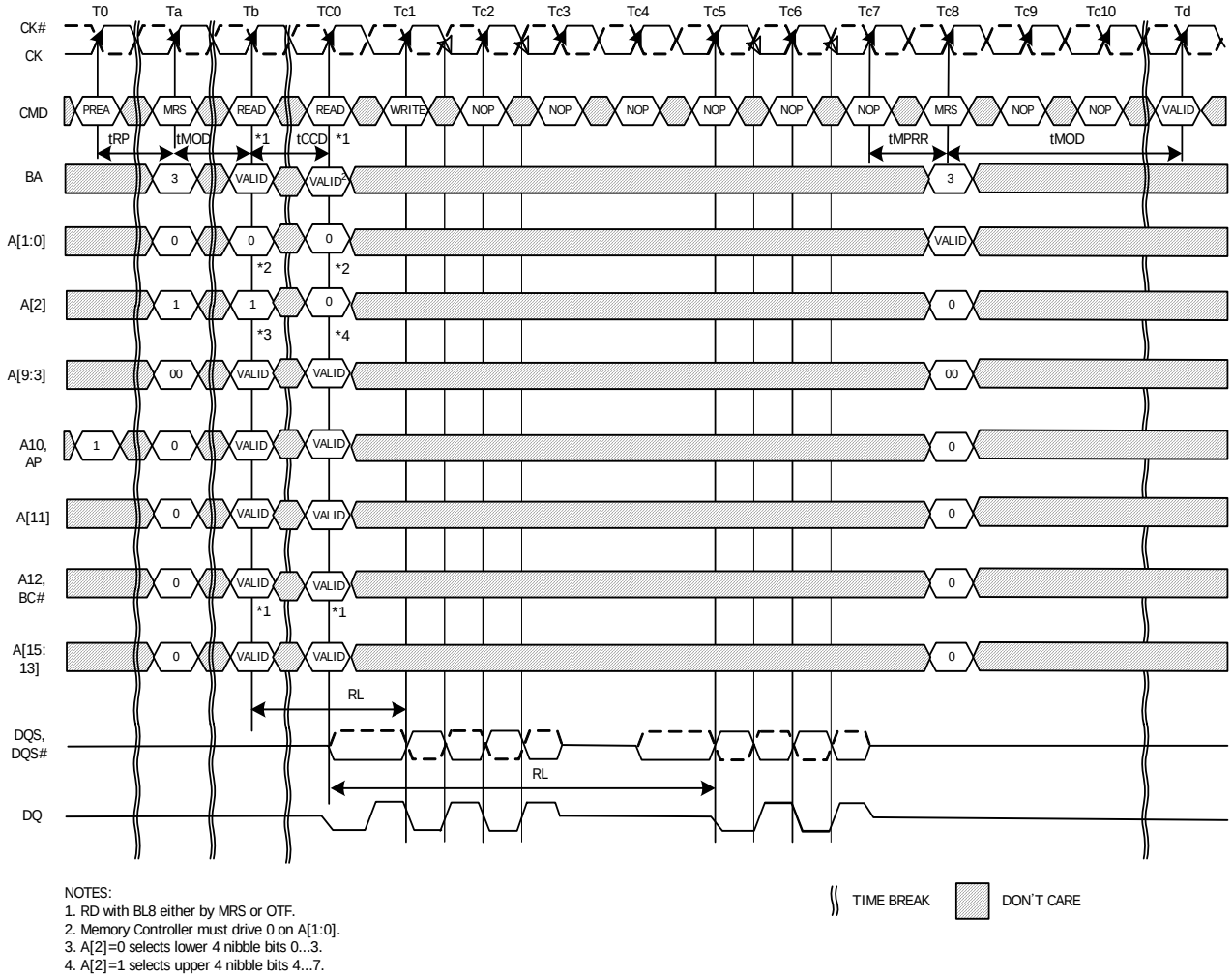


Figure 21. MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout



NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0...3.
4. A[2]=1 selects upper 4 nibble bits 4...7.

Figure 22. MPR Readout of predefined pattern, BC4, lower nibble then upper readout



NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0...3.
4. A[2]=1 selects upper 4 nibble bits 4...7.

Figure 23. MPR Readout of predefined pattern, BC4, upper nibble then lower readout

2.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

2.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

2.13 READ Operation

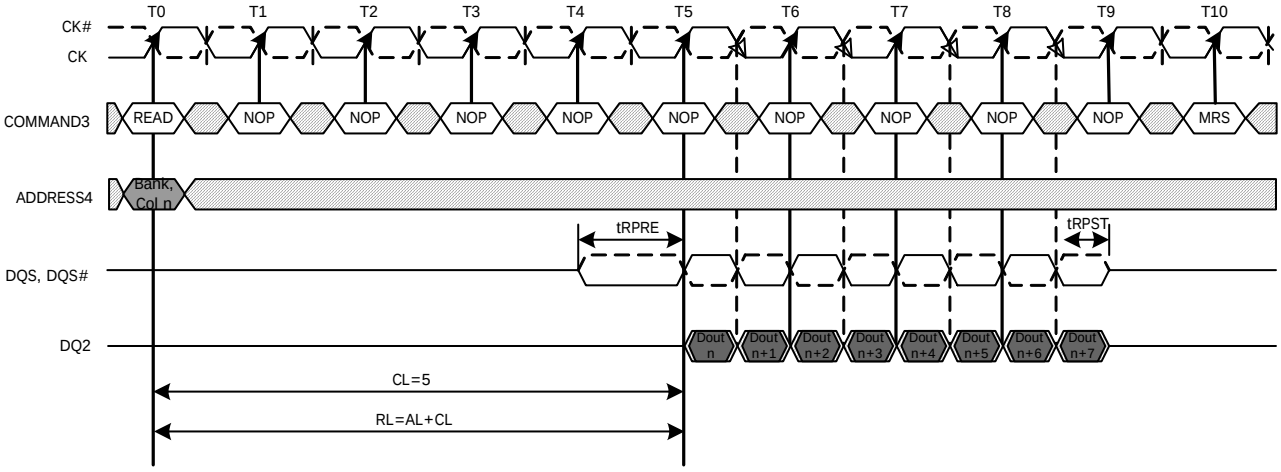
2.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE(AUTO PRECHARGE can be enabled or disabled).

A12=0, BC4(BC4=burst chop, tCCD=4)

A12=1, BL8

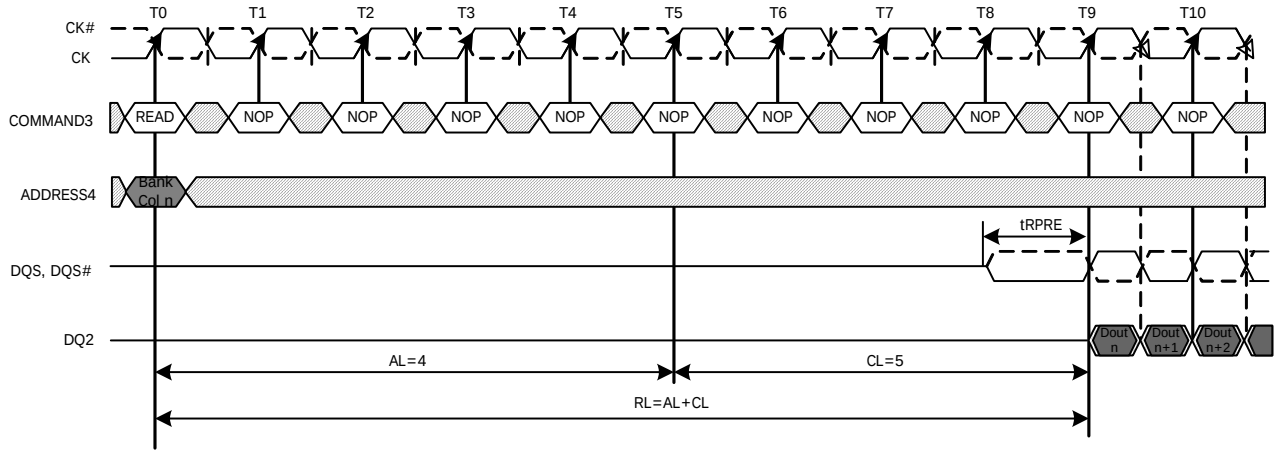
A12 is used only for burst length control, not as a column address.



NOTE: 1. BL8, RL=5, AL=0, CL=5.
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration: other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 24. READ Burst Operation RL=5 (AL=0,CL=5,BL8)



NOTE: 1. BL8, RL=9, AL=(CL-1), CL=5.
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 25. READ Burst Operation RL=9 (AL=4,CL=5,BL8)

2.13.2 READ Timing Definitions

Read timing is shown in Figure 26 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative a CK,CK#.
- tDQSCK is the actual position or a rising strobe edge relative to CK,CK#.
- tQSH describes the DQS,DQS# differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS,DQS# differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQS; both rising/falling edges of DQS, no tAC defined.

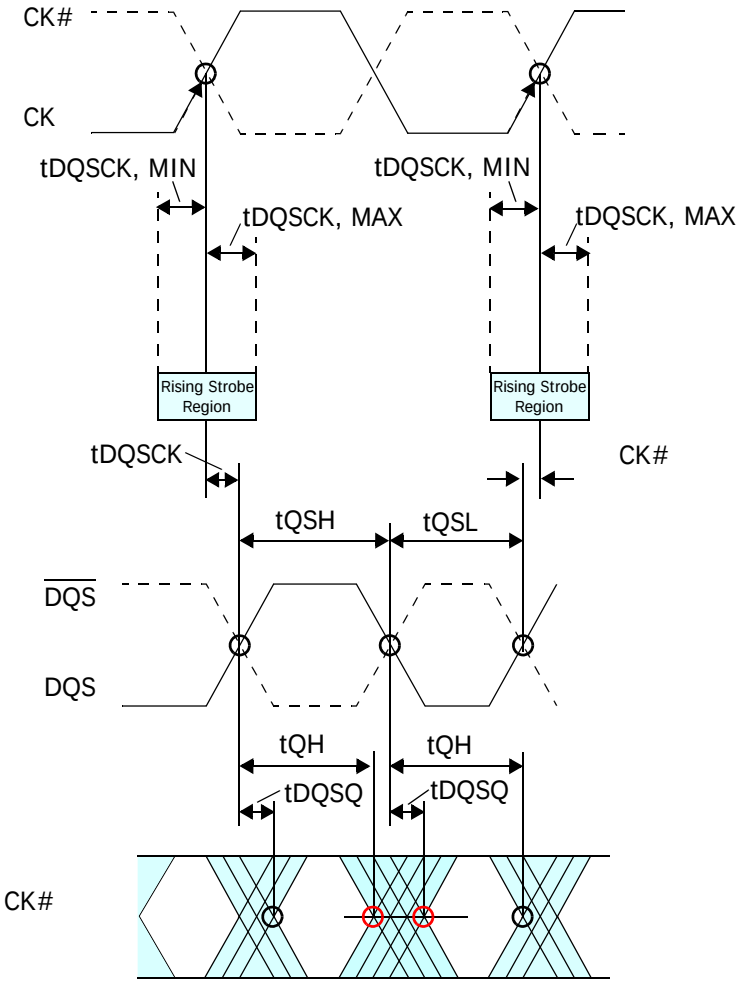


Figure 26. READ Timing Definition

2.13.2.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 27 and is applied when the DLL is enabled and locked.

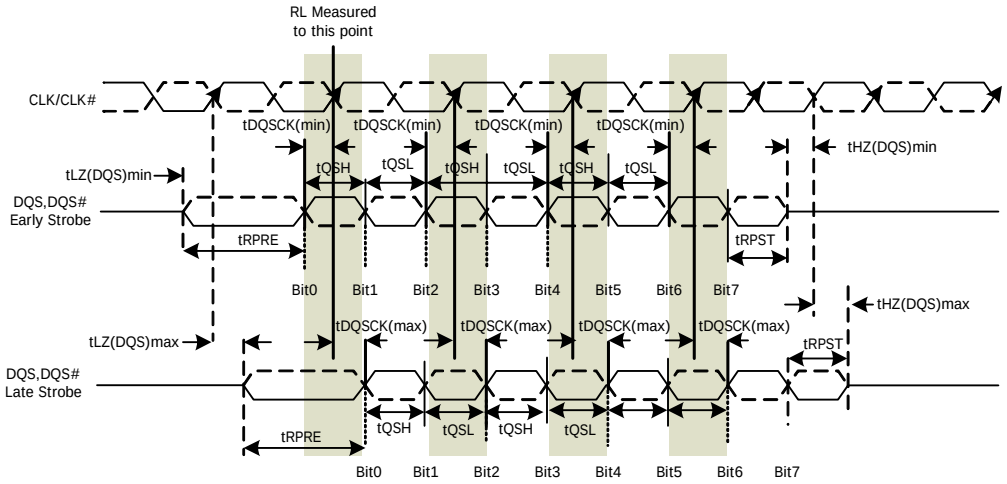
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK,CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK,CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

tLZ (DQS), tHZ (DQS) for preamble/postamble (see 2.13.2.3 and Figure 29)



NOTE: 1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising edge can vary between tDQSCK(min) and tDQSCK(max).
2. Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relactionship (tQSH, tQSL) exist:
if tDQSCK(n+1) < 0:
tDQSCK(n) < 1.0 tCH ? (tQSHmin + tQSLmin) - | tDQSCK(n+1) |
2. The DQS,DQS# differential output high time is defined by tQSH and the DQS,DQS# differential output low time is defined by tQSL.
3. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin(early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax(late strobe case).
4. The minimum pulse width of read preamble is defined tRPRE(min).
5. The maximum read postamble is bound by tDQSCK(min(plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
6. The minimum pulse width read postamble is defined by tRPST(min).
7. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Figure 27. Clock to Data Strobe Relationship

2.13.2.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 28 and is applied when the DLL is enabled and locked.

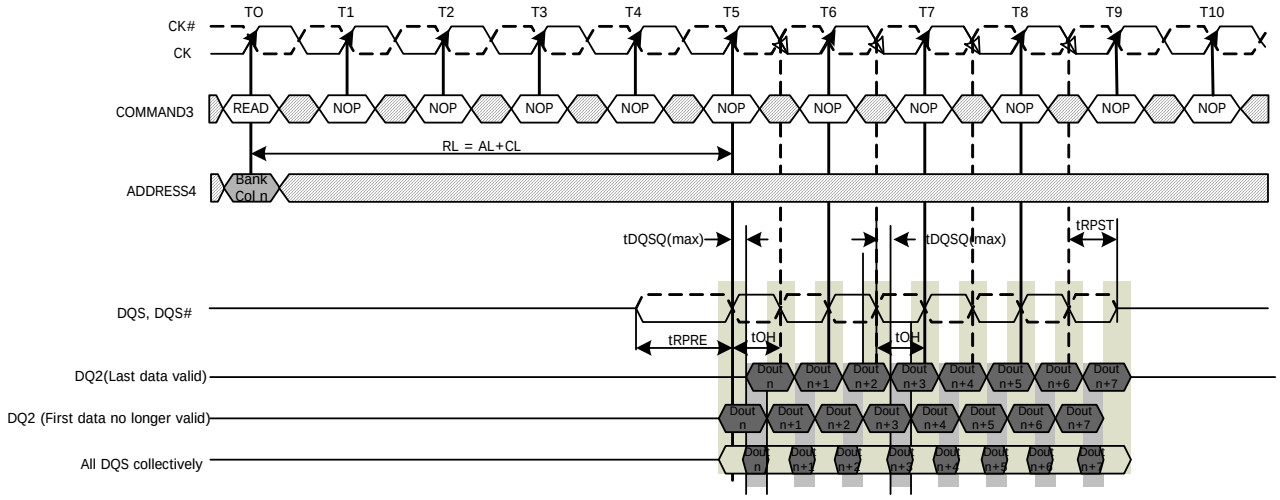
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Filling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined



NOTE: 1. BL=8, RL=5 (AL=0, CL=5)
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=] and A12=1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS, DQS# to Data and does net define DQS, DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

Figure 28. Data Strobe to Data Relationship

2.13.2.3 tLZ(DQS), tLZ (DQ), tHZ(DQS), tHZ (DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ (DQ), or begins driving tLZ(DQS), tLZ (DQ). Figure 29 shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ (DQ), or begins driving tLZ(DQS), tLZ (DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ (DQ), tHZ(DQS), and tHZ (DQ) are defined as singled ended.

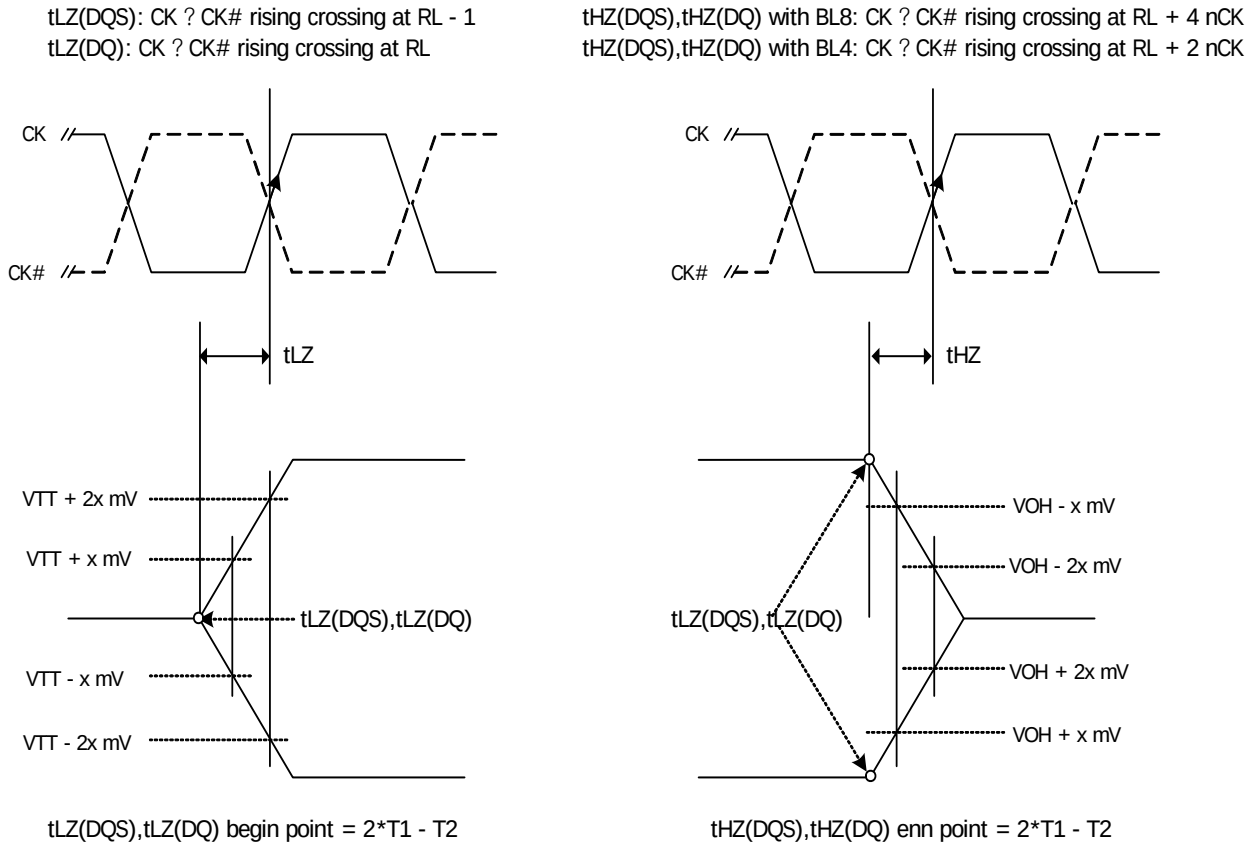


Figure 29. tLZ and tHZ method for calculating transitions and endpoints

2.13.2.4 tRPRE Calculation

Method for calculating differential pulse widths for tRPRE is shown in Figure 30.

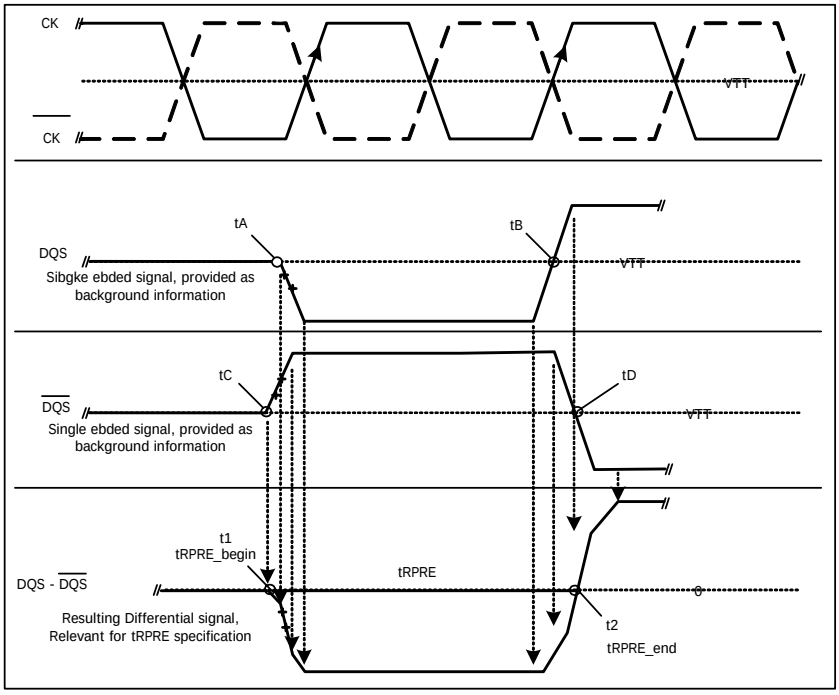


Figure 30. Method for calculating tRPRE transitions and endpoints

2.13.2.5 tRPST Calculation

Method for calculating differential pulse widths for tRPST is shown in Figure 31.

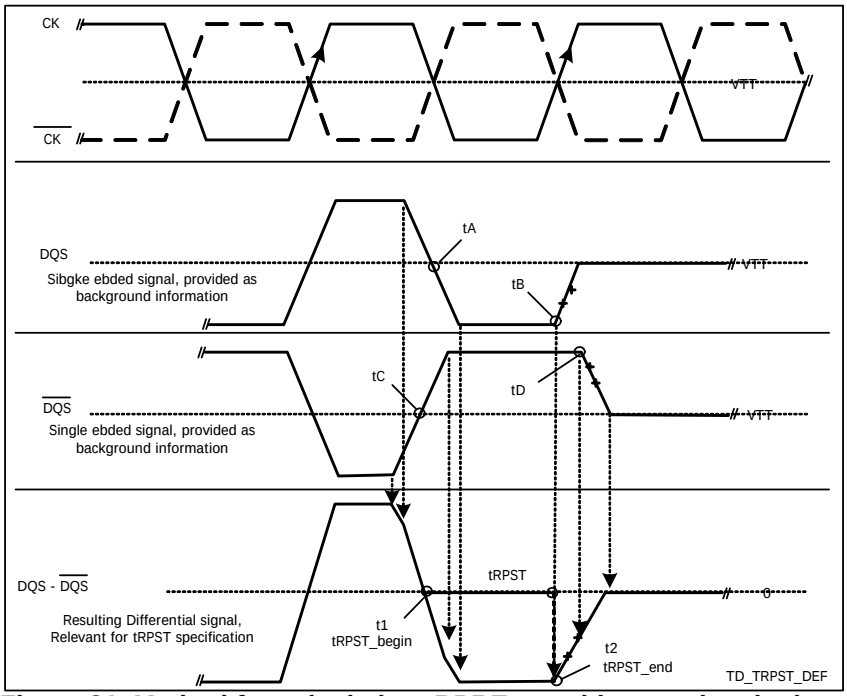
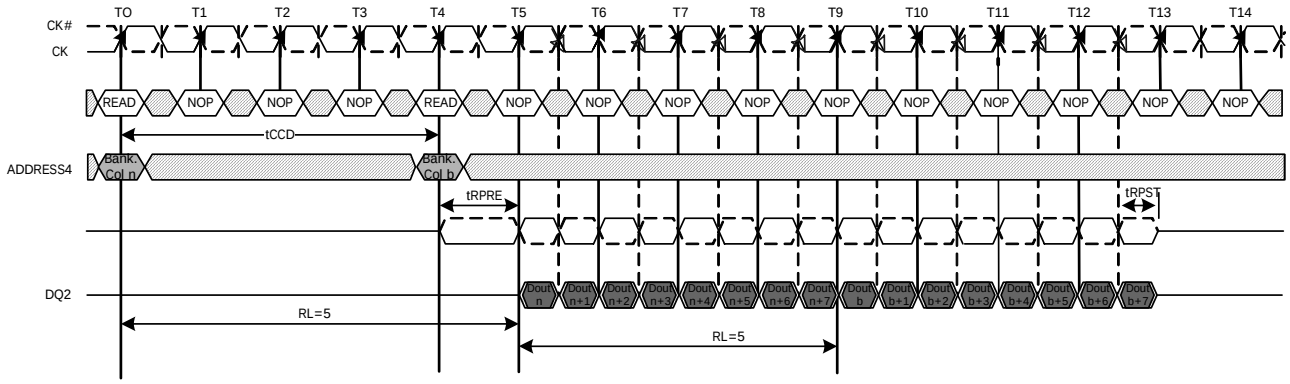


Figure 31. Method for calculating tRPRE transitions and endpoints



NOTE: 1. BL8, RL=5 (CL=5, AL=0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during READ command at T0 and T4

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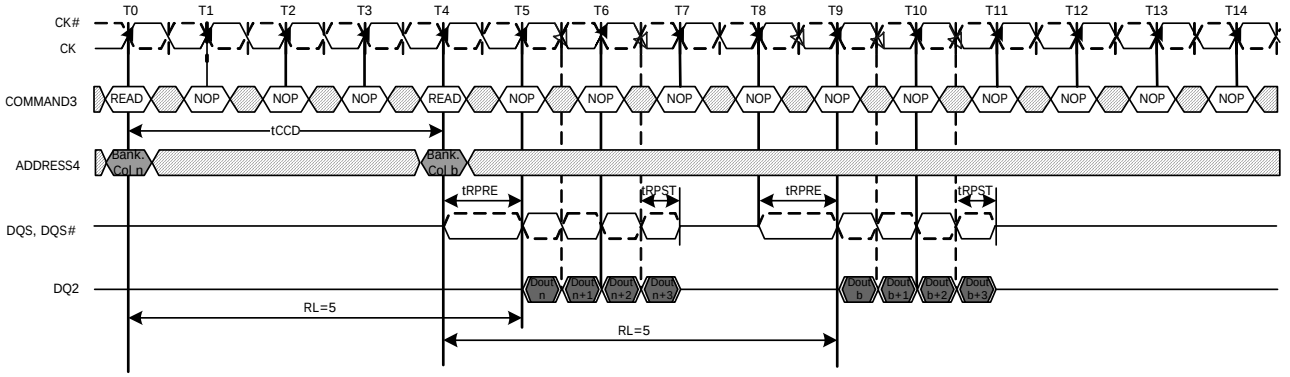
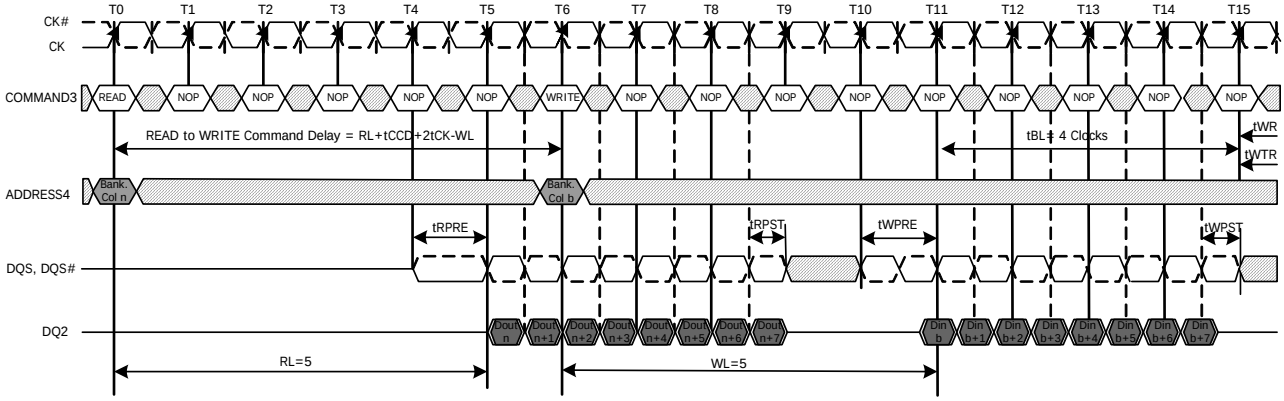
Figure 32. READ(BL8) to READ(BL8)



NOTE: 1. BL4, RL=5 (CL=5, AL=0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL4 setting activated by either MR0[A1:0=10] or MR0[A1:0=01] and A12=0 during READ command at T0 and T4.

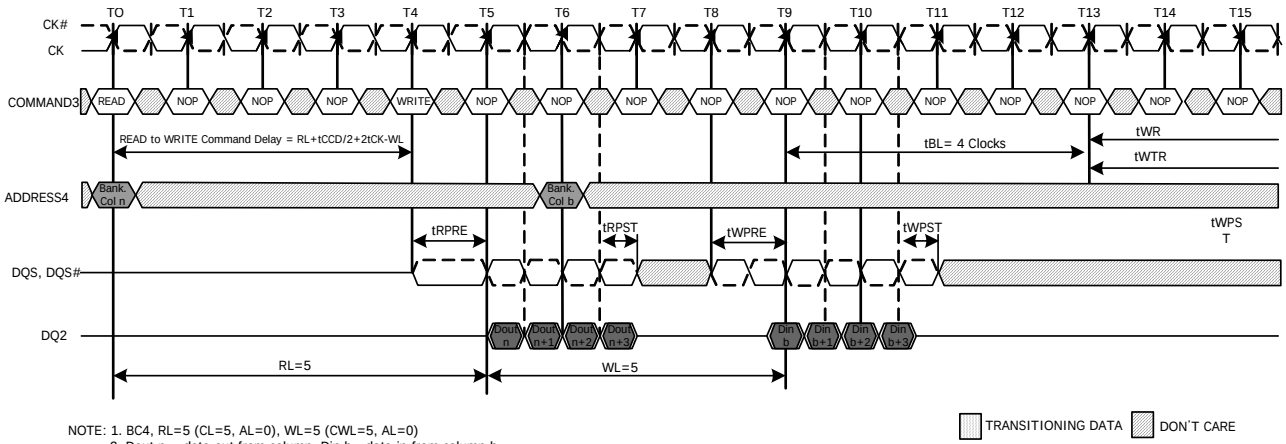
TRANSITIONING DATA DON'T CARE

Figure 33. READ(BC4) to READ(BC4)



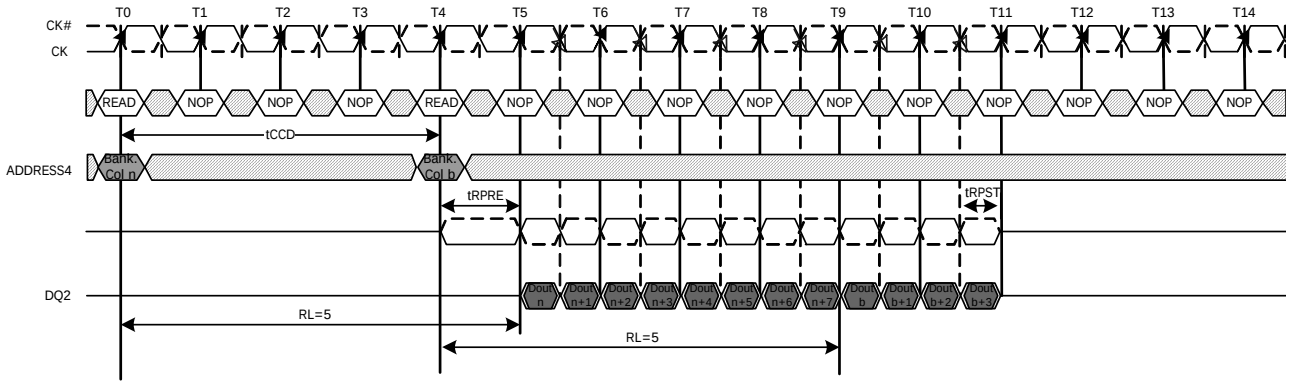
NOTE: 1. BL8, RL=5 (CL=5, AL=0), WL=5 (CWL=5, AL=0)
2. Dout n (or b) = data-out from column, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1=01] and A12=1 during READ command at T0 and WRITE command at T6

Figure 34. READ(BL8) to WRITE(BL8)



NOTE: 1. BC4, RL=5 (CL=5, AL=0), WL=5 (CWL=5, AL=0)
2. Dout n = data-out from column, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during READ command at T0 and WRITE command at T4.

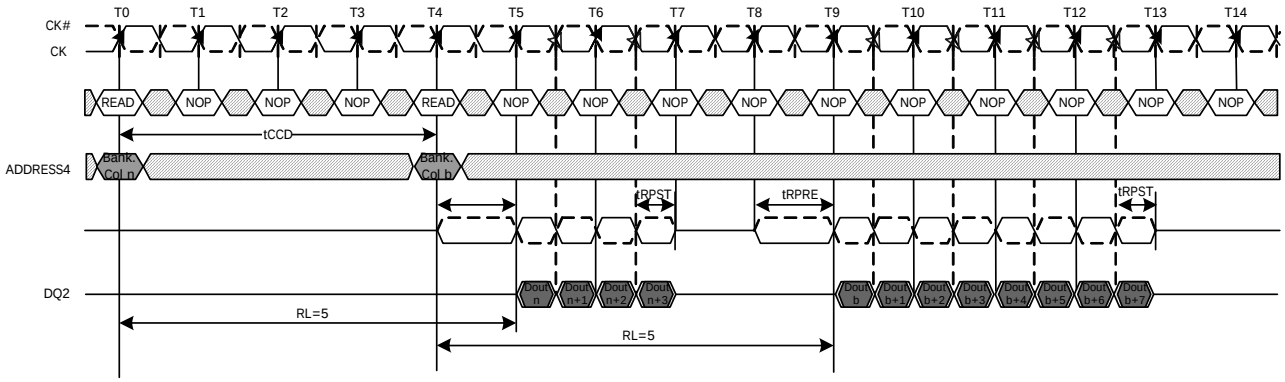
Figure 35. READ(BC4) to WRITE(BC4) OTF



NOTE: 1. RL=5 (CL=5, AL=0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=01] and A12=1 during READ command at T0.
BC4 setting activated by either MR0[A1:0=01] and A12=0 during READ command at T4.

TRANSITIONING DATA DON'T CARE

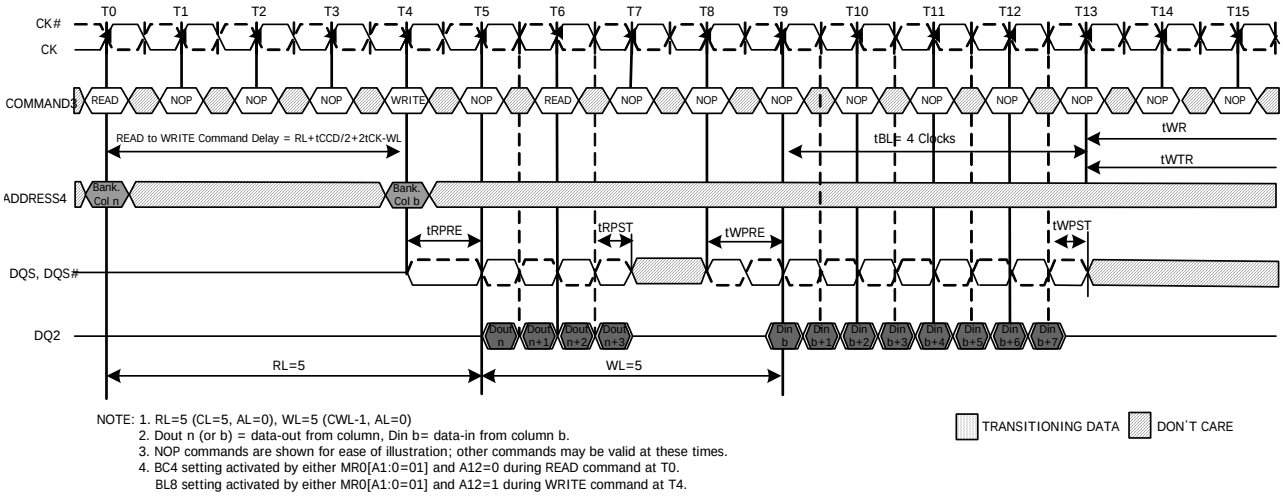
Figure 36. READ(BL8) to READ(BC4) OTF



NOTE: 1. RL=5 (CL=5, AL=0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during READ command at T0.
BL8 setting activated by either MR0[A1:0=01] and A12=1 during READ command at T4.

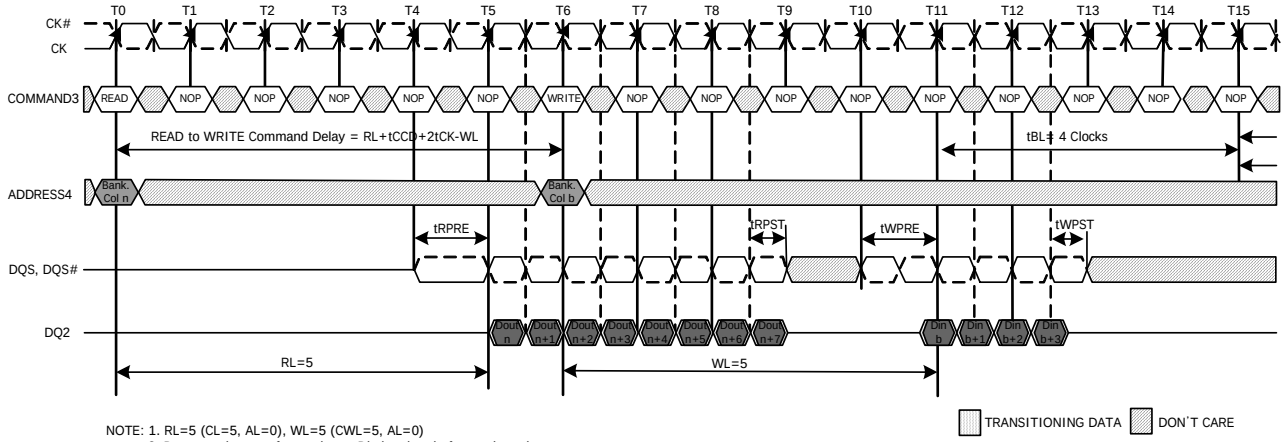
TRANSITIONING DATA DON'T CARE

Figure 37. READ(BC4) to READ(BL8) OTF



NOTE: 1. RL=5 (CL=5, AL=0), WL=5 (CWL-1, AL=0)
2. Dout n (or b) = data-out from column, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during READ command at T0.
BL8 setting activated by either MR0[A1:0=01] and A12=1 during WRITE command at T4.

Figure 38. READ(BC4) to WRITE(BL8) OTF



NOTE: 1. RL=5 (CL=5, AL=0), WL=5 (CWL=5, AL=0)
2. Dout n = data-out from column, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=01] and A12=1 during READ command at T0.
BC4 setting activated by either MR0[A1:0=01] and A12=0 during WRITE command at T6.

Figure 39. READ(BL8) to WRITE(BC4) OTF

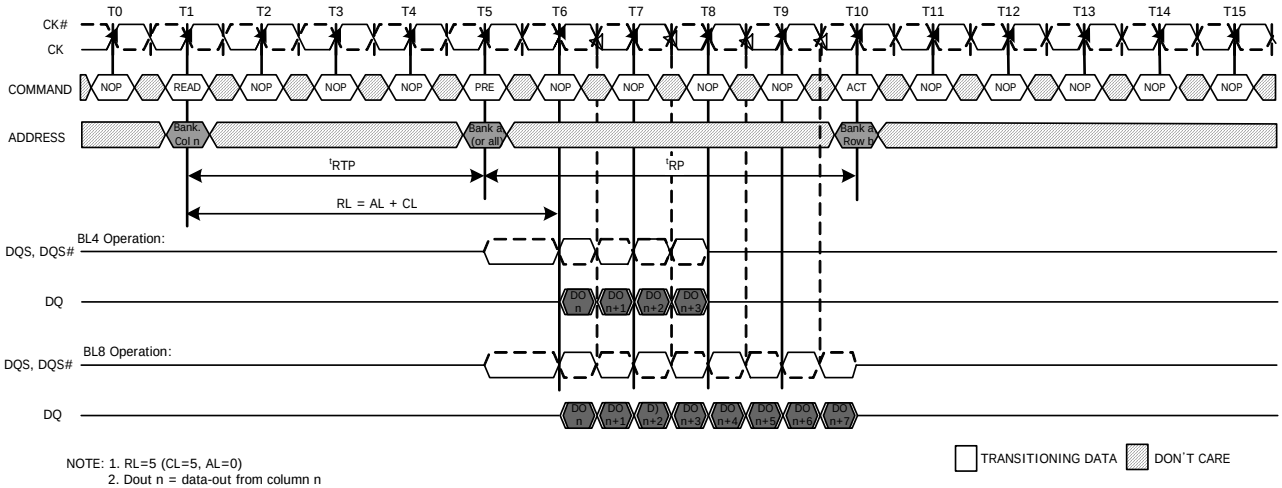
2.13.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.MIN = max(4 x nCK, 7.5 ns). A new bank active command may be issued to the same bank if the following tow conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.

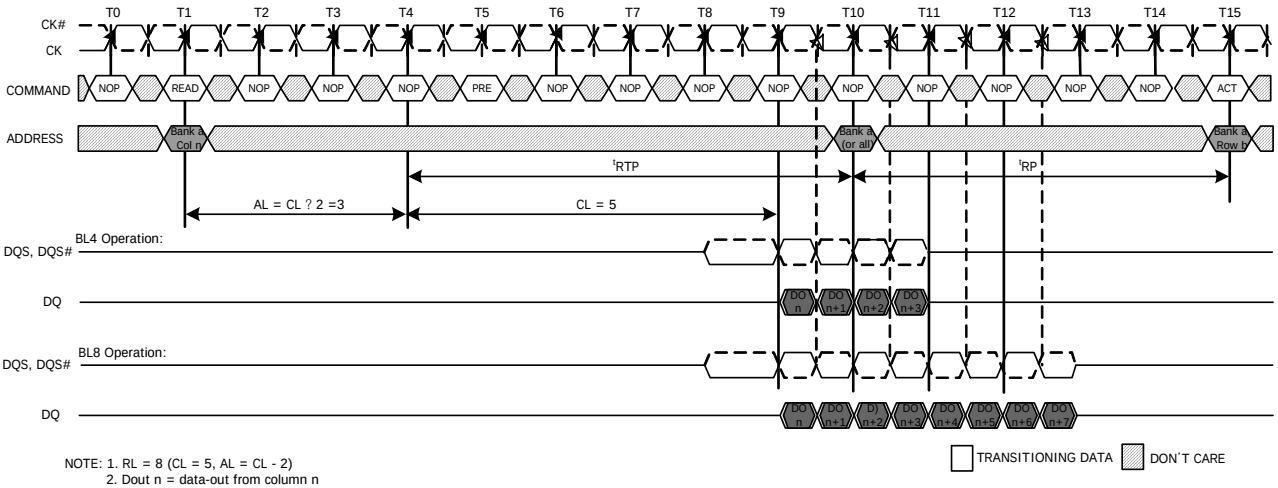
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Figure 40 and Figure 41.



NOTE: 1. RL=5 (CL=5, AL=0)
2. Dout n = data-out from column n
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time (T5) and that tRC. MIN is satisfied at the next Active command time (T10).

Figure 40. READ to PRECHARGE, RL = 5, AL = 0, CL = 5, tRTP = 4, tRP = 5



NOTE: 1. RL = 8 (CL = 5, AL = CL - 2)
2. Dout n = data-out from column n
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time (T10) and that tRC. MIN is satisfied at the next Active command time (T15).

Figure 41. READ to PRECHARGE, RL = 8, AL = CL - 2, CL = 5, tRTP = 6, tRP = 5

2.14. WRITE Operation

2.14.1 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE(AUTO PRECHARGE can be enabled or disabled).

A12=0, BC4(BC4=burst chop, tCCD=4)

A12=1, BL8

A12 is used only for burst length control, not as a column address.

2.14.2 WRITE Timing Violations

2.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain minor violations, that the DRAM is guaranteed not to “hang up” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

2.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example (Figure 42 on page 87), the relevant strobe edges for write burst A are associated with the clock edges: T5,T5.5,T6,T6.5,T7,T7.5,T8,T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

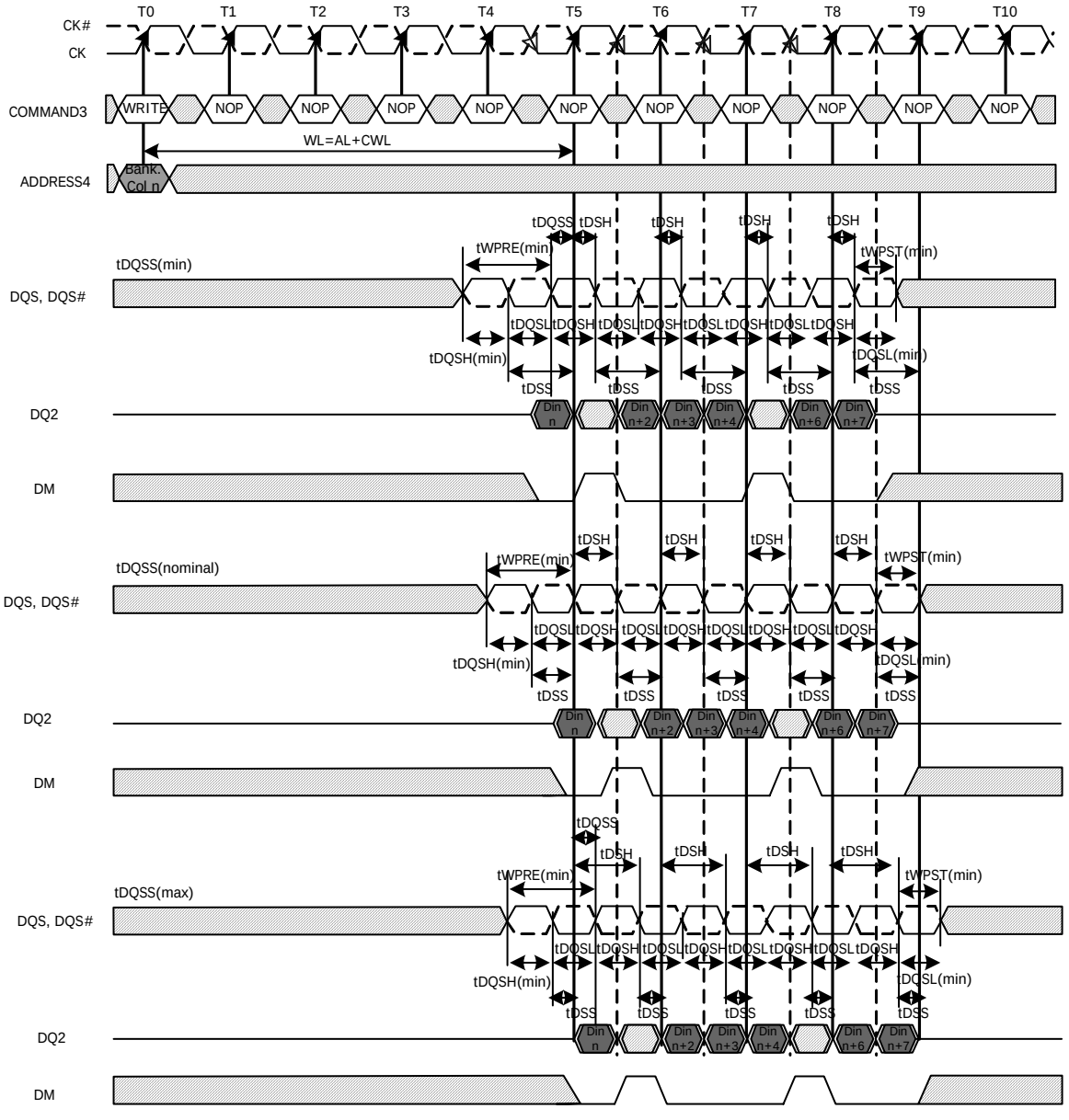
2.14.2.3 Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 50 on page 91) the relevant strobe edges for Write burst n are associated with the clock edges: T4,T4.5,T5,T5.5,T6,T6.5,T7,T7.5,T8,T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fulfilled for a valid burst. For Write burst b the relevant edges are T8,T8.5,T9,T9.5,T10,T10.5,T11,T11.5,T12,T12.5 and T13. Some edges are associated with both bursts.

2.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).



NOTE: 1. BL8, WL=5 (AL=0, CWL=5)
2. Din n = data-in from column n
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0=00] or MR0[A1:0=] and A12=1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

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Figure 42. Write Timing Definition and Parameters

2.14.3 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, consistent with the implementation on DDR2 SDRAMs. It has identical timings on write operations as the data bits as shown in Figure 42, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM of x8 bit organization can be used as TDQS during write cycles if enabled by the MR1[A11] setting. See 1.4.3.7 “TDQS,TDQS” on page 16 for more details on TDQS vs. DM operations.

2.14.4 tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown in Figure 43.

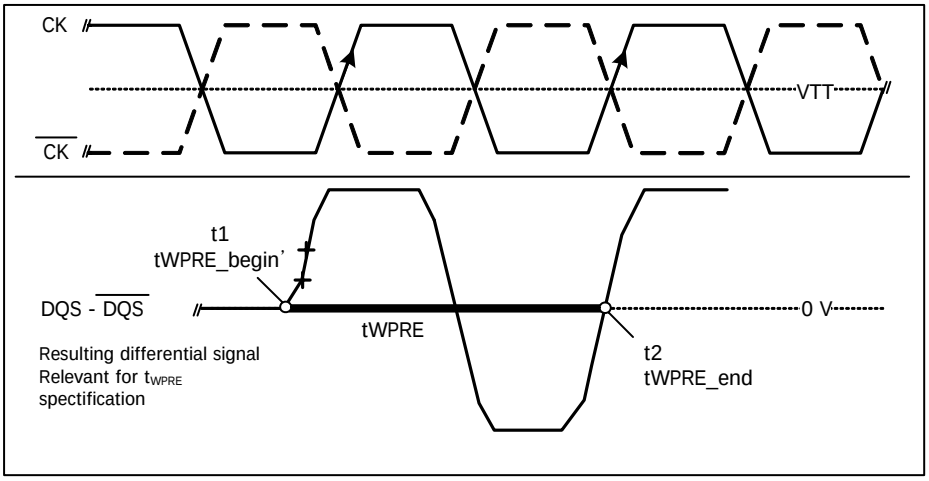


Figure 43. Method for calculating tWPRE transitions and endpoint

2.14.5 tWPST Calculation

The method for calculating differential pulse widths for tWPST is shown in Figure 44.

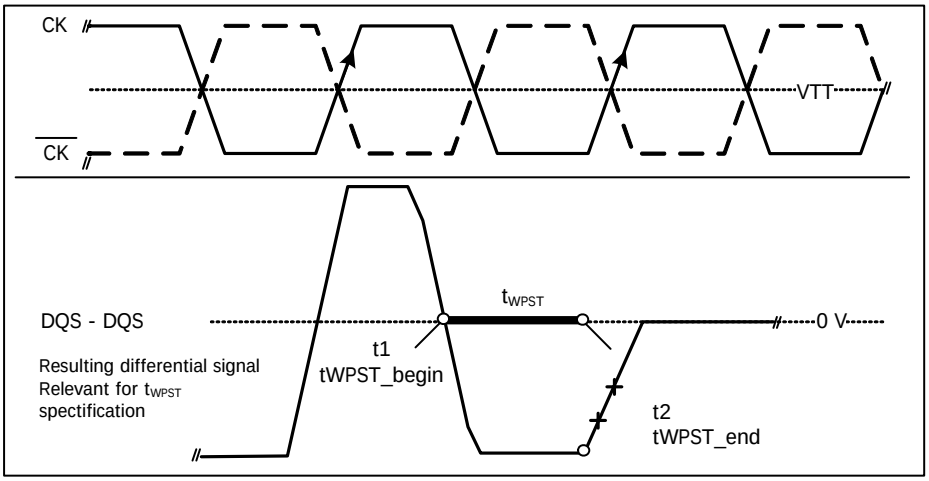
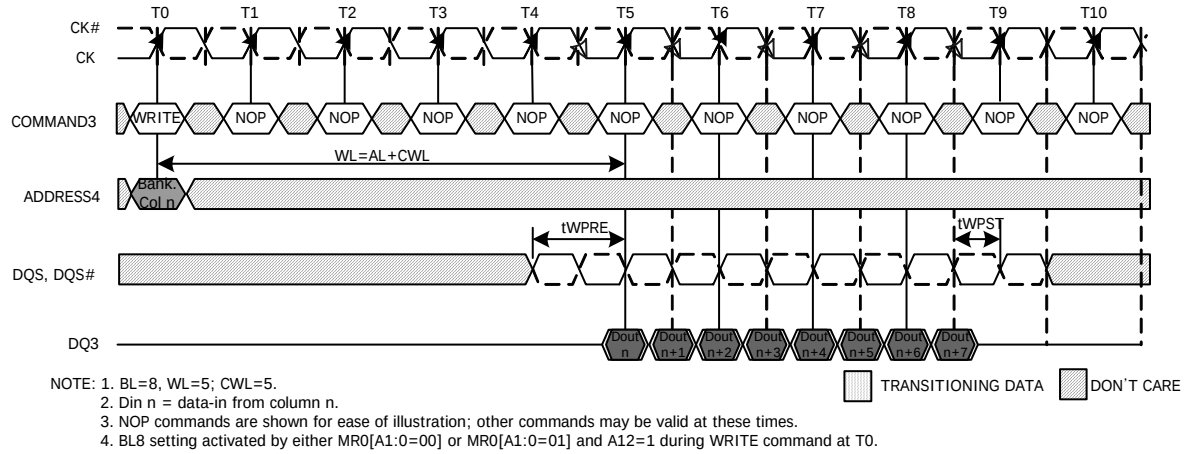
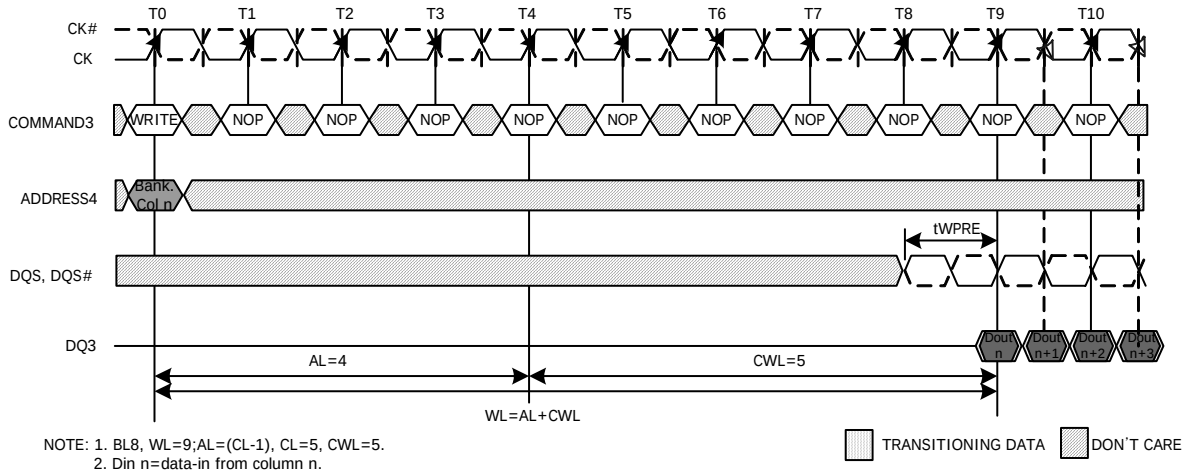


Figure 44. Method for calculating tWPST transitions and endpoint



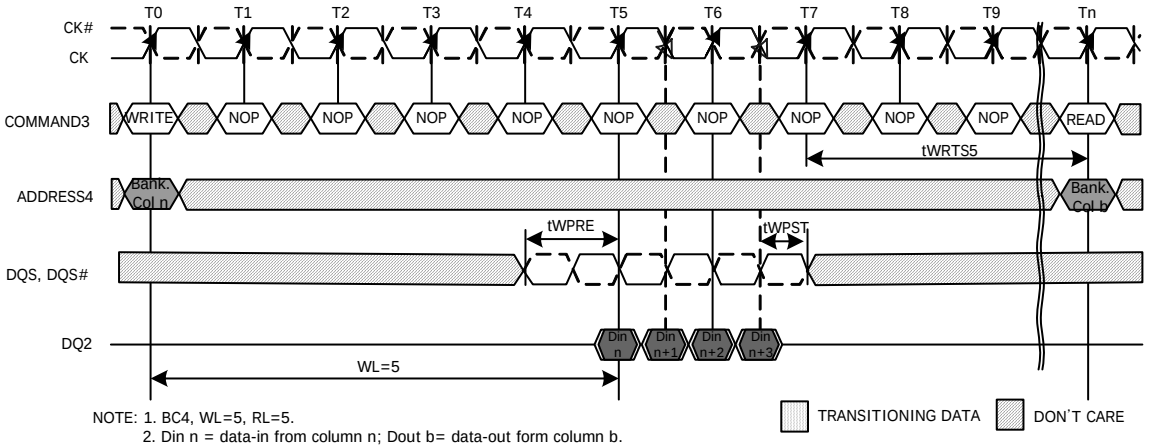
NOTE: 1. BL=8, WL=5; CWL=5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0.

Figure 45. WRITE Burst Operation WL=5 (AL=0,CWL=5,BL8)



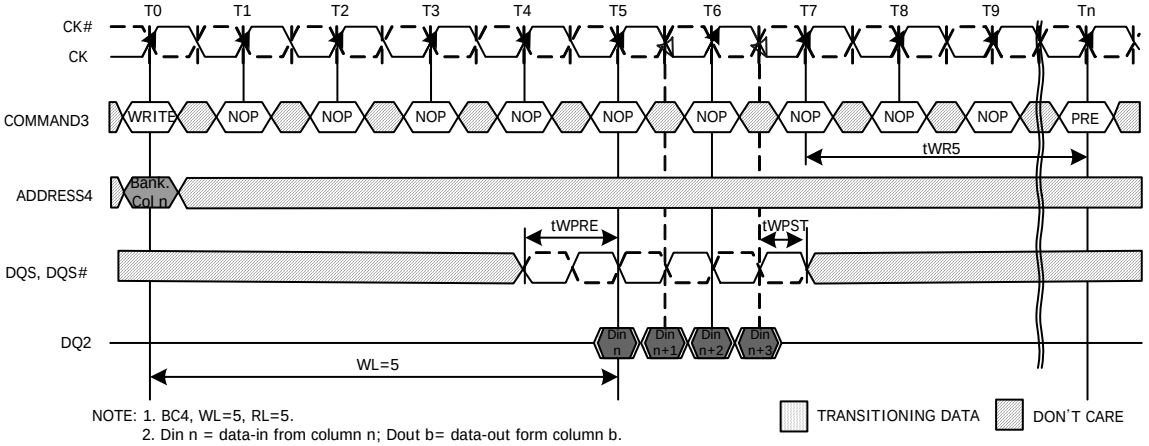
NOTE: 1. BL8, WL=9;AL=(CL-1), CL=5, CWL=5.
2. Din n=data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0.

Figure 46. WRITE Burst Operation WL=9 (AL=CL-1,CWL=5,BL8)



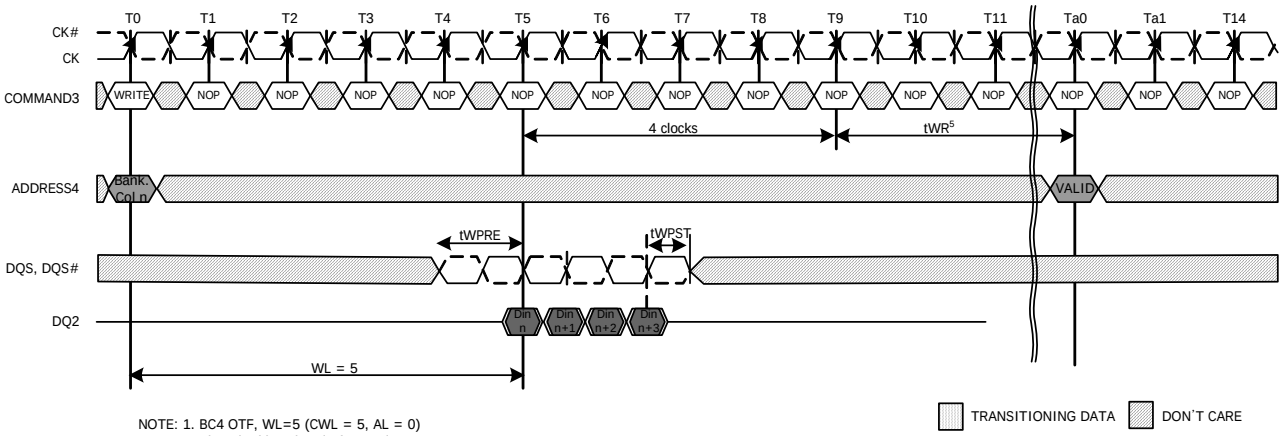
NOTE: 1. BC4, WL=5, RL=5.
2. Din n = data-in from column n; Dout b= data-out form column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC=4 setting activated by MR0[A1:0=10] during WRITE command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

Figure 47. WRITE (BC4) to READ (BC4) Operation



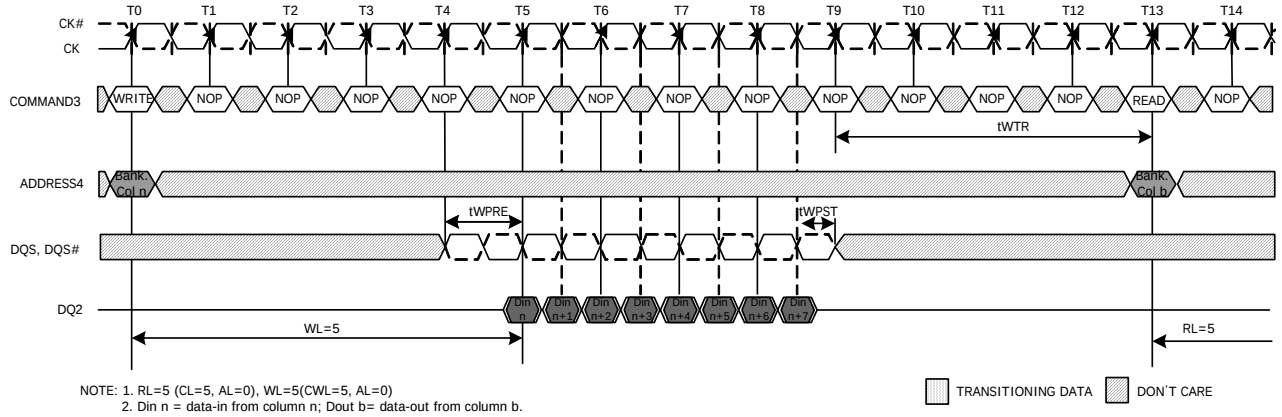
NOTE: 1. BC4, WL=5, RL=5.
2. Din n = data-in from column n; Dout b= data-out form column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0=10] during WRITE command at T0.
5. The write recovery time(tWR) referenced from the first rising clock edge after the last write data shown at T7.
tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 48. WRITE (BC4) to PRECHARGE Operation



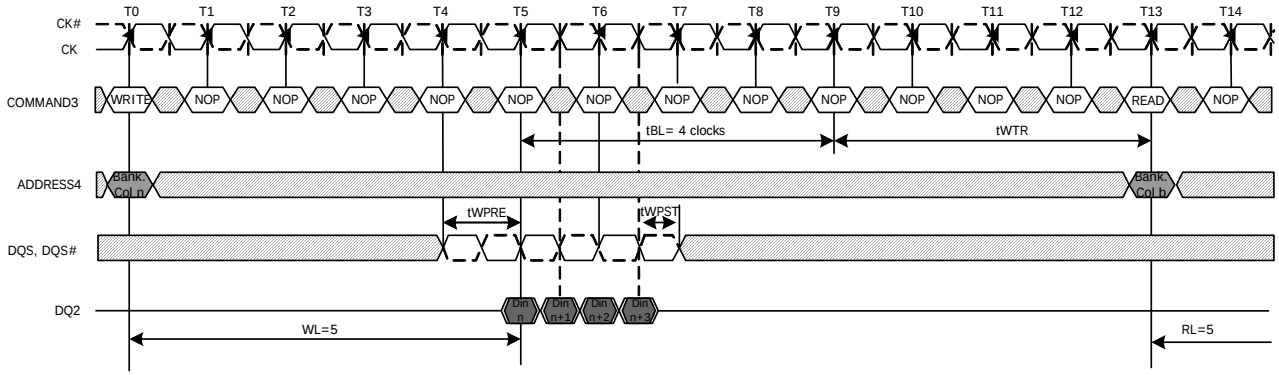
NOTE: 1. BC4 OTF, WL=5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 OTF setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
5. The write recovery time(tWR) starts at the rising clock edge T9 (4 clocks from T5).

Figure 49. WRITE (BC4) OTF to PRECHARGE Operation



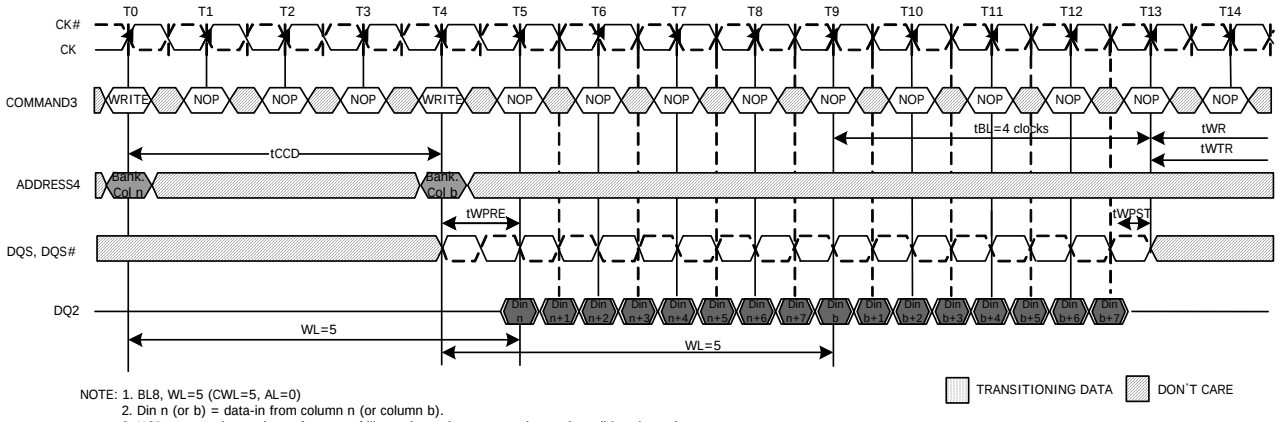
NOTE: 1. RL=5 (CL=5, AL=0), WL=5(CWL=5, AL=0)
2. Din n = data-in from column n; Dout b= data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on MR0[A1:0] and A12 status at T13.

Figure 50. WRITE (BL8) to WRITE (BL8)



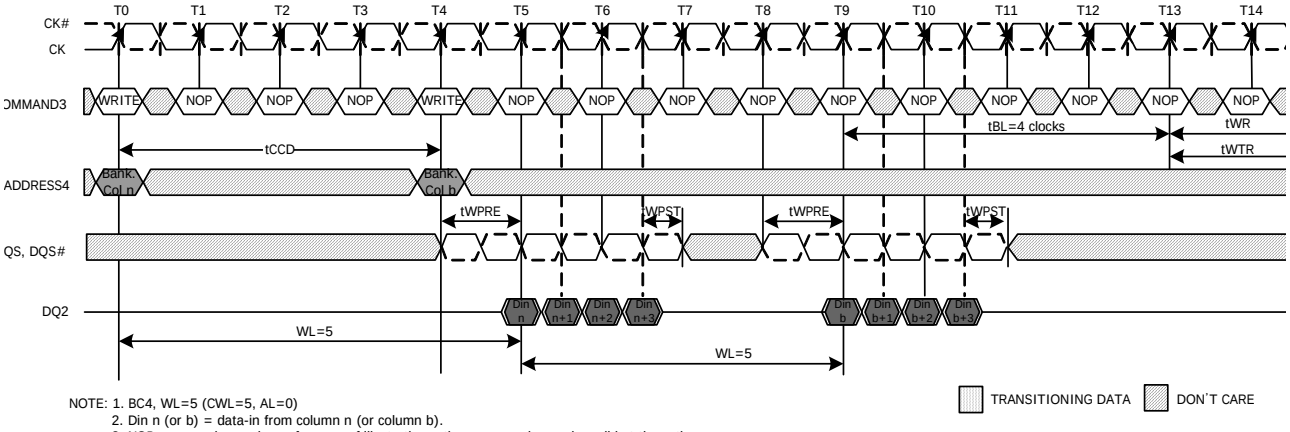
NOTE: 1. RL=5 (CL=5, AL=0), WL=5 (CWL=5, AL=0)
2. Din n = data-in from column n; Dout b= data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on A12 status at T13.

Figure 51. WRITE (BC4) to WRITE (BC4) OTF



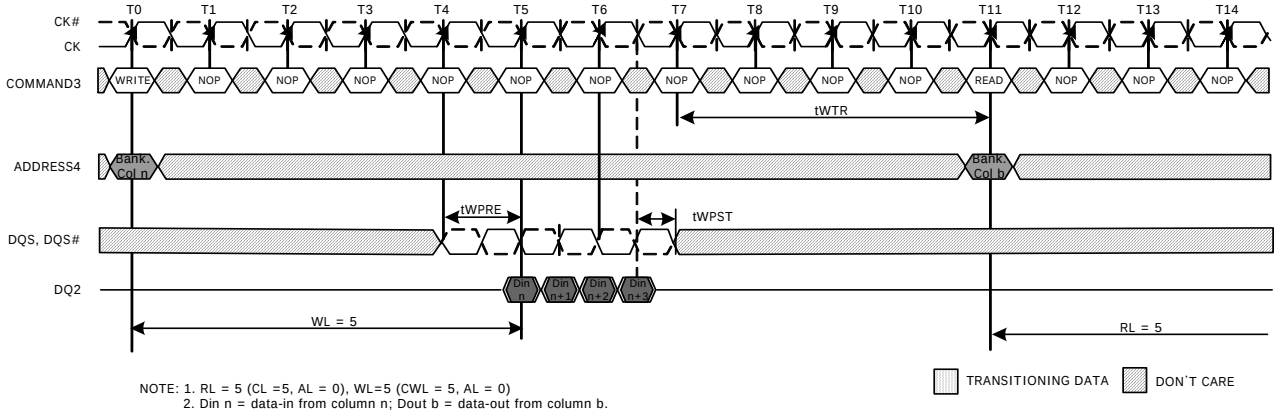
NOTE: 1. BL8, WL=5 (CWL=5, AL=0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12=1 during WRITE command at T0 and T4.

Figure 52. WRITE (BL8) to READ (BC4/BL8) OTF



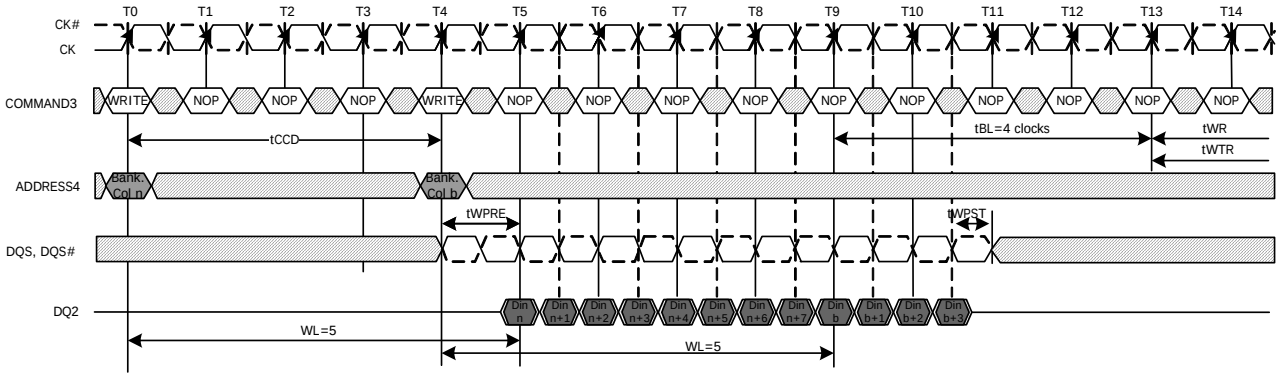
NOTE: 1. BC4, WL=5 (CWL=5, AL=0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during WRITE command at T0 and T4.

Figure 53. WRITE (BC4) to READ (BC4/BL8) OTF



NOTE: 1. RL = 5 (CL =5, AL = 0), WL=5 (CWL = 5, AL = 0)
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10].

Figure 54. WRITE (BC4) to READ (BC4)



NOTE: 1. WL=5 (CWL=5, AL=0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=01] and A12=1 during WRITE command at T0.
BC4 setting activated by either MR0[A1:0=01] and A12=0 during WRITE command at T4.

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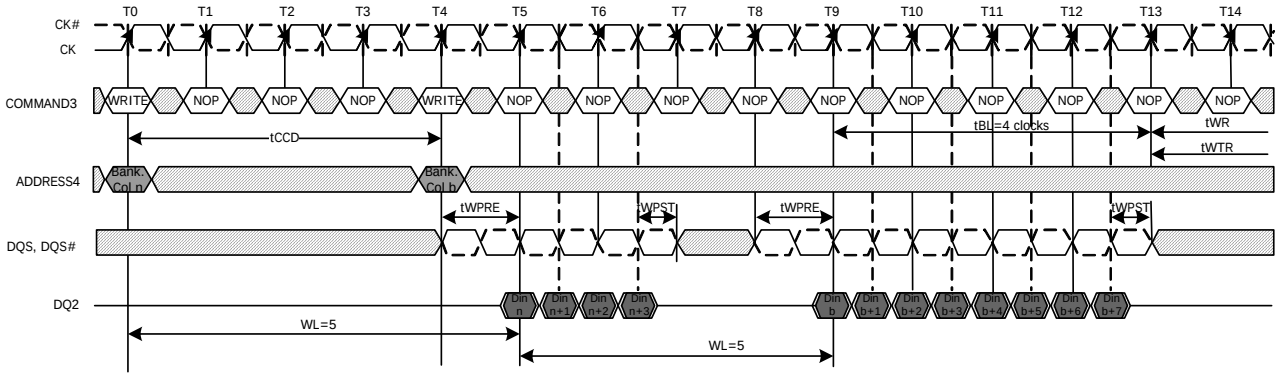
Figure 55. WRITE (BL8) to WRITE (BC4) OTF



NOTE: 1. WL=5 (CWL=5, AL=0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=01] and A12=0 during WRITE command at T0.
BL8 setting activated by either MR0[A1:0=01] and A12=1 during WRITE command at T4.

TRANSITIONING DATA DON'T CARE

Figure 56. WRITE (BC4) to WRITE (BL8) OTF

2.15 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When $\overline{CS}$,$\overline{RAS}$, and $\overline{CAS}$ are held Low and $\overline{WE}$ High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP (min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure 57. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 x tREFI (see Figure 58). A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 x tREFI (see Figure 59). At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI. Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Reresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

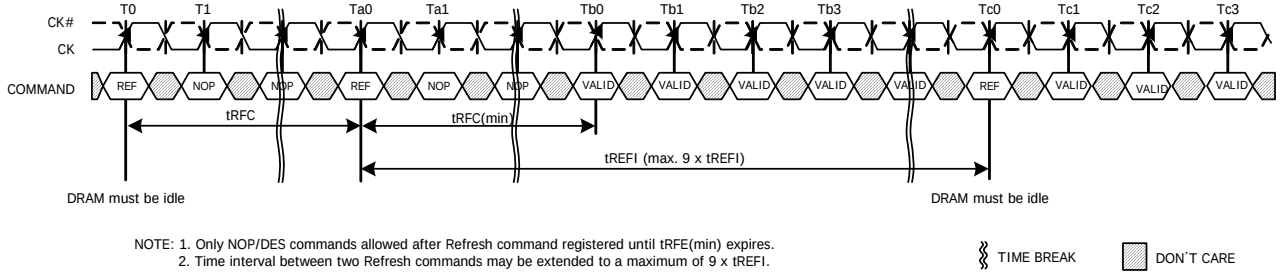


Figure 57. Refresh Command Timing

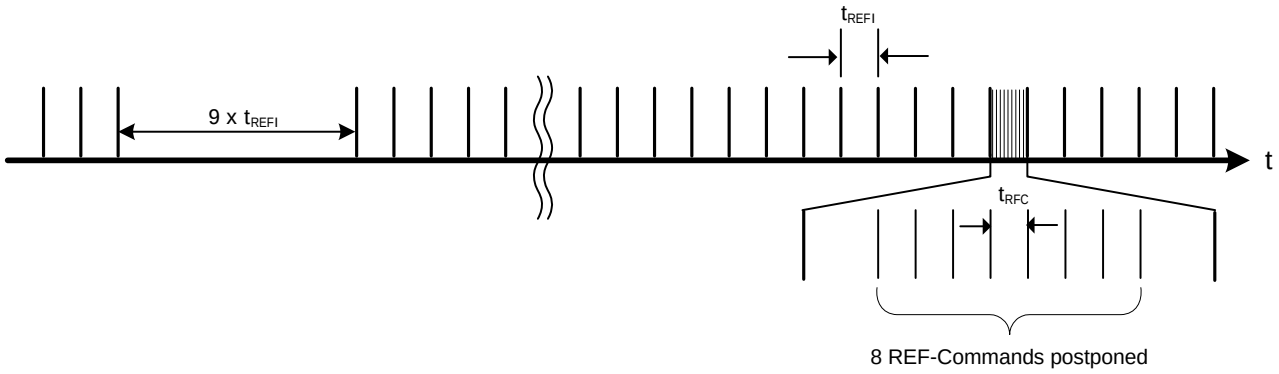


Figure 58. Postponing Refresh Commands (Example)

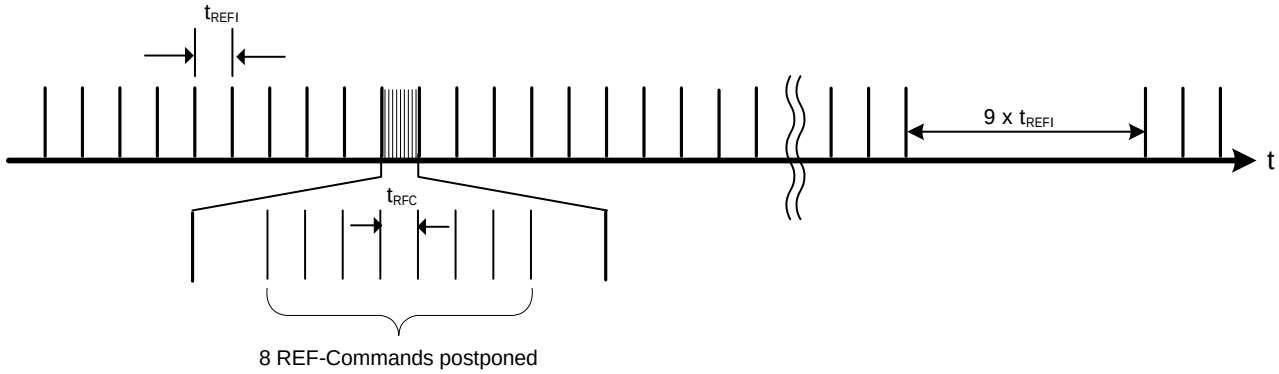


Figure 59. Pulling-in Refresh Commands (Example)

2.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and CKE held low with $\overline{WE}$ high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low “ODTL + 0.5tCK” prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1(A0=0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

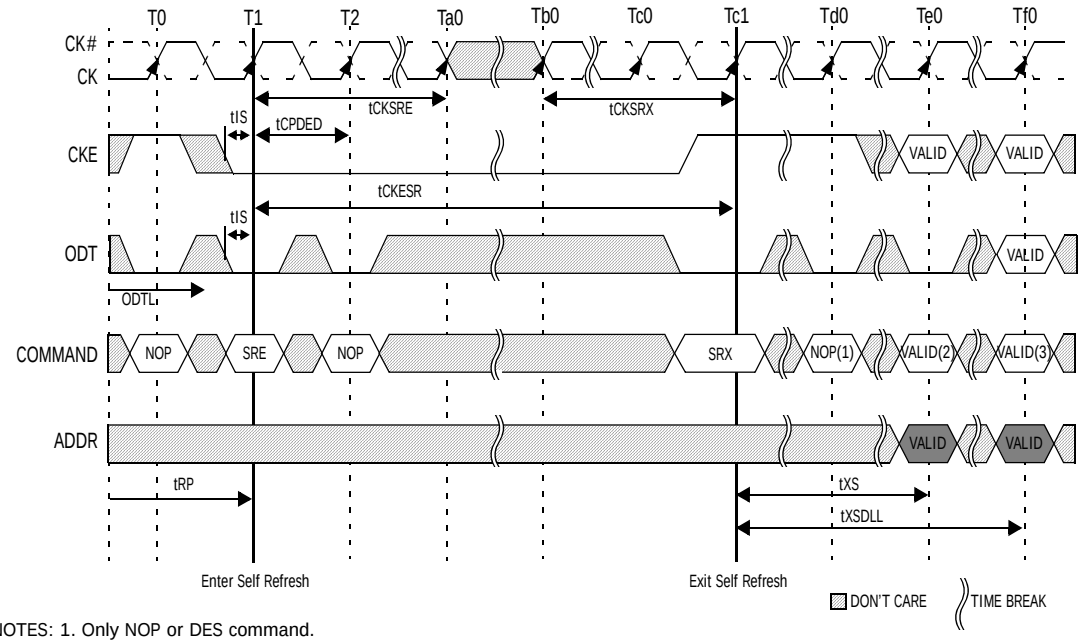
When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and $\overline{RESET}$, are “don’t care”. For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA and VRefDQ) must be at valid levels. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during self-Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self-Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Sell-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied. Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in “ZQ Calibration Commands” on page 76. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure 74 - “ZQ Calibration Timing” on page 108).

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL.



NOTES: 1. Only NOP or DES command.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

Figure 60. Self-Refresh Entry/Exit Timing

2.17 Power-Down Modes

2.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 61 through Figures 73 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT, CKE and $\overline{RESET}$. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

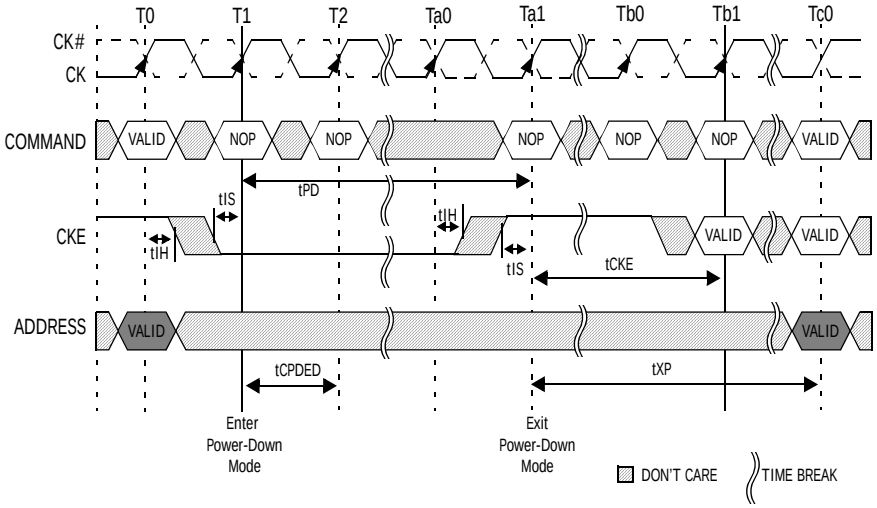
Table 22. Power-Down Entry Definitions

Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	**tXP** to any valid command
Precharged (All banks Precharged)	0	Off	Slow	**tXP** to any valid command. Since it is in precharge state, commands here will be ACT,REF,MRS,PRE or PREA. **tXPDLL** to commands that need the DLL to operate, such as RD,RDA or ODT control line.
Precharged (All banks Precharged)	1	On	Fast	**tXP** to any valid command.

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, $\overline{RESET}$ high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care" (If $\overline{RESET}$ goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined in the AC specifications table of this data sheet.

Active Power Down Entry and Exit timing diagram example is shown in Figure 61. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 62 through Figure 70. Additional clarifications are shown in Figure 71through Figure 73.



NOTE: VALID command at T0 is ACT, NOP, DES or PRE with still on bank remaining open after completion of the precharge command.

Figure 61. Active Power-Down Entry and Exit Timing Diagram

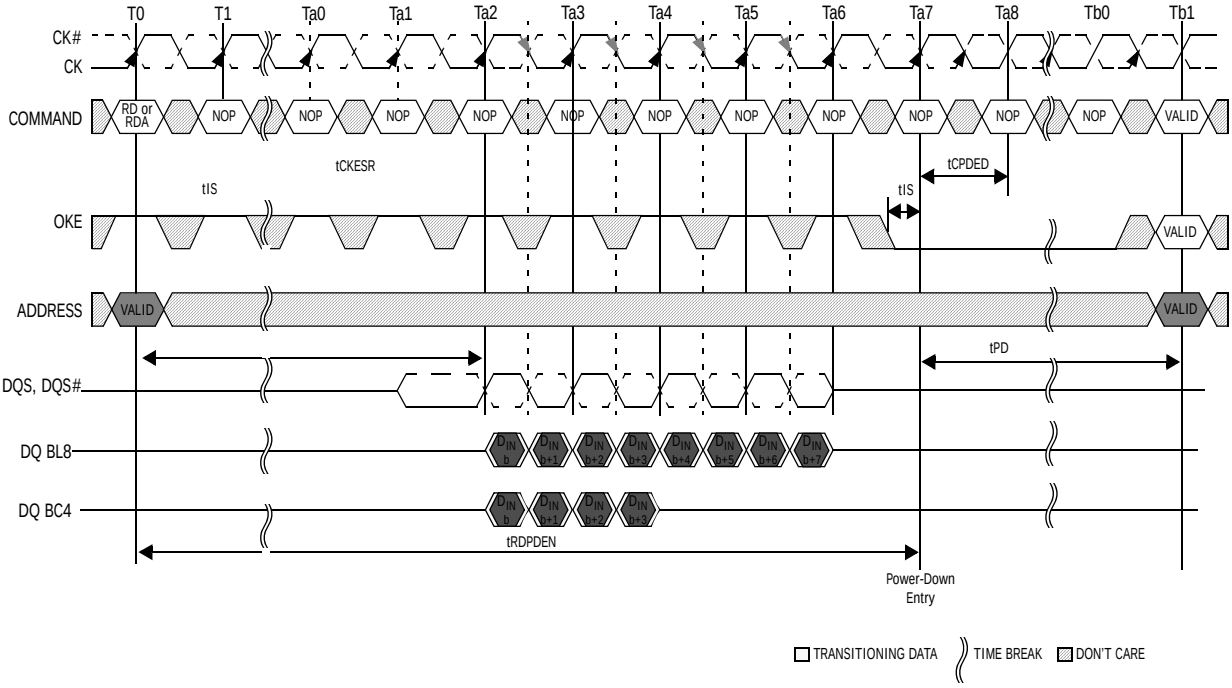
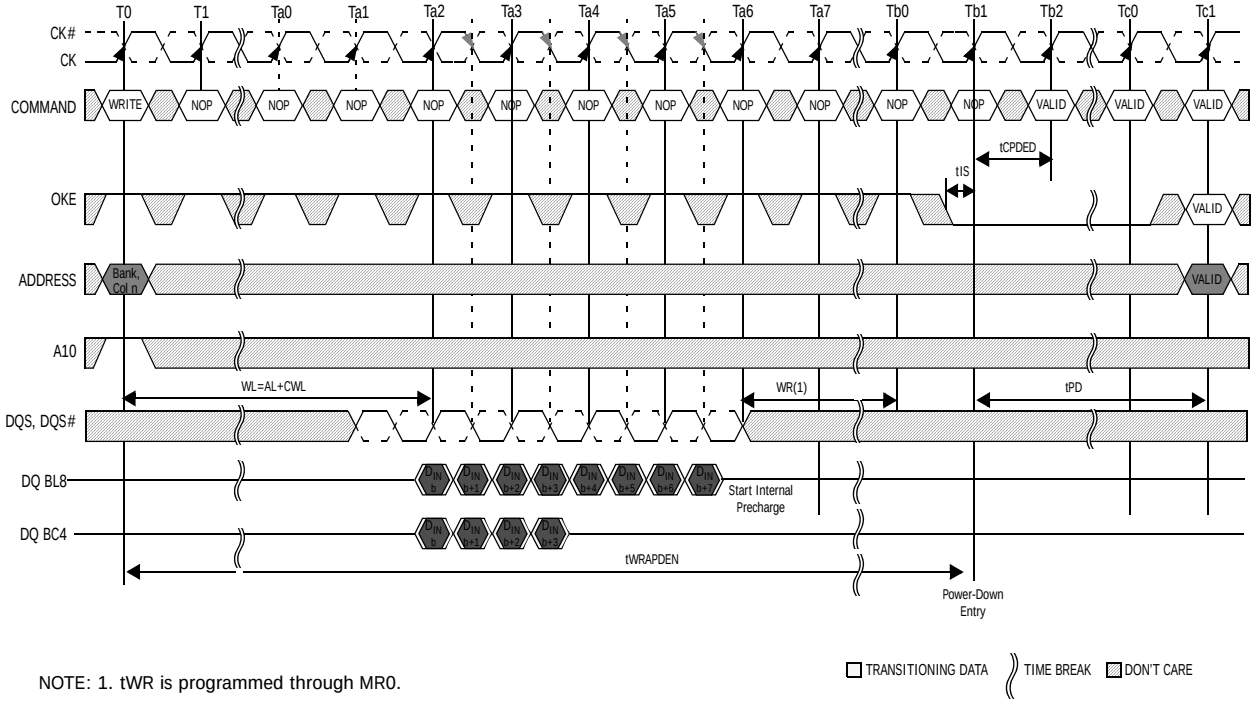


Figure 62. Power-Down Entry after Read with Auto Precharge



NOTE: 1. tWR is programmed through MR0.

Figure 63. Power-Down Entry after Write with Auto Precharge

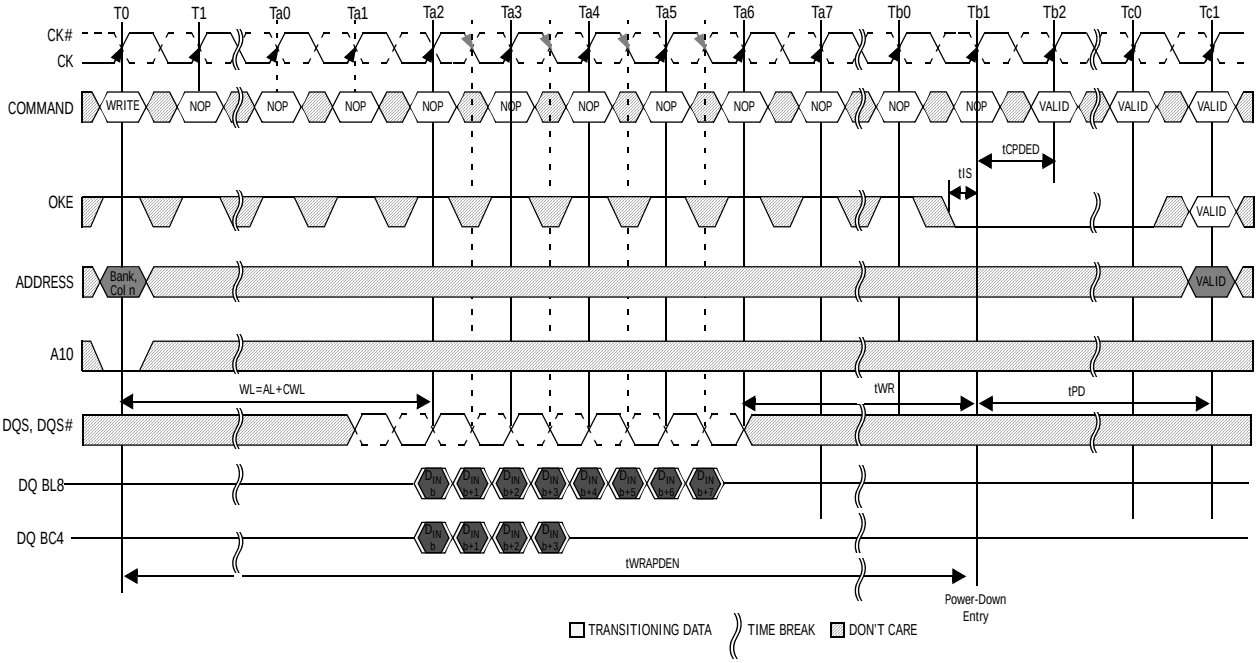


Figure 64. Power-Down Entry after Write

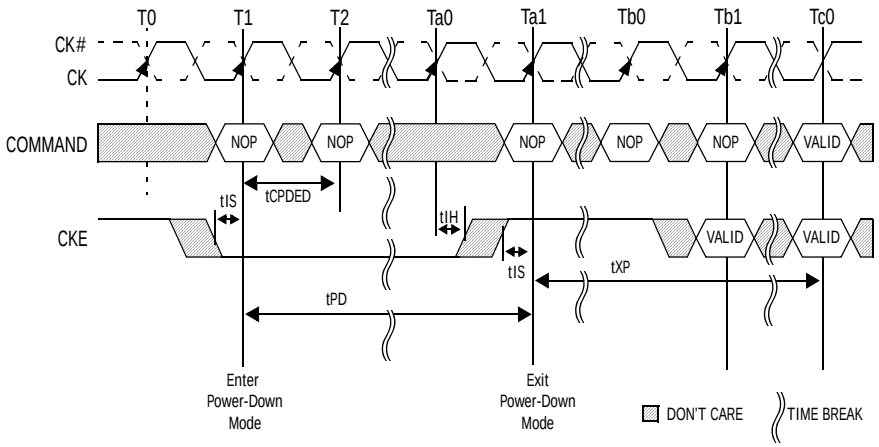


Figure 65. Precharge Power-Down (Fast Exit Mode) Entry and Exit

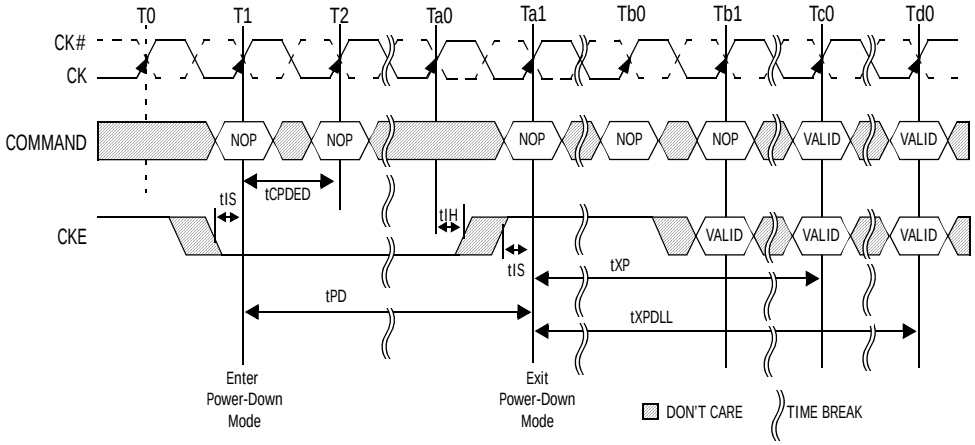


Figure 66. Precharge Power-Down (Slow Exit Mode) Entry and Exit

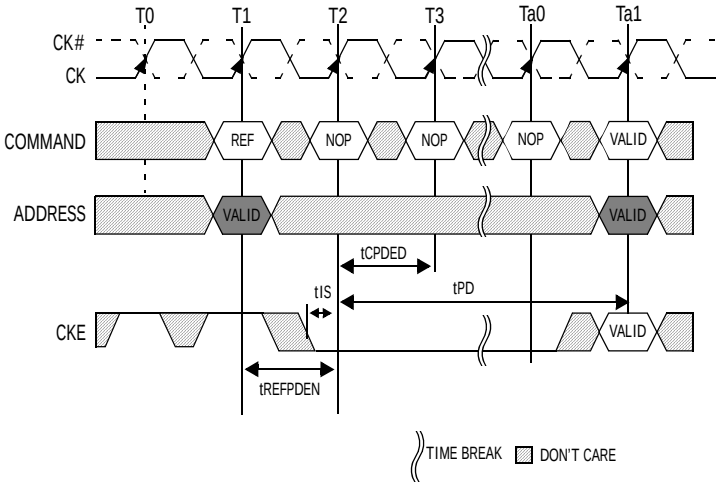


Figure 67. Refresh Command to Power-Down Entry

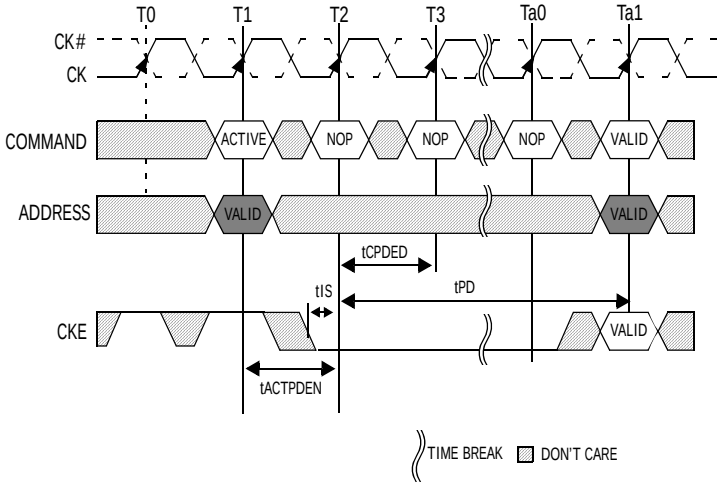


Figure 68. Active Command to Power-Down Entry

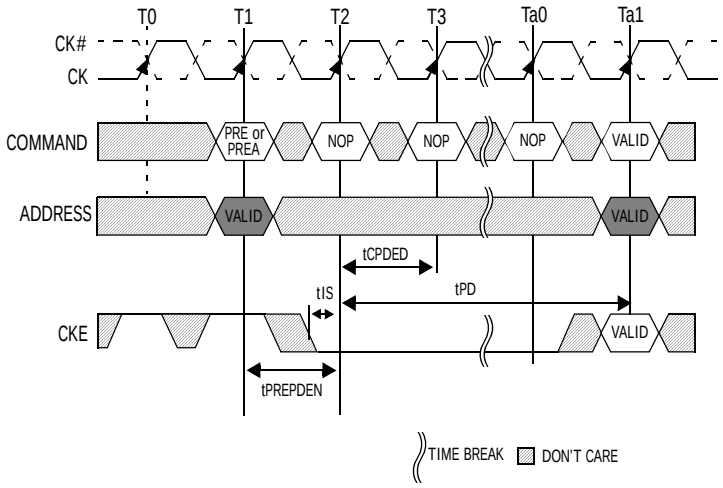


Figure 69. Precharge/Precharge all Command to Power-Down Entry

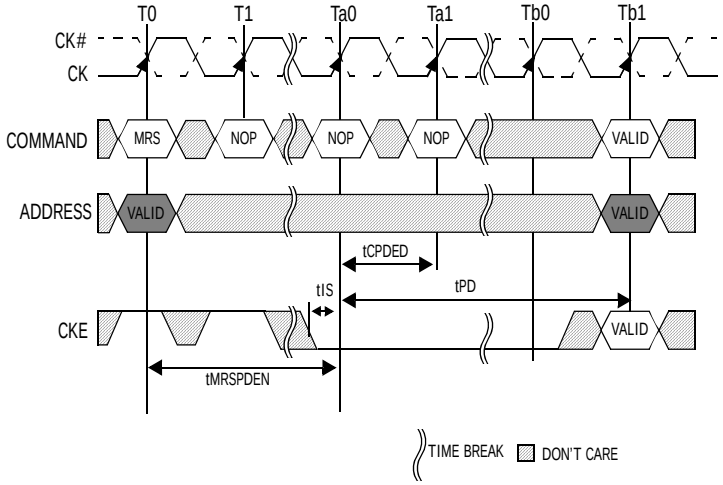


Figure 70. MRS Command to Power-Down Entry

2.17.2 Power-Down clarifications - Case 1

When CKE is registered low for power-down entry, tPD (min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD (min) is equal to the minimum value of parameter tCKE(min) as shown in Table 52, Timing Parameters by Speed Bin. A detail example of Case 1 is shown figure 71.

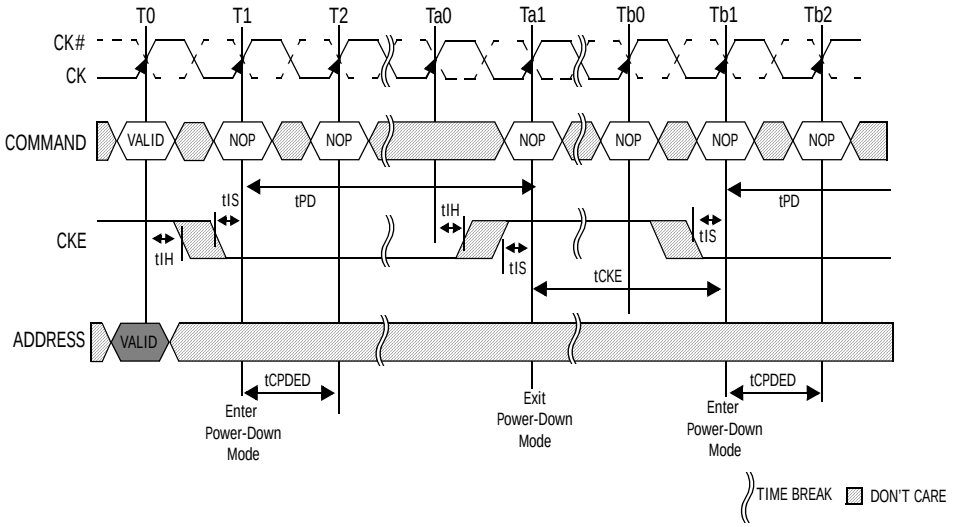


Figure 71. Power-Down Entry/Exit Clarifications - Case1

2.17.3 Power-Down clarifications - Case 2

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequences, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to tCKE in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met: 1) tXP must be satisfied before issuing the command. 2) tXPDLL must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 72.

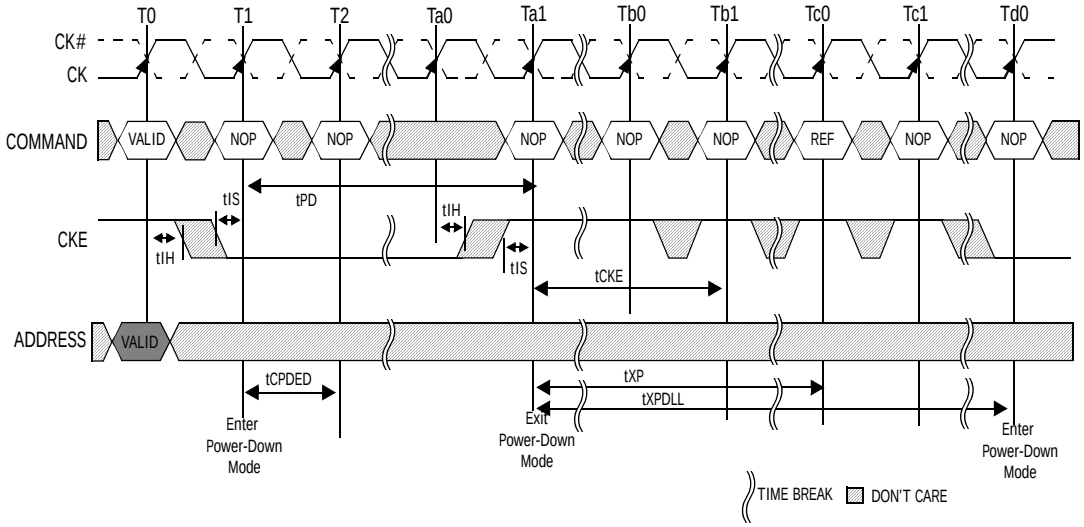


Figure 72. Power-Down Entry/Exit Clarifications - Case2

2.17.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until tRFC(min) from the Refresh command is satisfied. This means CKE can not be registered low twice within a tRFC(min) window. A detailed example of Case 3 is shown in Figure 73.

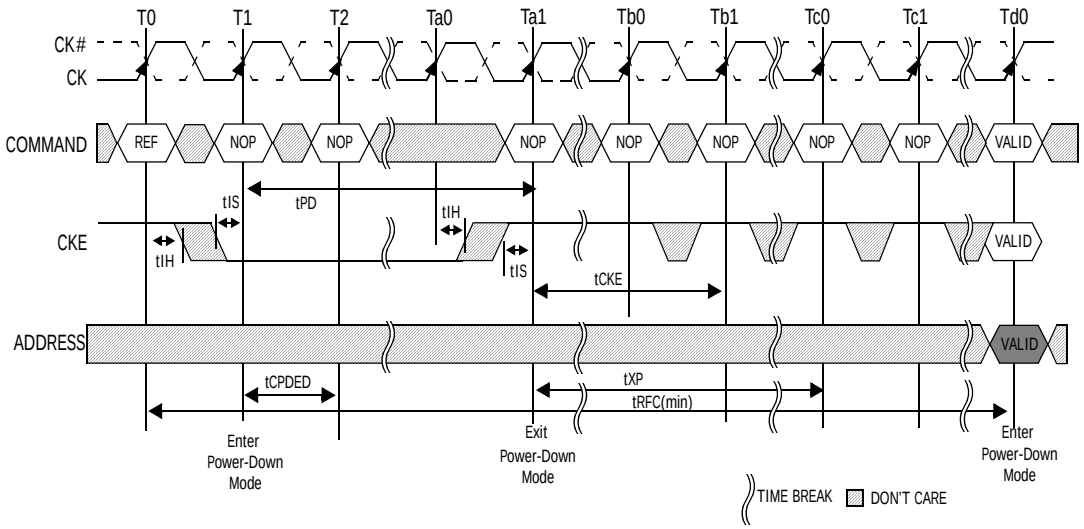


Figure 73. Power-Down Entry/Exit Clarifications - Case3

2.18 ZQ Calibration Commands

2.18.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.One ZQCS command can effectively correct a minimum of 0.5%(ZQcorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max (dRTTdT, dRONdTM) and VSens = max (dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5%/℃, VSens = 0.15%/mV, Tdriftrate = 1℃/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\,ms$$

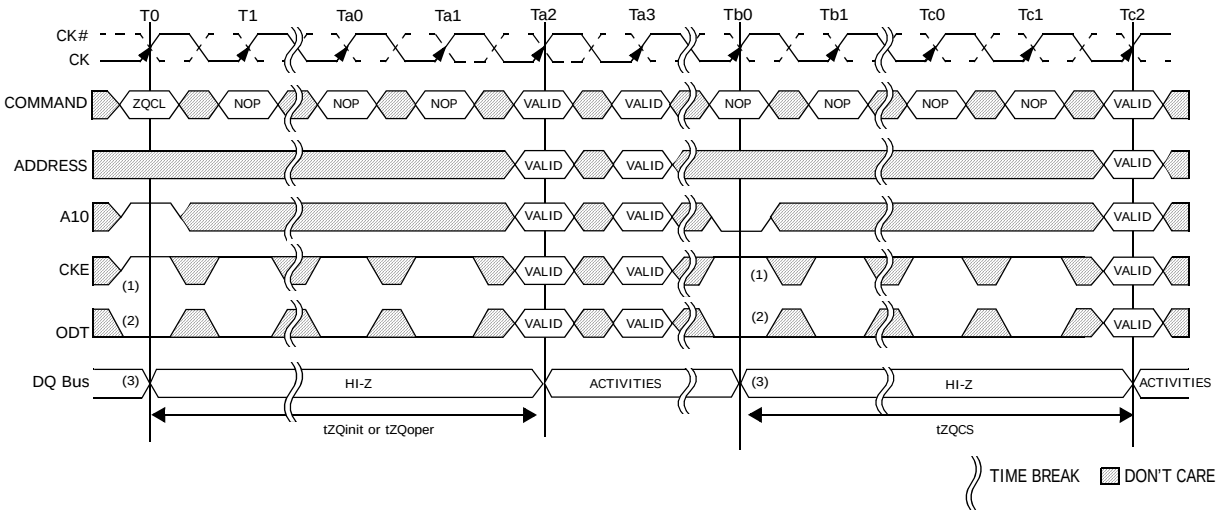
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. Sea Table 14 "Command Truth Table" on page 50 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper , tZQinit or tZQCS between the devices.

2.18.2 ZQ Calibration Timing



NOTE: 1. CKE must be continuously registered high during the calibration procedure.
2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.
3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

Figure 74. ZQ Calibration Timing

2.18.3 ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm+/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited (See “Input / Output Capacitance” on each datasheet).

3. On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$ and DM for x4 and x8 configuration (and *TDQS, $\overline{\text{TDQS}}$ for X8 configuration, when enabled via A11=1 in MR1)* via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document:

- The ODT control modes are described in 3.1.
- The ODT synchronous mode is described in 3.2.
- The dynamic ODT feature is described in 3.3.
- The ODT asynchronous mode is described in 3.4
- The transitions between ODT synchronous and asynchronous are described in 3.4.1 through 3.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 75.

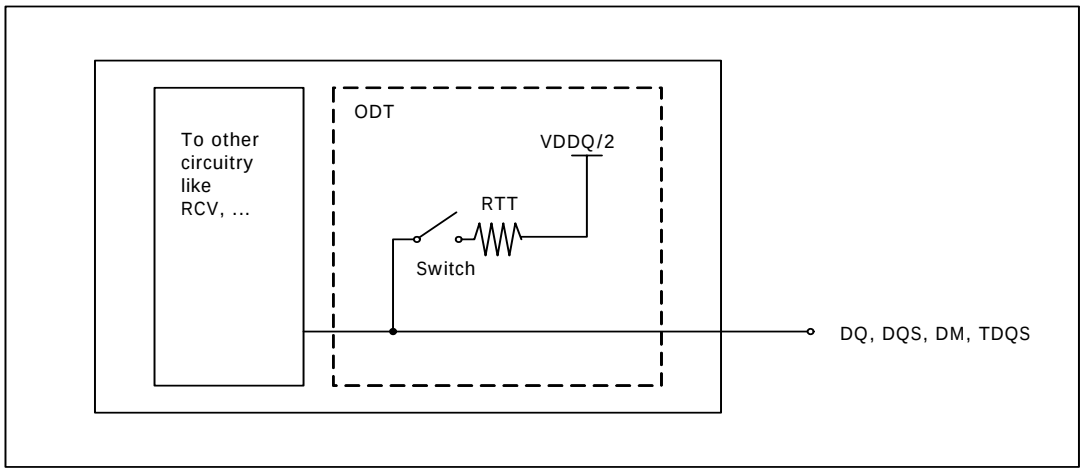


Figure 75. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 9 on page 44 and Figure 10 on page 47). The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

3.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 {A9, A6, A2} or MR2 {A10, A9} are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure 9 on page 44).

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 23.

Table 23. Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	On, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general)

3.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL -2.

3.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2;
ODTLoff = CWL + AL - 2. For details, refer to ODT Timing Parameters listed in Table 52 on page 150 and Table 53 on page 159.

3.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see also Figure 76):

ODTLon, ODTLoff, $t_{AON,min,max}$, $t_{AOF,min,max}$.

Minimum RTT turn-on time (t_{AON}min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AON}max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (t_{AOF}min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (t_{AOF}max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 77). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

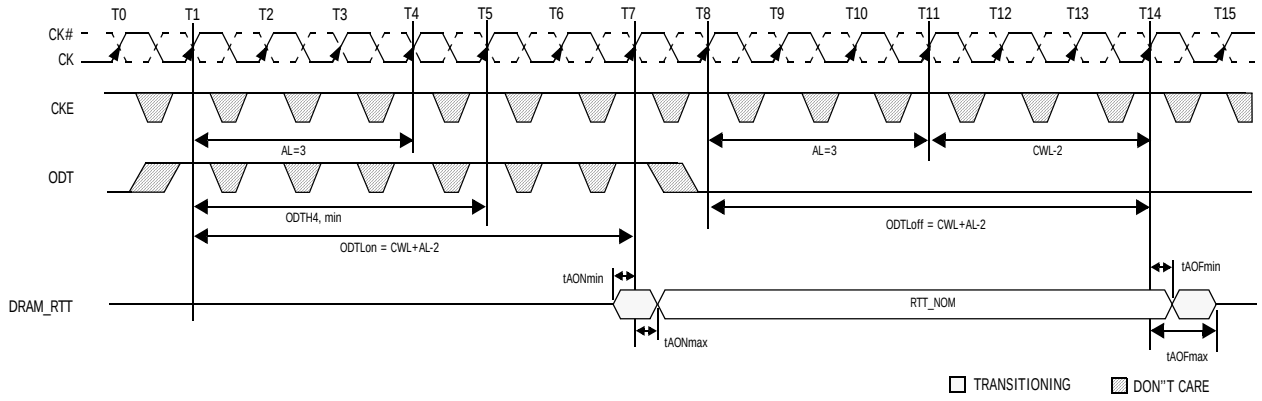


Figure 76. Synchronous ODT Timing Example for AL=3; CWL=5; ODTLon = AL+CWL-2=6.0; ODTLoff = AL+CWL-2=6

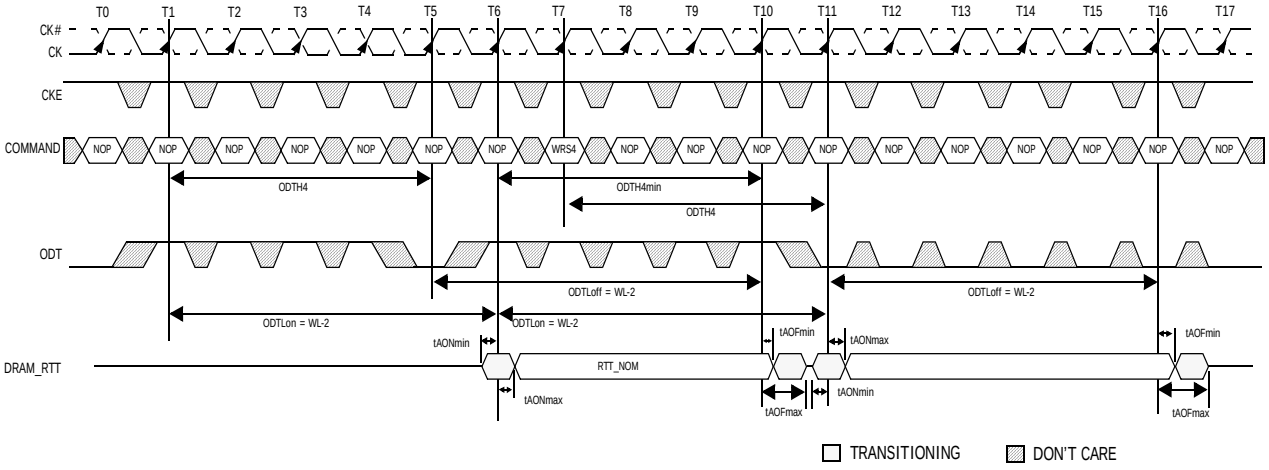


Figure 77. Synchronous ODT example with BL=4, WL=7

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL = 4) or ODTH8 (BL = 8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6, ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

3.2.3 ODT during Reads

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the example below. As shown in Figure 78 below at cycle T15, DRAM turns on the termination when it stops driving, which is determined by tHZ. If DRAM stops driving early (i.e., tHZ is early), then tAONmin timing may apply. If DRAM stops driving late (i.e., tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 78.

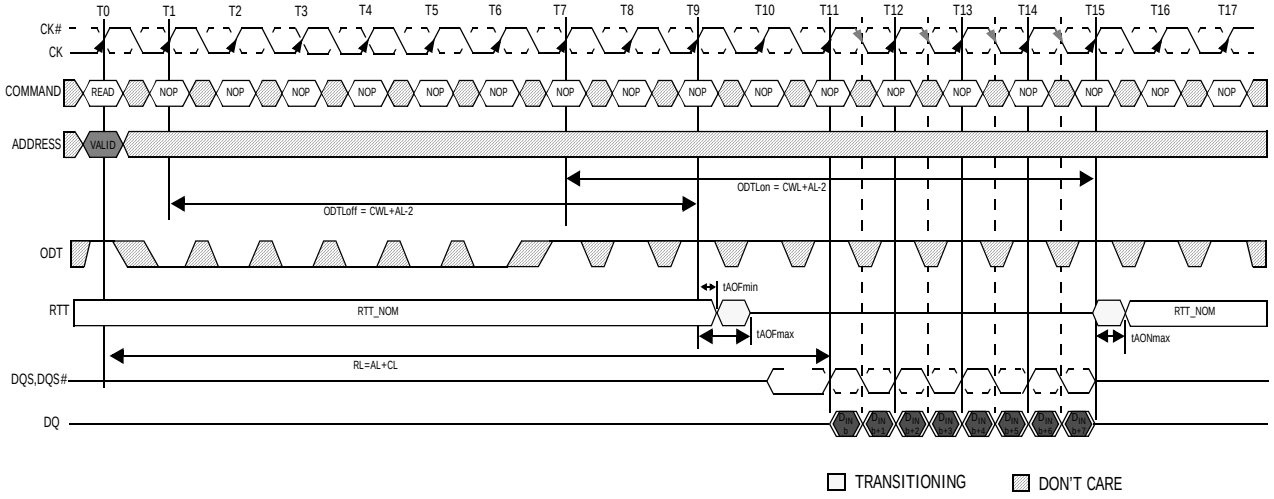


Figure 78. ODT must be disabled externally during Reads by driving ODT low. (example: CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon = CWL+AL-2=8; ODTLoff = CWL+AL-2=8)

3.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

3.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ’1’. The function is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
  - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.
  - The value for RTT_WR is preselected via bits A[10,9] in MR2.
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 25 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 77). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

Table 24. Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined From	Defined to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon = WL - 2	t_{CK}
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff = WL - 2	t_{CK}
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL - 2	t_{CK}
ODT Latency for change from RTT_WR to RTT_Nom(BL=4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4= 4+ODTLoff	t_{CK}
ODT Latency for change from RTT_WR to RTT_Nom(BL=8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8= 6+ODTLoff	t_{CK} (avg)

Table 24. Latencies and timing parameters relevant for Dynamic ODT (Cont'd)

Name and Description	Abbr.	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
minimum ODT high time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 = 4	t_{CK}(avg)
minimum ODT high time after Write (BL = 4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 = 4	t_{CK}(avg)
minimum ODT high time after Write (BL = 8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 = 6	t_{CK}(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min)=0.3*tCK(avg) tADC(max)=0.7*tCK(avg)	t_{CK}(avg)

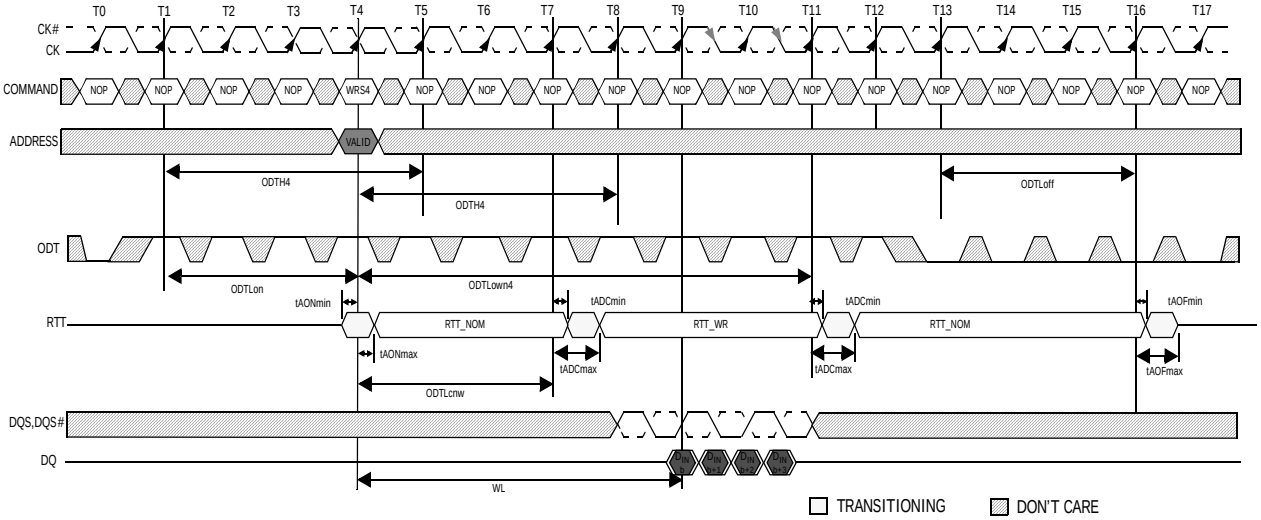
Note: tAOF, nom and tADC,nom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

3.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 25:

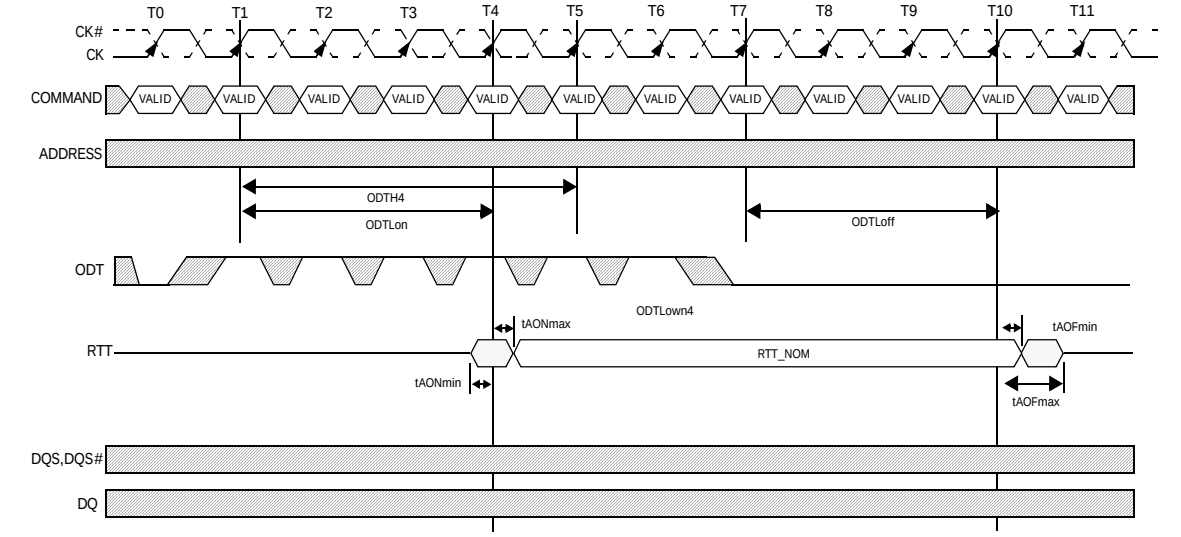
Table 25. Timing Diagrams for "Dynamic ODT"

Figure and Page	Description
Figure 79 on page 114	Figure 79, Dynamic ODT: Behavior with ODT being asserted before and after the write.
Figure 80 on page 114	Figure 80, Dynamic ODT: Behavior without write command, AL = 0, CWL = 5.
Figure 81 on page 115	Figure 81, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles.
Figure 82 on page 115	Figure 82, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.
Figure 83 on page 116	Figure 83, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles.



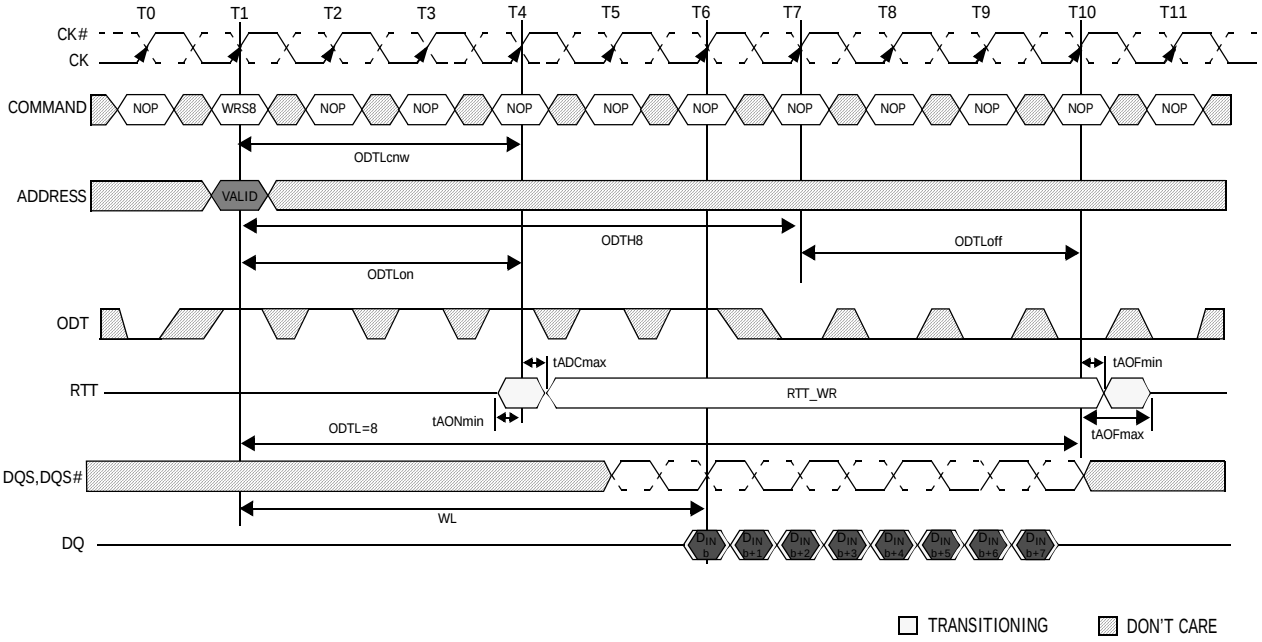
NOTE: Example for BC4 (via MRS or OTF), AL=0, CWL=5. ODTH4 applies to first registering ODT high and to the registration of the Write command. In this example, ODTH4 would be satisfied if ODT went low at T8(4 clocks after the Write command).

Figure 79. Dynamic ODT: Behavior with ODT being asserted before and after the write



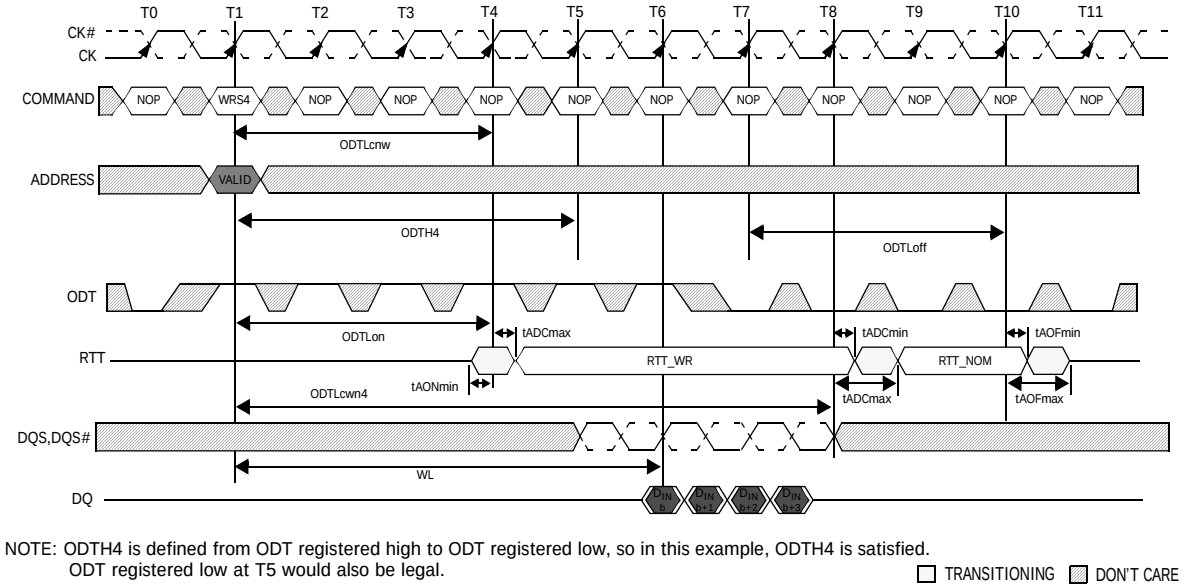
NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
ODT registered low at T5 would also be legal.

Figure 80. Dynamic ODT: Behavior without write command, AL=0, CWL=5



NOTE: Example for BL8 (via MRS or OTF), AL=0, CWL=5. In this example, ODTH8=6 is exactly satisfied.

Figure 81. Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles



NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
ODT registered low at T5 would also be legal.

Figure 82. Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL=0, CWL=5.

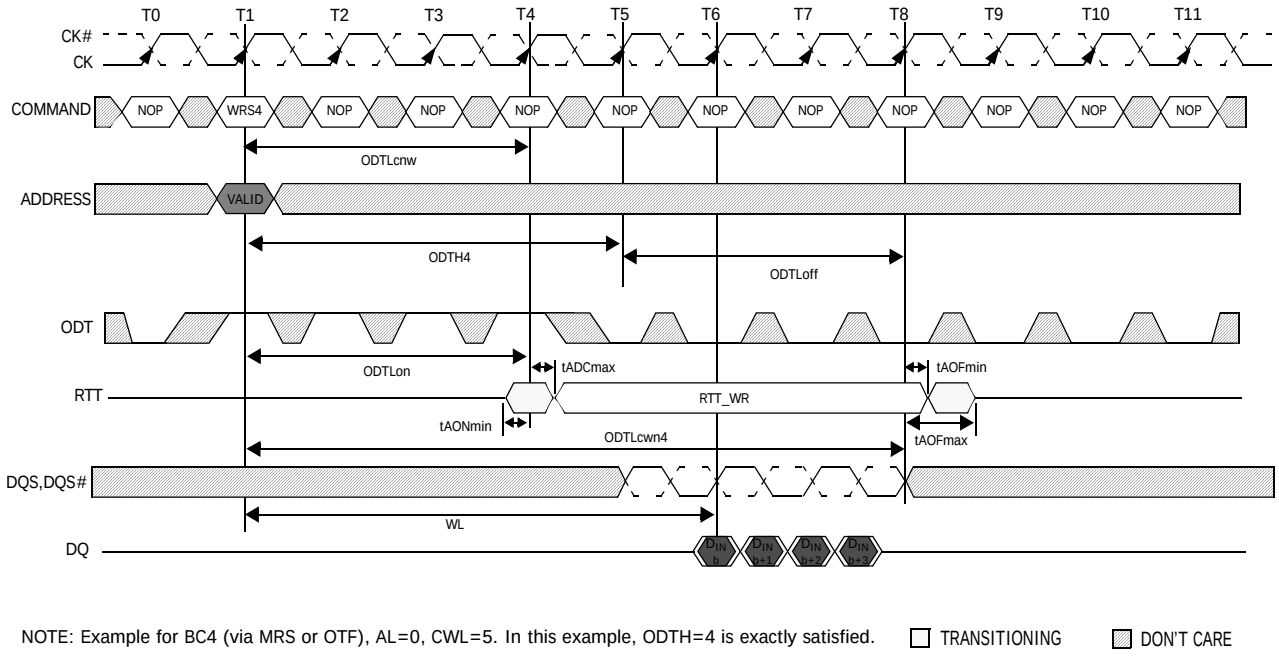


Figure 83. Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles

3.4 Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently (comment: update editorially after everything is set and done...): Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see Figure 84): $t_{AONPD,min,max}$, $t_{AOFPD,min,max}$.

Minimum RTT turn-on time (t_{AONPD}min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AONPD}max) is the point in time when the ODT resistance is fully on.

t_{AONPD}min and t_{AONPD}max are measured from ODT being sampled high.

Minimum RTT turn-off time (t_{AOFPD}min) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (t_{AOFPD}max) is the point in time when the on-die termination has reached high impedance. t_{AOFPD}min and t_{AOFPD}max are measured from ODT being sampled low.

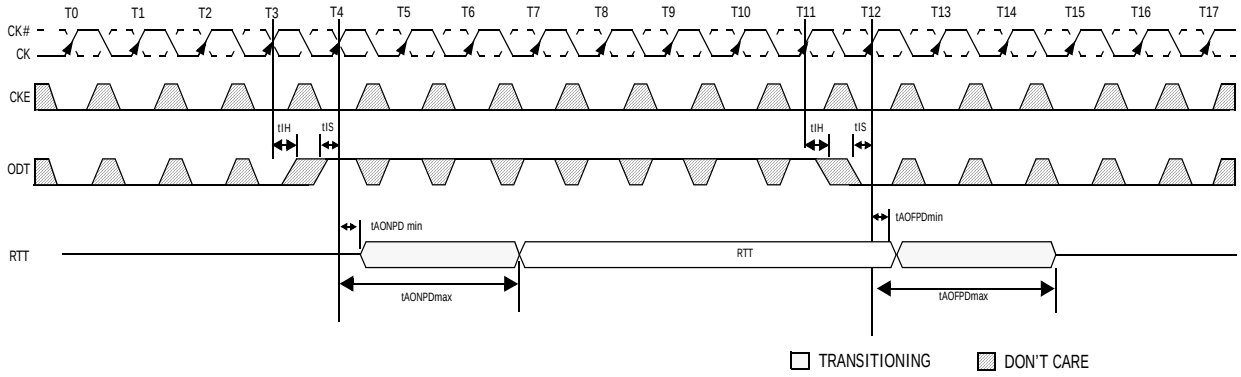


Figure 84. Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

Table 26. Asynchronous ODT Timings Parameters for all Speed Bins

Symbol	Description	min	max	Unit
t_{AONPD}	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

3.4.1 Synchronous to Asynchronous ODT Mode Transitions

Table 27. ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	min	max
ODT to RTT turn-on delay	min {ODTLon * tCK + tAONmin; tAONPDmin}	max {ODTLon * tCK + tAONmax; tAONPDmax}
	min {(WL-2) * tCK + tAONmin; tAONPDmin}	min {(WL-2) * tCK + tAONmax; tAONPDmax}
ODT to RTT turn-off delay	min {ODTLoff * tCK + tAOFmin; tAOFPDmin}	min {ODTLoff * tCK + tAOFmax; tAOFPDmax}
	min {(WL-2) * tCK + tAOFmin; tAOFPDmin}	min {(WL-2) * tCK + tAOFmax; tAOFPDmax}
tANPD	WL-1	

3.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min) as shown in Figure 85. If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED (min) as shown in Figure 86. Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end points at tCPDED(min) and tRFC(min), respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD}min and (ODTLon*t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD}max and (ODTLon*t_{CK} + t_{AON}max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD}min and (ODTLof*t_{CK} + t_{AOF}min) and as late as the larger of t_{AOFPD}max and (ODTLoff*t_{CK} + t_{AOF}max). See Figure 18 and Figure 85. Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 85 shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

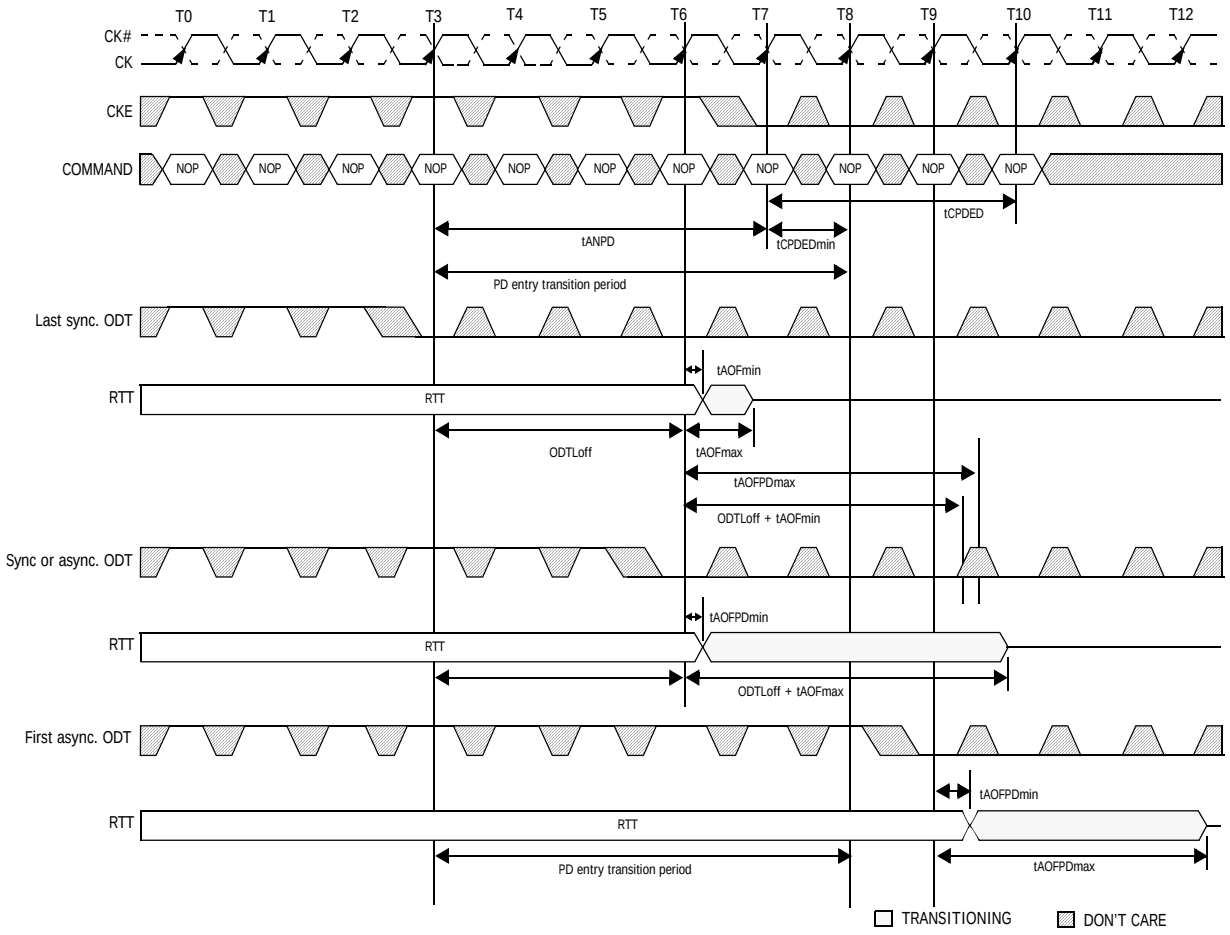


Figure 85. Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL=0; CWL=5; tANPD = WL-1=4)

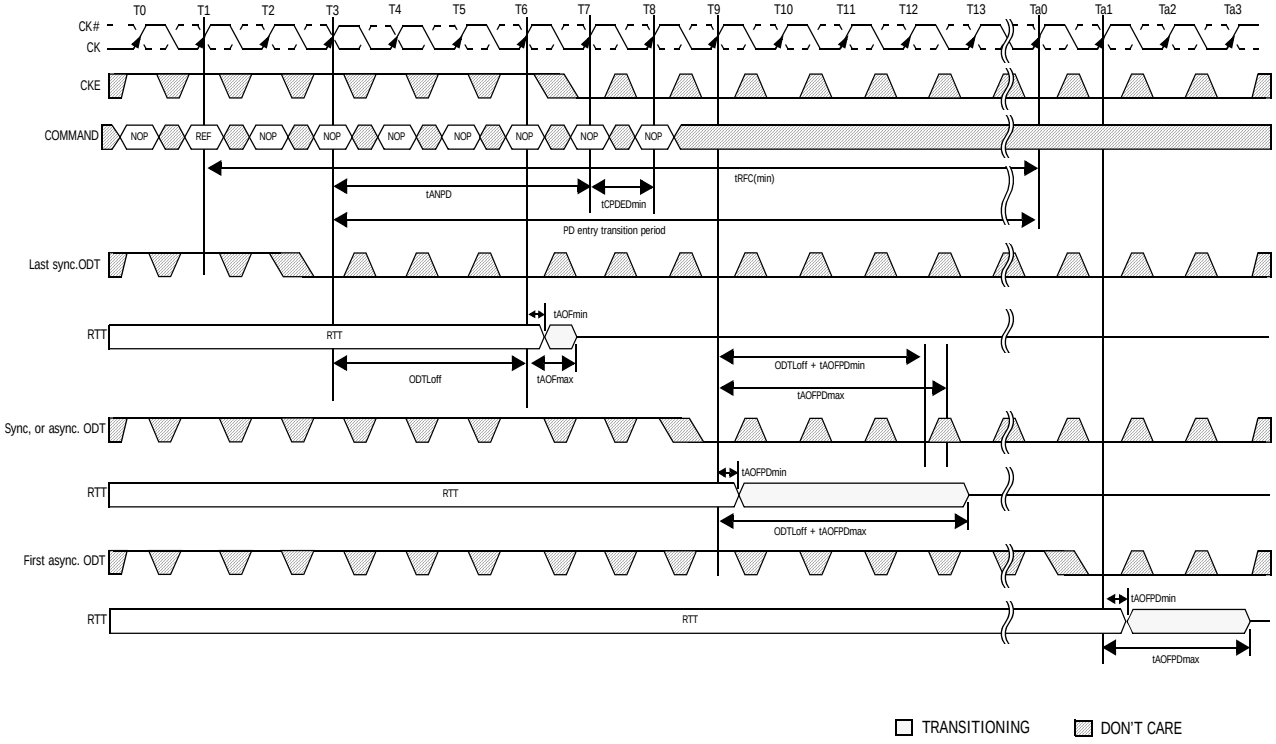


Figure 86. Synchronous to asynchronous transition after Refresh command (AL=0; CWL=5; tANPD = WL-1=4)

3.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL - 1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD}min and (ODTLon*t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD}max and (ODTLon*t_{CK} + t_{AON}max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD}min and (ODTLoff *t_{CK} + t_{AOF}min) and as late as the larger of t_{AOFPD}max and (ODTLoff*t_{CK} + t_{AOF}max). See Table 27.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 87 shows the three different cases: ODT_C, asynchronous response before t_{ANPD}; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

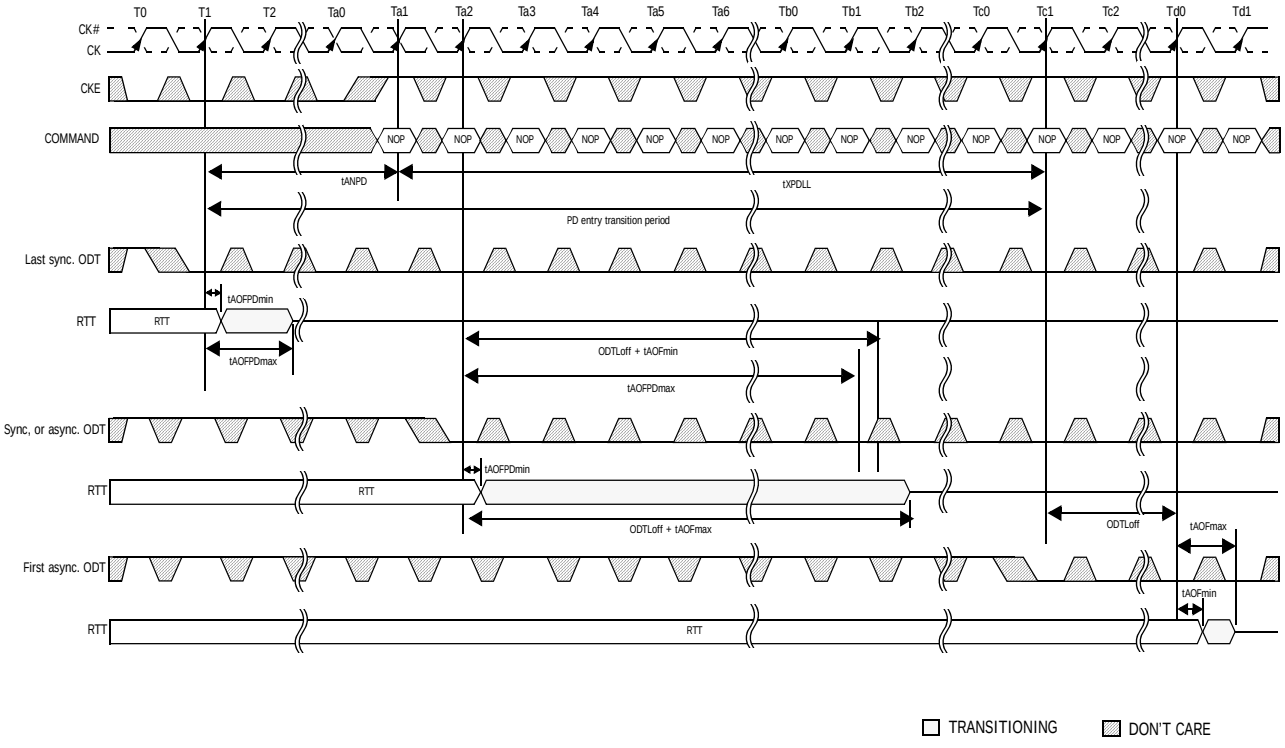


Figure 87. Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; tANPD = WL - 1=9)

3.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap (see Figure 88). In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that in the bottom part of Figure 88 it is assumed that there was no Refresh command in progress when Idle state was entered.

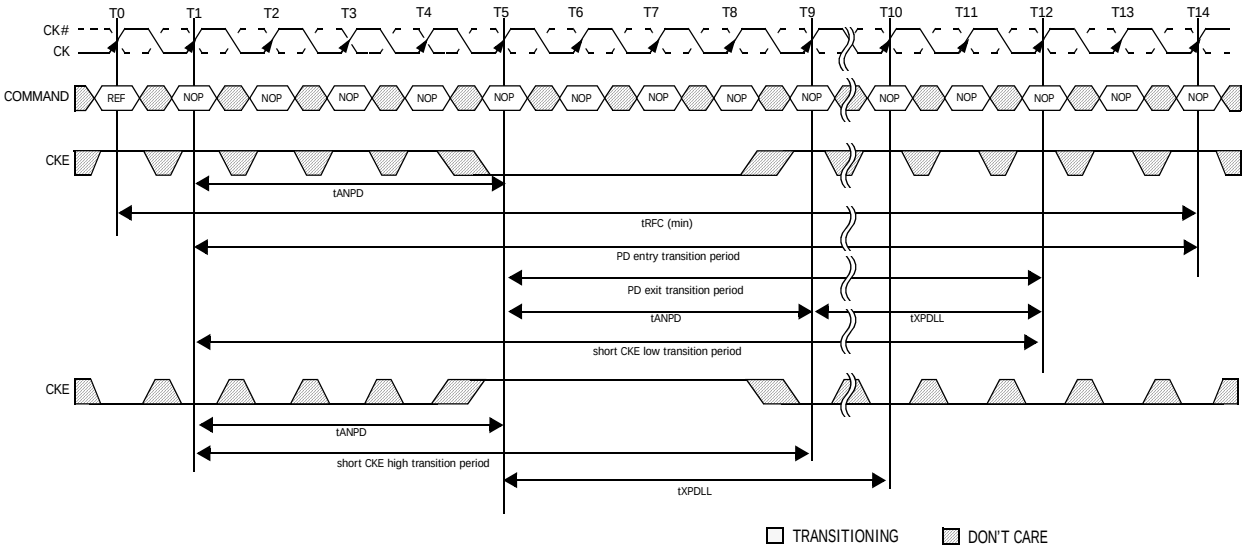


Figure 88. Transition period for short CKE cycles, entry and exit period overlapping (AL=0, WL=5, tANPD = WL-1=4)

4. AC & DC Input Measurement Levels

4.1 AC and DC Logic Input Levels for Single-Ended Signals

4.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 28. Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	Min	Max	Unit	Notes
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1, 5
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1, 6
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note 2	V	1, 2, 7
VIL.CA(AC175)	AC input logic low	Note 2	Vref - 0.175	V	1, 2, 8
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V	1, 2, 7
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V	1, 2, 8
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA(DC).
2. See ?$paratext>? on page 135.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC175) and VIH.CA(AC150); VIH.CA(AC175) value is used when Vref+0.175V is referenced and VIH.CA(AC150) value is used when Vref+0.150V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.CA(AC175) and VIL.CA(AC150); VIL.CA(AC175) value is used when Vref-0.175V is referenced and VIL.CA(AC150) value is used when Vref-0.150V is referenced.

4.1.2 AC and DC Input Levels for Single-Ended Data Signals

Table 29. Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	800MHz		900MHz/1.0GHz		Unit	Notes
		Min	Max	Min	Max		
VIH.DQ(AC150)	AC Input logic high	Vref + 0.150	Note 2	-	-	V	1, 2, 7
VIL.DQ(AC150)	AC input logic low	Note 2	Vref - 0.150	-	-	V	1, 2, 8
VIH.DQ(AC135)	AC Input logic high	-	-	Vref+0.135	Note 2	mV	1, 2, 7
VIL.DQ(AC135)	AC input logic low	-	-	Note 2	Vref-0.135	mV	1, 2, 8
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. Vref = VrefDQ(DC).
2. See ?$paratext>? on page 135.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when Vref+0.175V is referenced, VIH.DQ(AC150) value is used when Vref+0.150V is referenced, and VIH.DQ(AC135) value is used when Vref+0.135V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC175) value is used when Vref-0.175V is referenced, VIL.DQ(AC150) value is used when Vref-0.150V is referenced, and VIL.DQ(AC135) value is used when Vref-0.135V is referenced

4.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages $_{VRefCA}$ and V_{RefDQ} are illustrated in below Figure 89. It shows a valid reference voltage V_{Ref} (t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

V_{Ref} (DC) is the linear average of V_{Ref} (t) over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in Table 34. Furthermore V_{Ref} (t) may temporarily deviate from $V_{Ref\ (DC)}$ by no more than +/- 1% VDD.

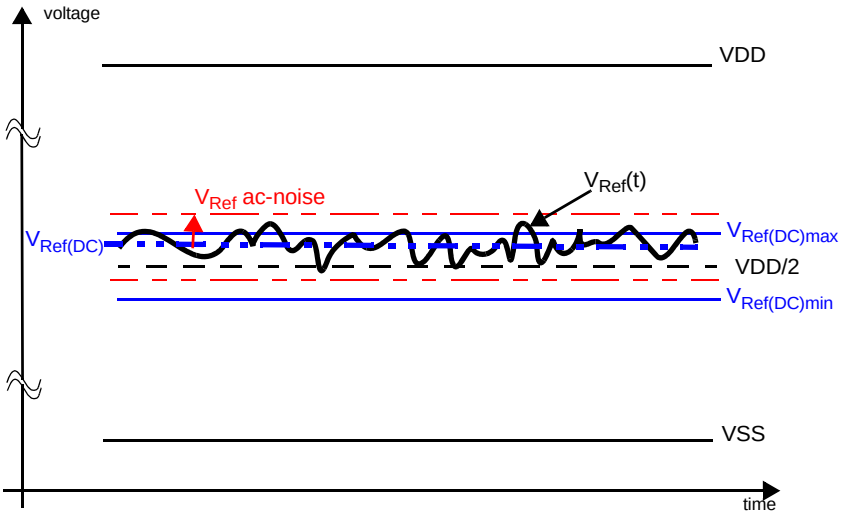


Figure 89. Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in Figure 89.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref}ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

4.3 AC and DC Logic Input Levels for Differential Signals

4.3.1 Differential signal definition

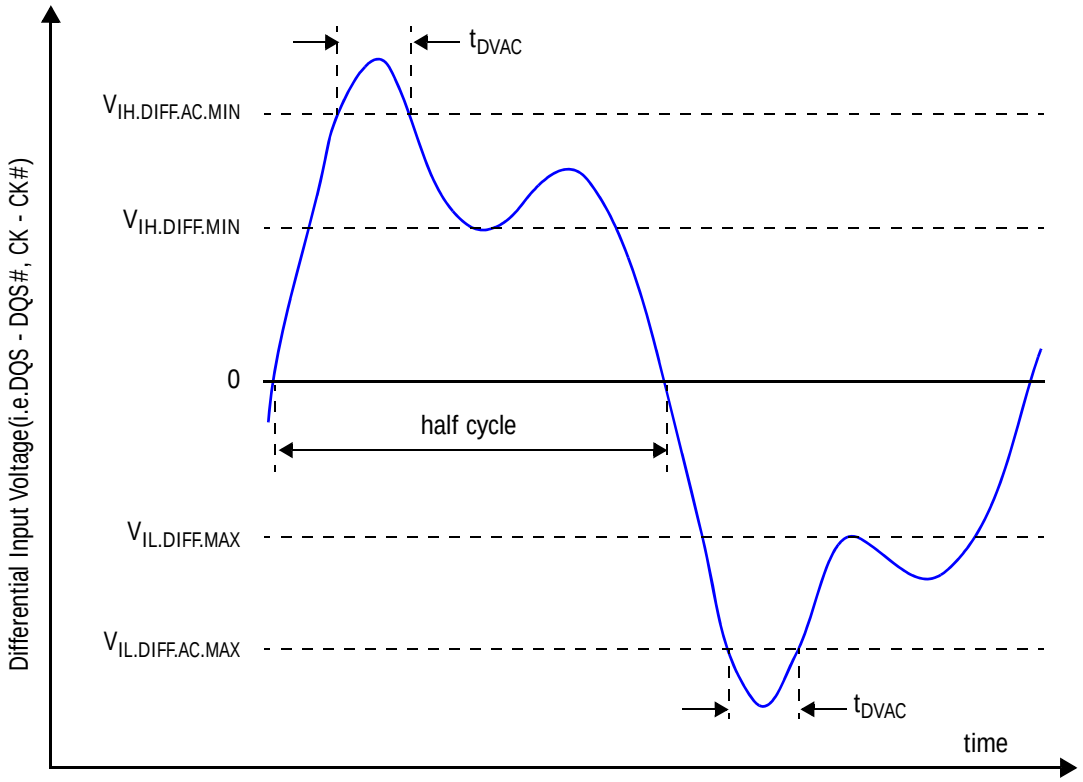


Figure 90. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

4.3.2 Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS-$\overline{DQS}$)

Table 30. Differential AC and DC Input Levels

Symbol	Parameter	800MHz/900MHz/1.0GHz		Unit	Notes
		Min	Max		
VIHdiff	Differential input high	+ 0.200	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.200	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - Vref)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - $\overline{CK}$ use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH(dc) max, VIL(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to ?$paratext>? on page 135.

Table 31. Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

4.3.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, of $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.

CK and CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.

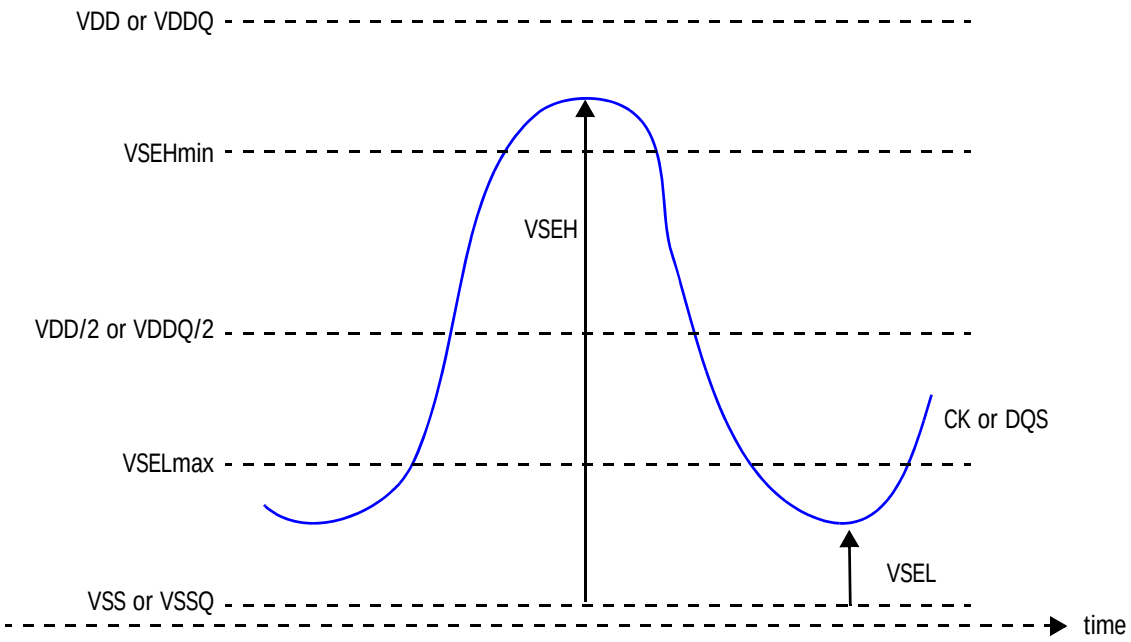


Figure 91. Single-ended requirement for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 32. Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

Symbol	Parameter	800MHz/900MHz/1.0GHz		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1, 2
	Single-ended high level for Ck, $\overline{CK}$	(VDD / 2) + 0.175	Note 3	V	1, 2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) -0.175	V	1, 2
	Single-ended low level for CK, $\overline{CK}$	Note 3	(VDD / 2) -0.175	V	1, 2

Notes:

1. For CK, $\overline{CK}$ use VIH/VIL (ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH(dc) max, VIL(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to ?$paratext>? on page 135.

4.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in Table 33. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

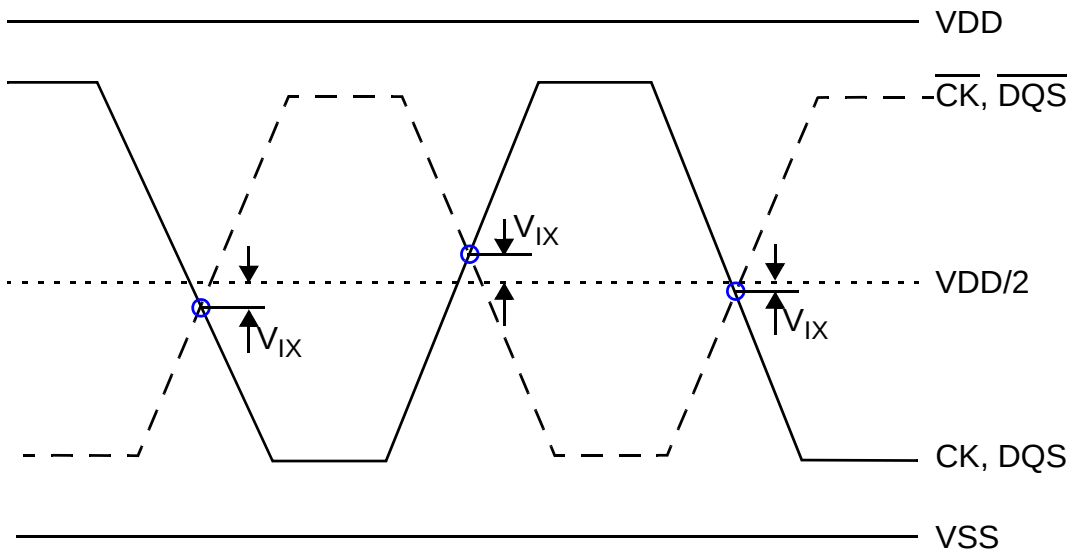


Figure 92. Vix Definition

Table 33. Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	800MHz/900MHz/1.0GHz		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	- 150	150	mV	
		- 175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	- 150	150	mV	

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.
   Refer to Table 32 on page 128 for VSEL and VSEH standard values.

4.5 Slew Rate Definitions for Single-Ended Input Signals

See ?$paratext>? on page 159 for single-ended slew rate definitions for address and command signals.

See ?$paratext>? on page 166 for single-ended slew rate definitions for data signals.

4.6 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in Table 34 and Figure 93.

Table 34. Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	[VIHdiffmin - VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff

Notes:

1. The differential signal (i.e., CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.

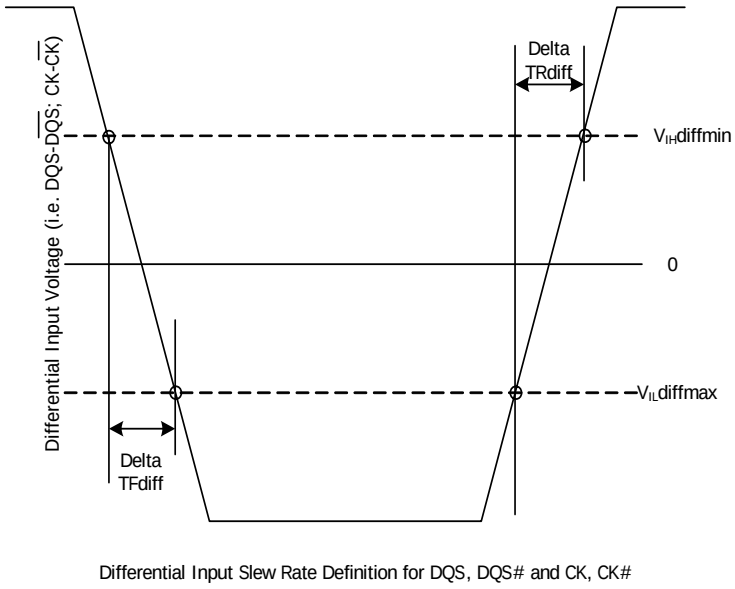


Figure 93. Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

5. AC & DC Output Measurement Levels

5.1 Single Ended AC and DC Output Levels

Table 35 shows the output levels used for measurements of single ended signals.

Table 35. Single-ended AC and DC Output Levels

Symbol	Parameter	800MHz/900MHz /1.0GHz	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ} /2.

5.2 Differential AC and DC Output Levels

Table 36 shows the output levels used for measurements of differential signals.

Table 36. Differential AC and DC Output Levels

Symbol	Parameter	800MHz/900MHz /1.0GHz	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

5.3 Single Ended Output Slew Rate

Whit the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 37 and Figure 94.

Table 37. Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

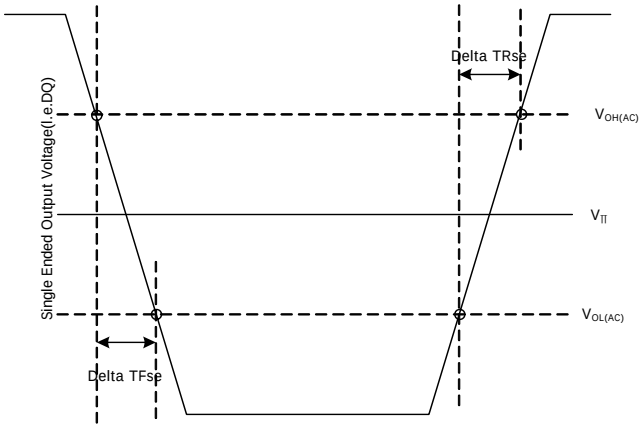


Figure 94. Single-ended Output slew Rate Definition

Table 38. Output Slew Rate (single-ended)

		800MHz		900MHz		1.0GHz		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	TBD	5	TBD	5(1)	TBD	5(1)	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Notes:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.
   Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
   Case 2 in defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies.

5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 39 and Figure 95.

Table 39. Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTFdiff

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

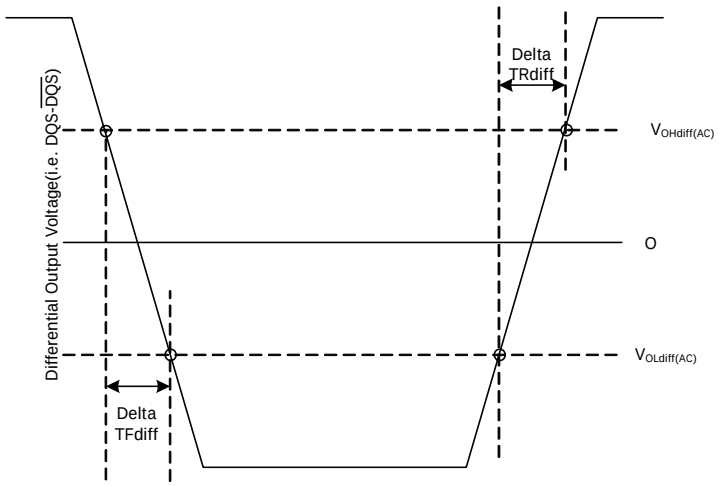


Figure 95. Differential Output slew Rate Definition

Table 40. Differential Output Slew Rate

		800MHz		900MHz		1.0GHz		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	12	5	12	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: DifferentialSignals

For Ron = RZQ/7 setting

5.5 Reference Load for AC Timing and Output Slew Rate

Figure 96 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

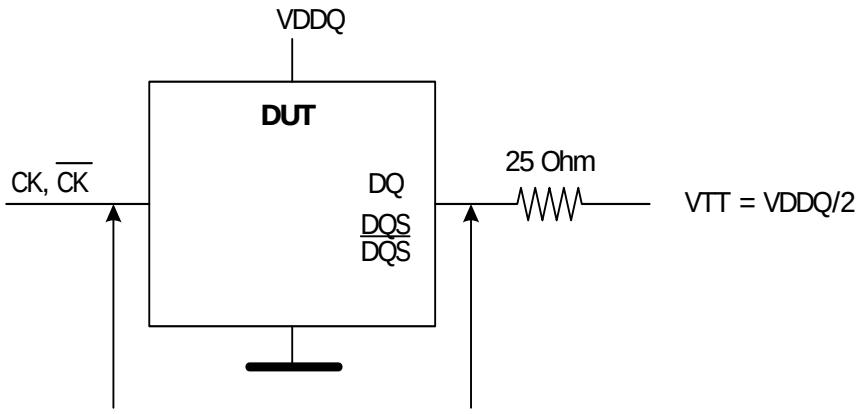


Figure 96. Reference Load for AC Timing and Output Slew Rate

5.6 Overshoot and Undershoot Specifications

5.6.1 Address and Control Overshoot and Undershoot Specifications

Table 41. AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	800MHz	900MHz	1.0GHz	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 97)	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure 97)	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure 97)	0.33	0.28	0.25	V-ns
Maximum undershoot area below VSS (See Figure 97)	0.33	0.28	0.25	V-ns
(A0-A15, BA0-BA3, CS, RAS, CAS, WE, CKE, ODT)				

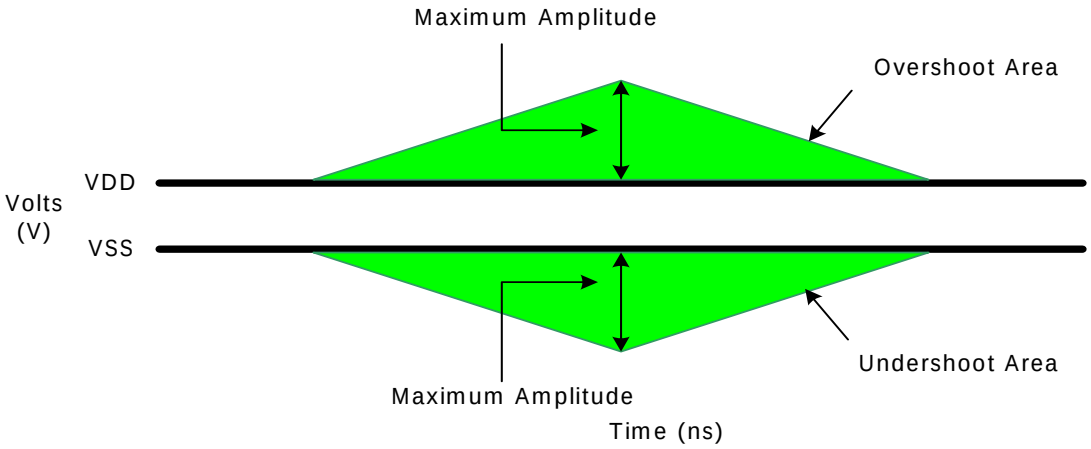


Figure 97. Address and Control Overshoot and Undershoot Definition

5.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Table 42. AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	800MHz	900MHz	1.0GHz	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 98)	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure 98)	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ (See Figure 98)	0.13	0.11	0.10	V-ns
Maximum undershoot area below VSSQ (See Figure 98)	0.13	0.11	0.10	V-ns

(CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM)

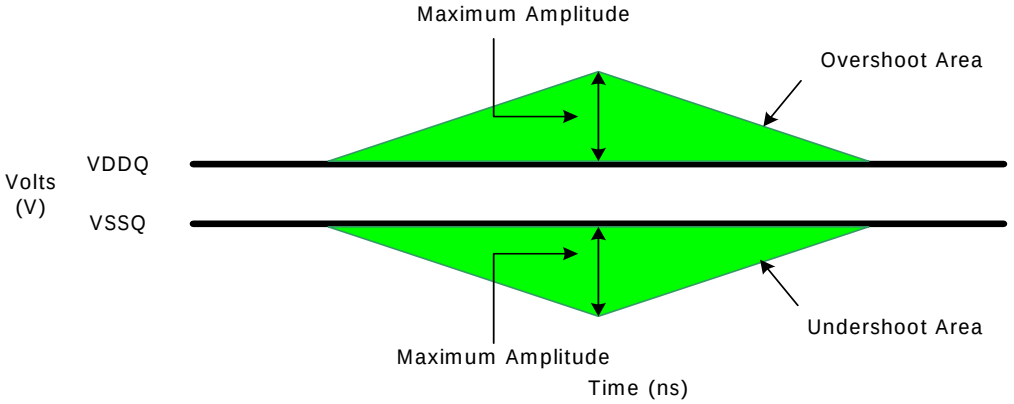


Figure 98. Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

5.7 Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure 99. Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

RON_{34} = R_{ZQ} / 7 (nominal 34.3 ohm +/- 10% with nominal R_{ZQ} = 240 ohm)

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ **under the condition that RON_{Pd} is turned off**

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ **under the condition that RON_{Pu} is turned off**

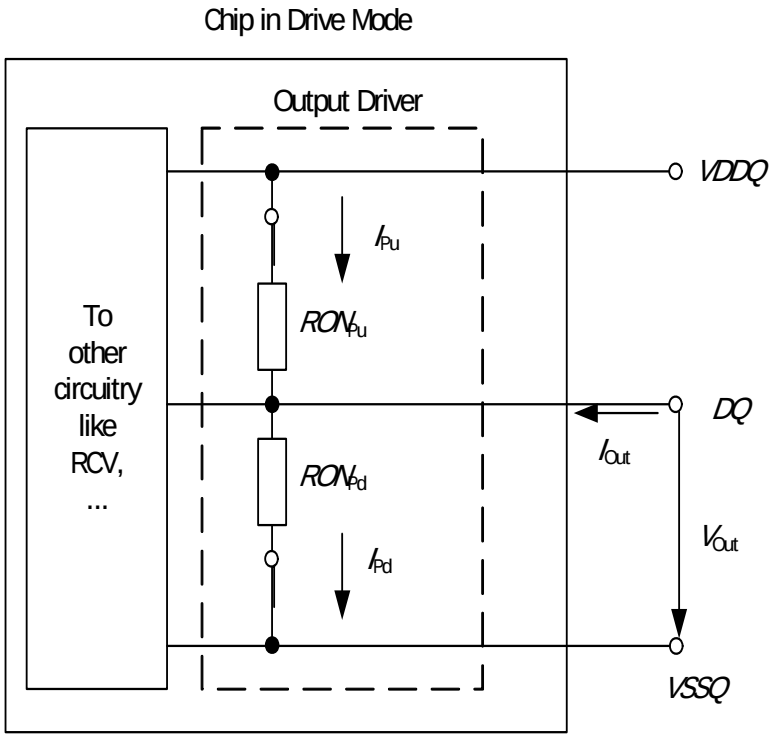


Figure 99. Output Driver: Definition of Voltages and Currents

Table 43. Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240Ω; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} = 0.2 x V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 x V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 x V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
	RON_{34Pu}	V_{OLdc} = 0.2 x V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 x V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 x V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
40 Ω	RON_{40Pd}	V_{OLdc} = 0.2 x V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 x V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 x V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1, 2, 3
	RON_{40Pu}	V_{OLdc} = 0.2 x V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 x V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 x V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5 x V_{DDQ}	-10		+10	%	1, 2, 4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
   Measure RON_{Pu} and RON_{Pd}, both at 0.5 * V_{DDQ}:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} X100$$

5.7.1 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 44 and Table 45.

$\Delta T = T - T(@calibration)$; $\Delta V = VDDQ - VDDQ(@calibration)$; VDD = VDDQ

Note: $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table 44. Output Driver Sensitivity Definition

	min	max	unit
RONPU@ V_{OHdc}	$0.6 - dR_{ON}dTH*\|\Delta T\| - dR_{ON}dVH*\|\Delta V\|$	$1.1 + dR_{ON}dTH*\|\Delta T\| + dR_{ON}dVH*\|\Delta V\|$	RZQ/7
RON@ V_{OMdc}	$0.9 - dR_{ON}dTM*\|\Delta T\| - dR_{ON}dVM*\|\Delta V\|$	$1.1 + dR_{ON}dTM*\|\Delta T\| + dR_{ON}dVM*\|\Delta V\|$	RZQ/7
RONPD@ V_{OLdc}	$0.6 - dR_{ON}dTL*\|\Delta T\| - dR_{ON}dVL*\|\Delta V\|$	$1.1 + dR_{ON}dTL*\|\Delta T\| + dR_{ON}dVL*\|\Delta V\|$	RZQ/7

Table 45. Output Driver Voltage and Temperature Sensitivity

Speed Bin	800MHz		900MHz/1.0GHz		Units
	min	max	min	max	
$dR_{ON}dTM$	0	1.5	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	0	0.13	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

5.8 On-Die Termination (ODT) Levels and I-V Characteristics

5.8.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS/$\overline{DQS}$ and TDQS/$\overline{TDQS}$ (x8 devices only) pins.
A functional representation of the on-die termination is shown in Figure 100. The individual pull-up and pull-down resistors (RTT_{Pu} and RTT_{Pd}) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ under the condition that RTT_{Pd} is turned off

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RTT_{Pu} is turned off

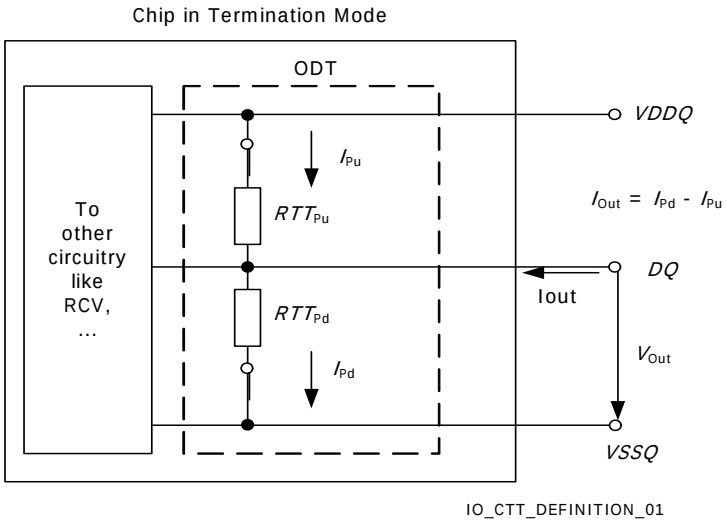


Figure 100. On-Die Termination: Definition of Voltages and Currents

5.8.2 ODT DC Electrical Characteristics

Table 46 provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60Pd120}$, $RTT_{60Pu120}$, $RTT_{120Pd240}$, $RTT_{120Pu240}$, RTT_{40Pd80}, RTT_{40Pu80}, RTT_{30Pd60}, RTT_{30Pu60}, RTT_{20Pd40}, RTT_{20Pu40} are not specification requirements, but can be used as design guide lines:

Table 46. ODT DC Electrical Characteristics, assuming R_{ZQ} = 240Ω+/-1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	RTT	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}	1,2,3,4
		$RTT_{120Pu240}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}	1,2,3,4
		RTT_{120}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/2	1,2,5
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/2	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/2	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/2	1,2,3,4
		$RTT_{60Pu120}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/2	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/2	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/2	1,2,3,4
		RTT_{60}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/4	1,2,5
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/3	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/3	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/3	1,2,3,4
		RTT_{40Pu80}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	R_{ZQ}/3	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	R_{ZQ}/3	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	R_{ZQ}/3	1,2,3,4
		RTT_{40}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	R_{ZQ}/6	1,2,5

Table 46. ODT DC Electrical Characteristics, assuming R_{ZQ} = 240Ω+/-1% entire operating temperature range; after proper ZQ calibration (Cont'd)

MR1 A9, A6, A2	RTT	Resistor	V_{Out}	min	nom	max	Unit	Notes
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	$R_{ZQ}/4$	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	$R_{ZQ}/4$	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	$R_{ZQ}/4$	1,2,3,4
		RTT_{30Pu60}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	$R_{ZQ}/4$	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	$R_{ZQ}/4$	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	$R_{ZQ}/4$	1,2,3,4
		RTT_{30}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/8$	1,2,5
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.1	$R_{ZQ}/6$	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	$R_{ZQ}/6$	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.4	$R_{ZQ}/6$	1,2,3,4
		RTT_{20Pu40}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.4	$R_{ZQ}/6$	1,2,3,4
			0.5 × V_{DDQ}	0.9	1.00	1.1	$R_{ZQ}/6$	1,2,3,4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.1	$R_{ZQ}/6$	1,2,3,4
		RTT_{20}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/12$	1,2,5
Deviation of V_M w.r.t. $V_{DDQ}/2$, DV_M				-5		+5	%	1,2,5,6

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for *RTT*:
   Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

Measurement definition for V_M and DV_M:

Measure voltage (V_M) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \bullet V_M}{V_{DDQ}} - 1\right) \bullet 100$$

5.8.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 47 and Table 48.

DT = T - T(@calibration); DV=VDDQ - VDDQ(@calibration); VDD = VDDQ

Table 47. ODT Sensitivity Definition

	min	max	unit
RTT	0.9 - $dR_{TT}dT^*\|\Delta T\|$ - $dR_{TT}dV^*\|\Delta V\|$	1.6 + $dR_{TT}dT^*\|\Delta T\|$ + $dR_{TT}dV^*\|\Delta V\|$	RZQ/2,4,6,8,12

Table 48. ODT Voltage and Temperature Sensitivity

	min	max	unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

5.9 ODT Timing Definitions

5.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 101.

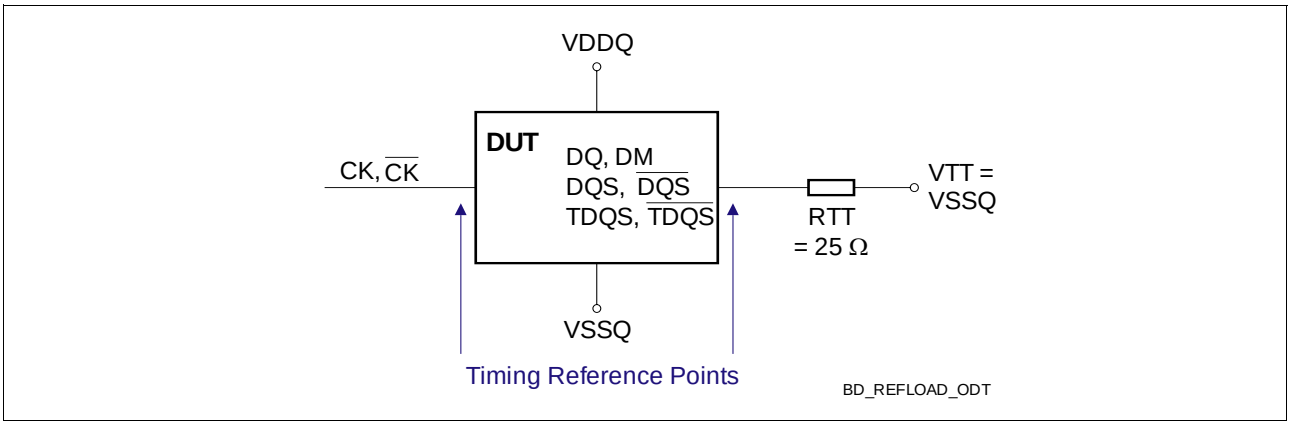


Figure 101. ODT Timing Reference Load

5.9.2 ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD} and t_{ADC} are provided in Table 49 and subsequent figures. Measurement reference settings are provided in Table 50.

Table 49. ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure 102
t_{AONPD}	Rising edge of CK - $\overline{CK}$ with ODT being first registered high	Extrapolated point at VSSQ	Figure 103
t_{AOF}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure 104
t_{AOFPD}	Rising edge of CK - $\overline{CK}$ with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure 105
t_{ADC}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure 106

Table 50. Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	

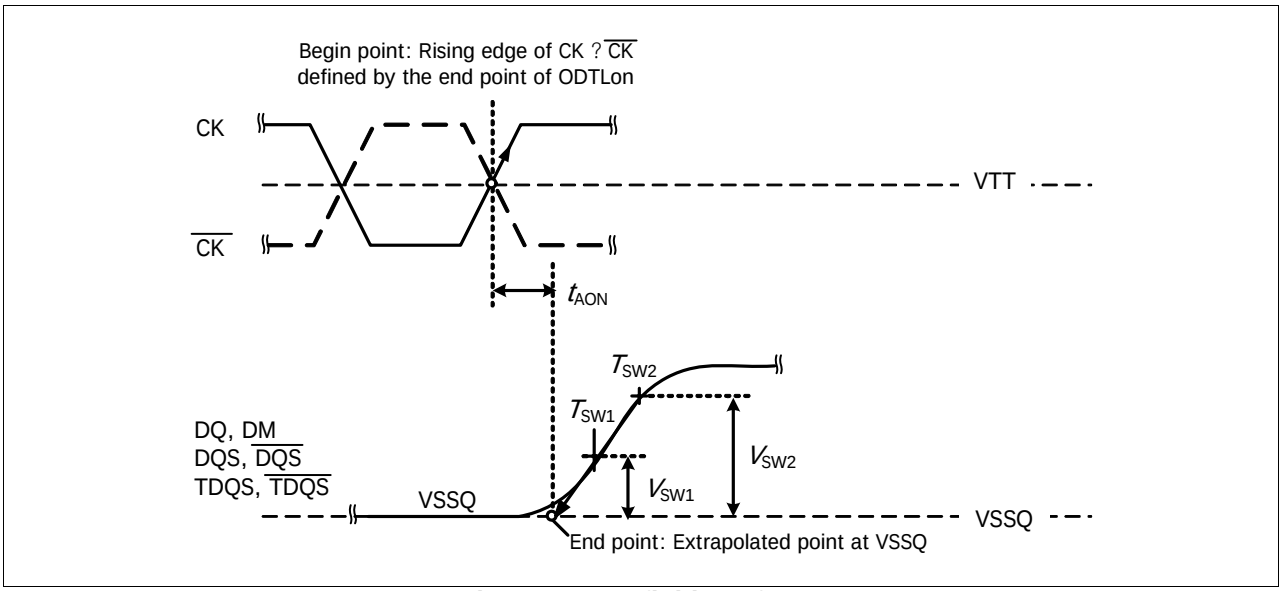


Figure 102. Definition of t_{AON}

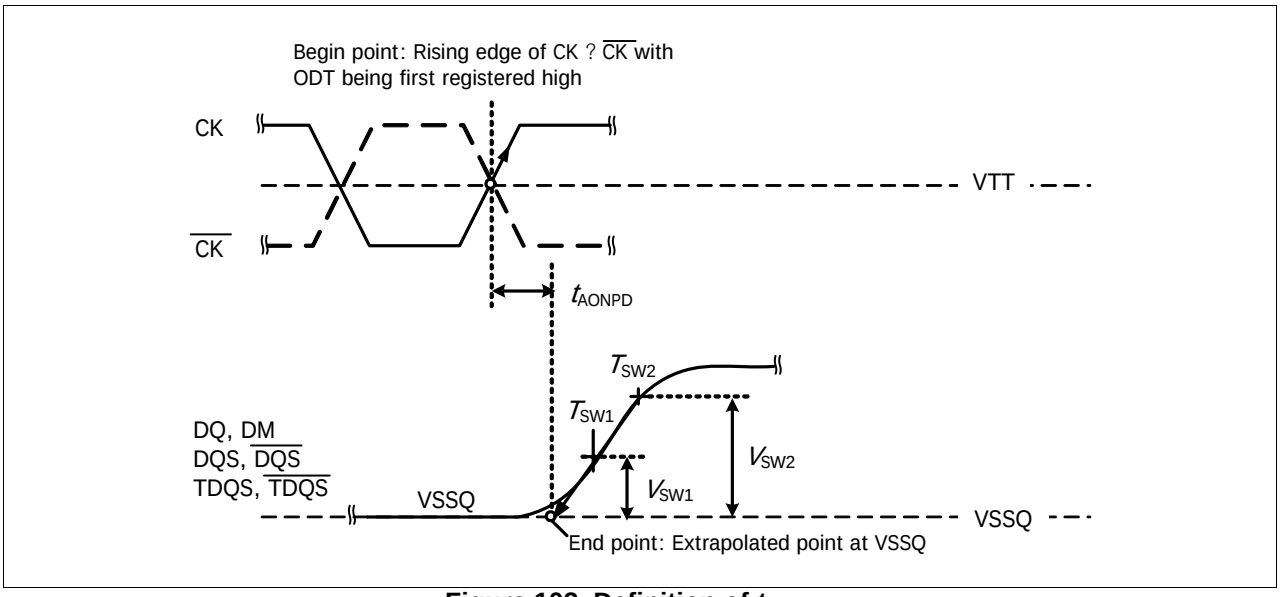


Figure 103. Definition of t_{AONPD}

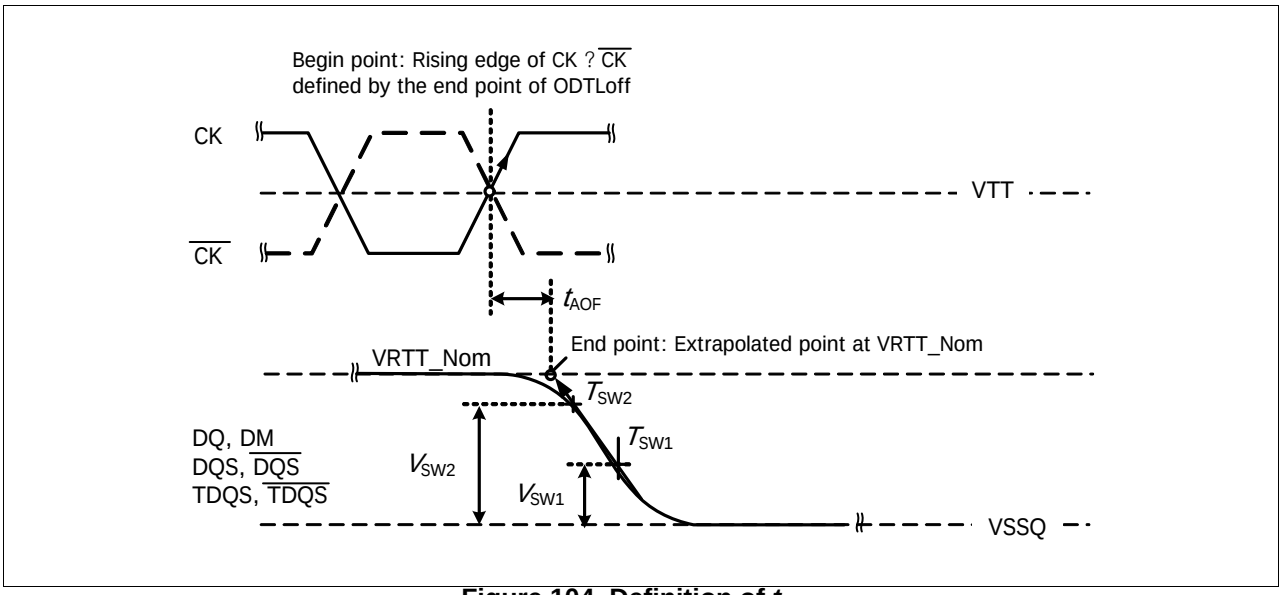


Figure 104. Definition of t_{AOF}

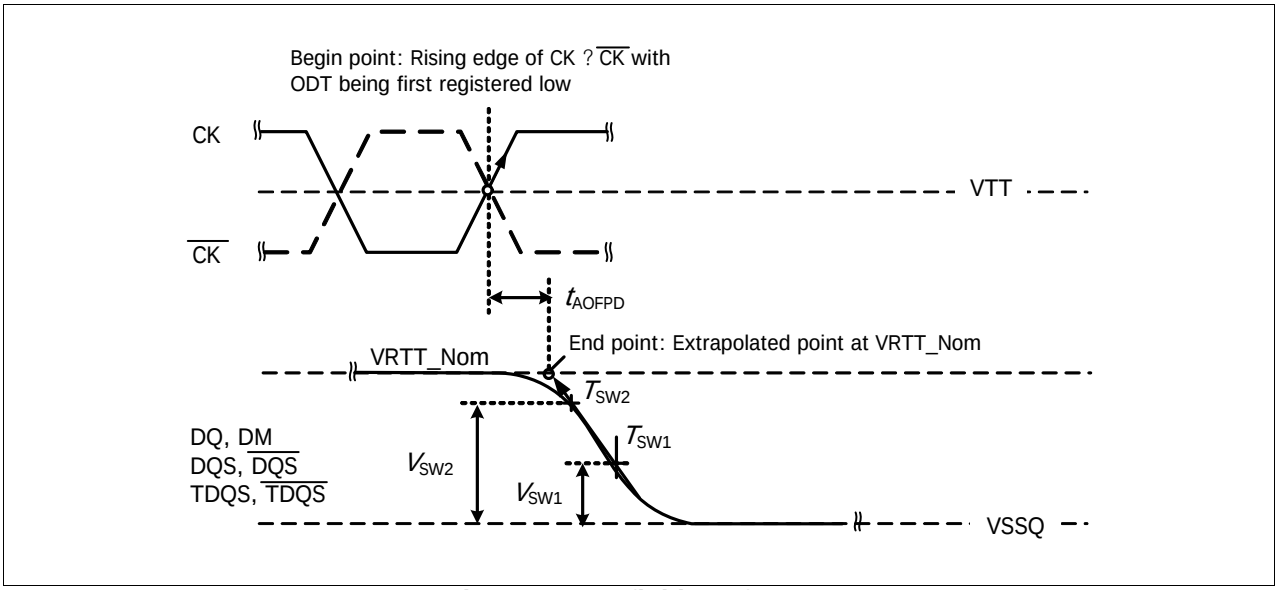


Figure 105. Definition of t_{AOFPD}

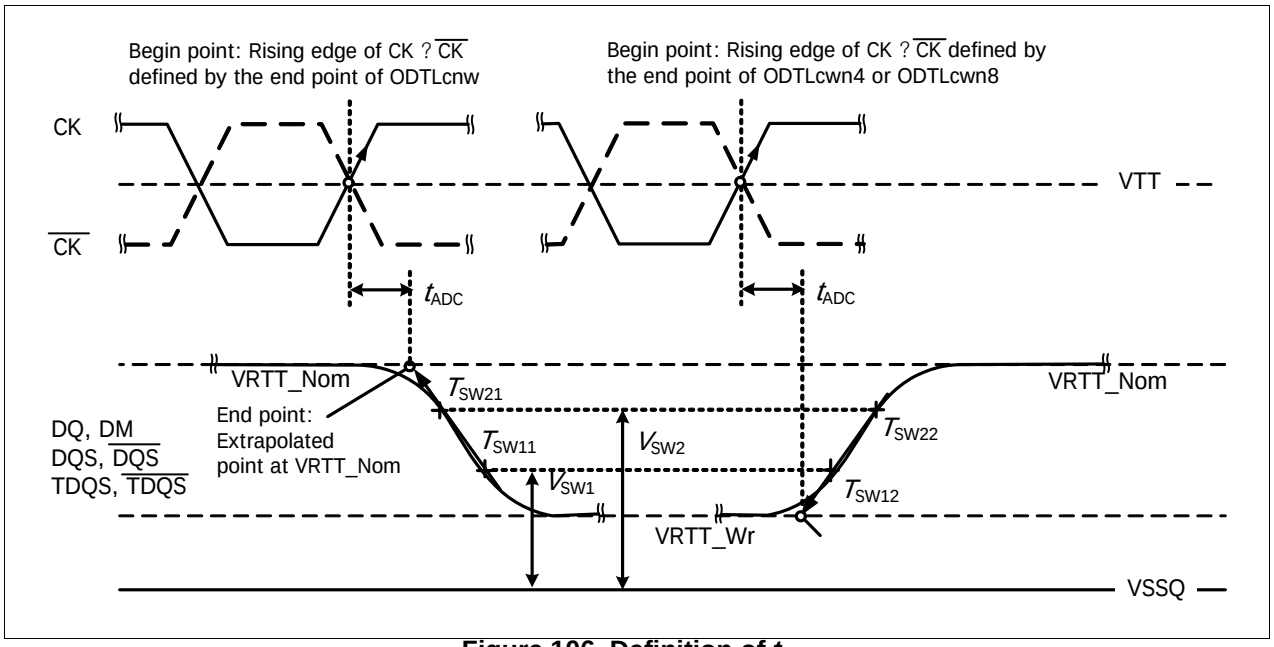


Figure 106. Definition of t_{ADC}

6. Electrical Characteristics & AC Timing for 800MHz to 1.0GHz

6.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

6.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[\sum_{j=1}^{N} tCK_j \right] / N$$

where $N = 200$

6.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

6.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j \right] / (N \times tCK(avg))$$

where $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j \right] / (N \times tCK(avg))$$

where $N = 200$

6.1.4 Definition for tJIT(per) and tJIT(per,lck)

tJIT(per) = Min/max of {tCK_i = tCK(avg) where i = 1 to 200}.

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not subject to production test.

6.1.5 Definition for tJIT(cc) and tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of $|\{tCK_{i+1} - tCK_i\}|$.

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT (cc,lck) are not subject to production test.

6.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

6.2 Refresh parameters by device density

Table 51. Refresh parameters by device density

Parameter	RTT_Nom Setting		1Gb	Units	Notes
REF command to ACT or REF command time	tRFC		110	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	us	
		85 °C < T_{CASE} ≤ 95 °C	3.9	us	1

Notes:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

7. Electrical Characteristics and AC Timing

7.1 Timing Parameters for 800MHz, 900MHz, and 1.0GHz Speed Bins

Table 52. Timing parameters by Speed Bin

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK (avg)	See “10. Standard Speed Bins” on page 62.						ps	f
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Absolute Clock Period	tCK (abs)	tCK(avg)min+tJIT(per)min						ps	
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT (per)	-70	70	-60	60	-40	40	ps	
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-60	60	-50	50	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	140	140	130	130	TBD	TBD	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	120	120	110	110	TBD	TBD	ps	
Duty Cycle jitter	tJIT (duty)	-	-	-	-	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR (2per)	-103	103	-93	93	TBD	TBD	ps	
Cumulative error across 3 cycles	tERR (3per)	-122	122	-112	112	TBD	TBD	ps	
Cumulative error across 4 cycles	tERR (4per)	-136	136	-122	122	TBD	TBD	ps	
Cumulative error across 5 cycles	tERR (5per)	-147	147	-135	135	TBD	TBD	ps	
Cumulative error across 6 cycles	tERR (6per)	-155	155	-140	140	TBD	TBD	ps	
Cumulative error across 7 cycles	tERR (7per)	-163	163	-146	146	TBD	TBD	ps	
Cumulative error across 8 cycles	tERR (8per)	-169	169	-149	149	TBD	TBD	ps	
Cumulative error across 9 cycles	tERR (9per)	-175	175	-160	160	TBD	TBD	ps	

Table 52. Timing parameters by Speed Bin (Continued)

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Cumulative error across 10 cycles	tERR (10per)	-180	180	-165	165	TBD	TBD	ps	
Cumulative error across 11 cycles	tERR (11per)	-184	184	-168	168	TBD	TBD	ps	
Cumulative error across 12 cycles	tERR (12per)	-188	188	-170	170	TBD	TBD	ps	
Cumulative error across n = 13, 14,.....49, 50 cycles	tERR (nper)	tERR(nper)min=(1+0.68ln(n))*JIT(per)min tERR(nper)max=(1+0.68ln(n))*JIT(per)max						ps	24
Data Timing									
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	100	-	87	-	75	-	ps	13
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQ low-impedance time from CK, $\overline{CK}$	tLZ (DQ)	-450	225	-400	200	-360	180	ps	13, 14, a
DQ high impedance time from CK, $\overline{CK}$	tHZ (DQ)	-	225	-	200	-	180	ps	13, 14, a
Data setup time to DQS, $\overline{DQS}$ referenced to Vih (ac) / Vil (ac) levels	tDS (base)	10	-	0	-	-10	-	ps	d, 17
Data hold time from DQS, $\overline{DQS}$ referenced to Vih (dc) / Vil (dc) levels	tDH (base)	45	-	45	-	40	-	ps	d, 17
Data Strobe Timing									
DQS,$\overline{DQS}$ differential READ Preamble	tRPRE	0.9	Note	0.9	Note	0.9	TBD	tCK (avg)	13, 19 b
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	Note	0.3	Note	0.3	TBD	tCK (avg)	11, 13, b
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK (avg)	
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK (avg)	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK	-225	225	-180	180	-180	180	ps	13, a
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	-400	200	-360	180	ps	13, 14, a
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	-	200	-	180	ps	13, 14 a

Table 52. Timing parameters by Speed Bin (Continued)

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.3	0.3	tCK (avg)	c
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK (avg)	c
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK (avg)	c
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e, 18
WRITE recovery time	tWR	16.3	-	15.6	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max(12nCK,15ns)	-	max(12nCK,15ns)	-	max(12nCK,15ns	-		
ACT to internal read or write delay time	tRCD	15	-	15.4	-	16	-		e
PRE command period	tRP	15	-	15.4	-	16	-		e
ACT to ACT or REF command period	tRC	50	-	50.6	-	52	-		e
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL (min)	24	-	28	-	31	-	nCK	
End of MPR Read burst to MSR for MPR (exit)	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	37.5	-	37.4	-	37	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	7	-	7	-	7	-		e

Table 52. Timing parameters by Speed Bin (Continued)

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Four activate window for 2KB page size	tFAW	42.5	-	41.8	-	40	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih (ac) / Vil (ac) levels	tIS (base)	45	-	35		25	-	ps	b, 16
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih (dc) / Vil (dc) levels	tIH (base)	120	-	110	-	100	-	ps	b, 16
Calibration Timing					-				
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-		
Self Refresh Timings									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min)+1nCK		tCKE(min)+1nCK		tCKE(min)+1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-		
Power Down Timings									

Table 52. Timing parameters by Speed Bin (Continued)

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	7	-	7	-	7	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	MAX(10nCK,24ns)	-	MAX(10nCK,24ns)	-	MAX(10nCK,24ns)	-		2
CKE minimum pulse width	tCKE	4	-	5	-	5	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	nCK	,
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timings									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	

Table 52. Timing parameters by Speed Bin (Continued)

Note: The following general notes from page 156 apply to Table 52: Note a. VDD=VDDQ=1.5V+/-0.075V

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	1	9	ns	
RTT turn-on	tAON	-225	225	-200	200	-175	175	ps	7, a
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	8, a
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	a
Write Leveling Timings									
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	3
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLS	170	-	130	-	120	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	tWLH	170	-	130	-	120	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

7.2 Jitter Notes

a. Until 'tCK (avg)' represents the actual tCK (avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD = 4[nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK (avg) + tERR(4per), min.

b. These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT (per), tJIT (cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

c. These parameters are measured from a data strobe signal (DQS(L/U), $\overline{DQS(L/U)}$) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT (per), tJIT (cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

d. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{DQS}$(L/U)) crossing.

e. For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU {tPARAM [ns] / tCK (avg) [ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.For example, the device will support tnRP = RU {tRP / tCK (avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU {tRP / tCK (avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

f. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR (mper), act of the input clock, where 2 <= m <=12.(output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR-800 SDRAM has tERR (mper), act, min = -172 ps and tERR (mper), act, max =+ 193 ps, then t DQSCK, min (derated) = tDQSCK, min - tERR (mper), act, max = -400 ps - 193 ps = - 593 ps and tDQSCK, max (derated) = tDQSCK, max - tERR (mper), act, min = 400 ps+ 172 ps = + 572 ps. Similarly, tLZ (DQ) for DDR3-800 derates to tLZ (DQ), min (derated) = - 800 ps - 193 ps = - 993 ps and tLZ (DQ), max (derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR (mper), act, min is the minimum measured value of tERR (nper) where 2 <= n <=12, and tERR (mper), act, max is the maximum measured value of tERR (nper) where 2 <= n <= 12

g. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT (per), act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK (avg), act = 2500 ps, tJIT (per), act, min = - 72 ps and tJIT (per), act, max = + 93 ps, then tRPRE, min (derated) = tRPRE, min + tJIT (per), act, min = 0.9 x tCK (avg), act + tJIT (per), act + tJIT (per), act, min = 0.9 x 2500 ps - 72 ps =+ 2178 ps. Similarly, tQH, min (derated) = tQH, min + tJIT (per), act, min = 0.38 x tCK (avg), act + tJIT (per), act, min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

7.3 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions See ?$paratext>? on page 87 and See ?$paratext>? on page 87.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON See ?$paratext>? on page 109.
8. For definition of RTT turn-off time tAOF See ?$paratext>? on page 109.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tHZDQS(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See ?$paratext>? on page 76.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
15. tREFI depends on TOPER
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except $\overline{RESET}$, VRef(DC) = VRefCA(DC). See ?$paratext>? on page 159.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except $\overline{RESET}$, VRef(DC) = VRefCA(DC). See ?$paratext>? on page 166.
18. Start of internal write transaction is defined as follows:
    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.See ?$paratext>? on page 76.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See ?$paratext>? on page 104.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
29. tDQSL describes the instantaneous differential input low pulse width on DQS - $\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS - $\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH,act + tDQSL,act = 1 tCK,act; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
32. tDSH,act + tDSS,act = 1 tCK,act; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

7.4 Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 53) to the ΔtIS and ΔtIH derating value (see Table 54) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 107). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 109).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region'. use nominal slew rate for derating value (see Figure 108). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 110).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 58).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rate in between the values listed in Table 59, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 53. ADD/CMD Setup and Hold Base-Values for 1V/ns

Symbol	Reference	800MHz	900MHz	1.0GHz	Units
tIS(base) AC175	$V_{IH/L(ac)}$	45	35	TBD	ps
tIS(base) AC150	$V_{IH/L(ac)}$	170	160	TBD	ps
tIH(base) DC100	$V_{IH/L(dc)}$	120	110	TBD	ps

Notes:

1. (ac/dc referenced for 1V/ns Address/Command slew rate and 2 V/ns differential Ck-$\overline{CK}$ slew rate)
2. The tIS(base) AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 125 ps for 800MHz of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns.

Table 54. Derating values 800MHz tIS/tIH - ac/dc based AC175 Threshold

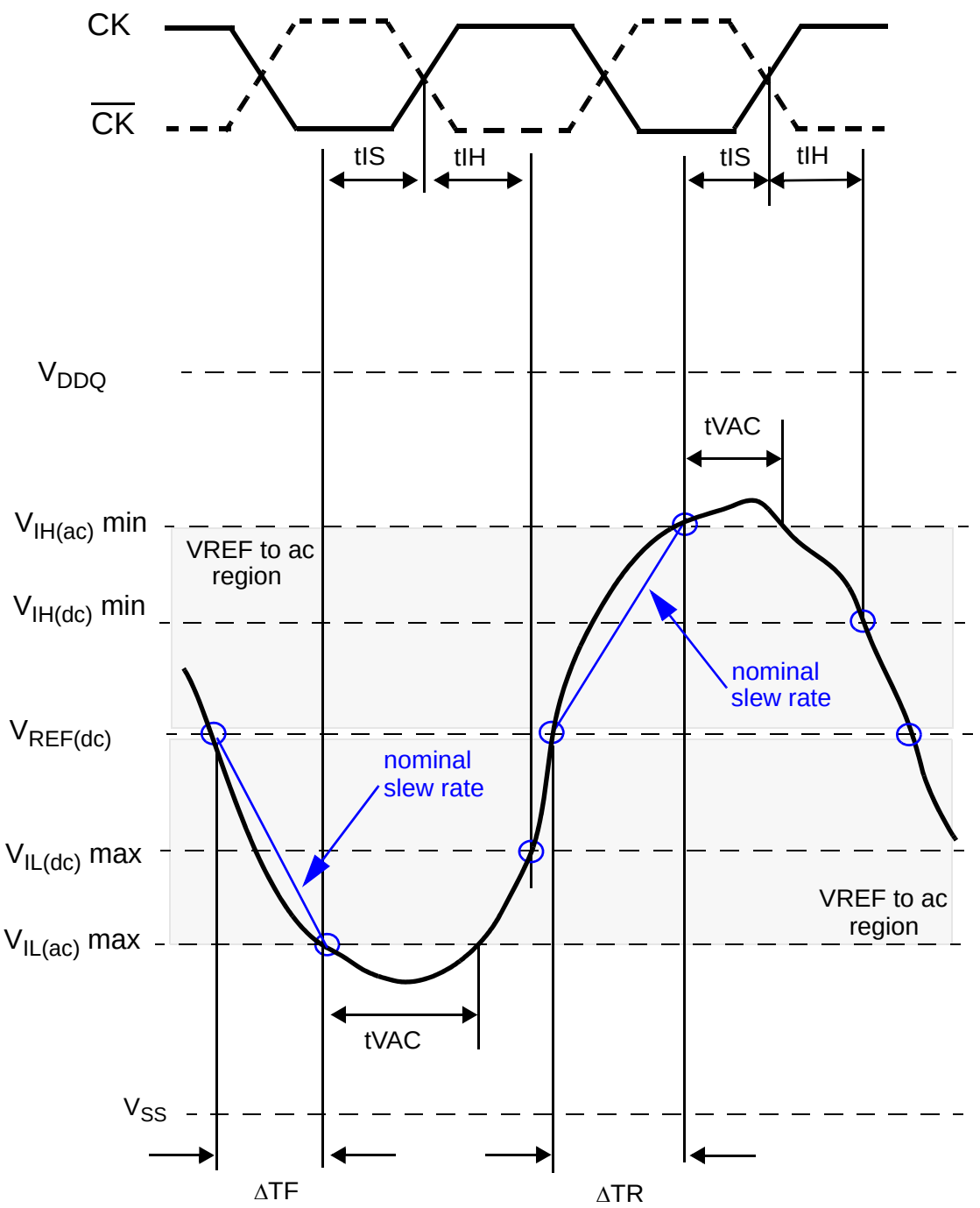
ΔtIS, ΔtIH derating in [ps] AC/DC based AC175 Threshold -> VIH(ac) = VREF(dc)+175mV, VIL(ac) = VREF(dc)-175mV																	
		CK,$\overline{CK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 55. Derating values 800MHz tISt/IH - ac/dc based - Alternate AC150 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC150 Threshold -> VIH(ac) = VREF(dc)+150mV, VIL(ac) = VREF(dc)-150mV																	
		CK,$\overline{CK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 56. Required time t_{AVC} above VIH(ac) {below VIL(ac)} for valid ADD/CMD transition

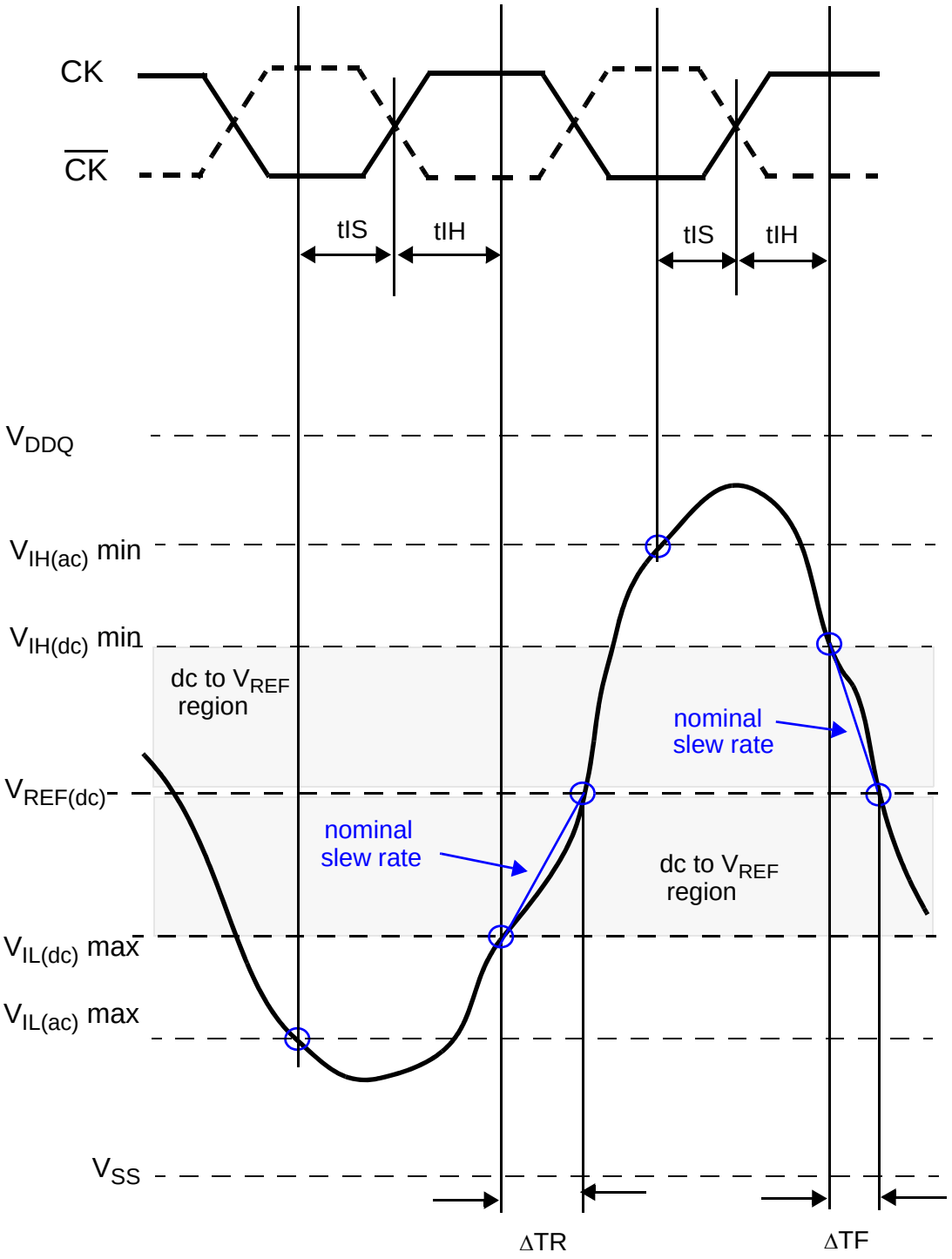
Slew Rate [V/ns]	t_{VAC} @ 175 mV [ps]		t_{VAC} @ 150 mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 107. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 108. Illustration of nominal slew rate for hole time t_{IH} (for ADD/CMD with respect to clock).

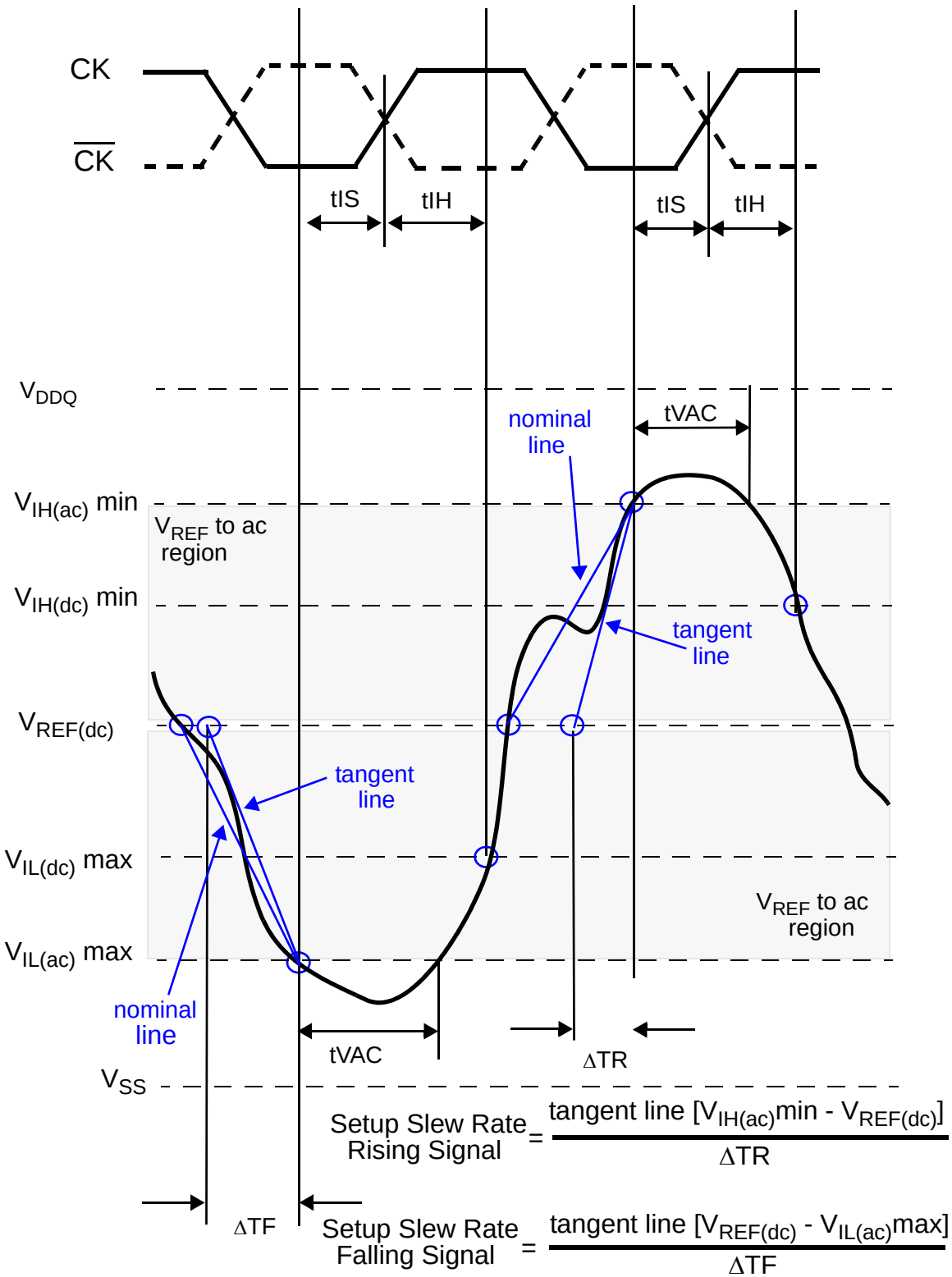
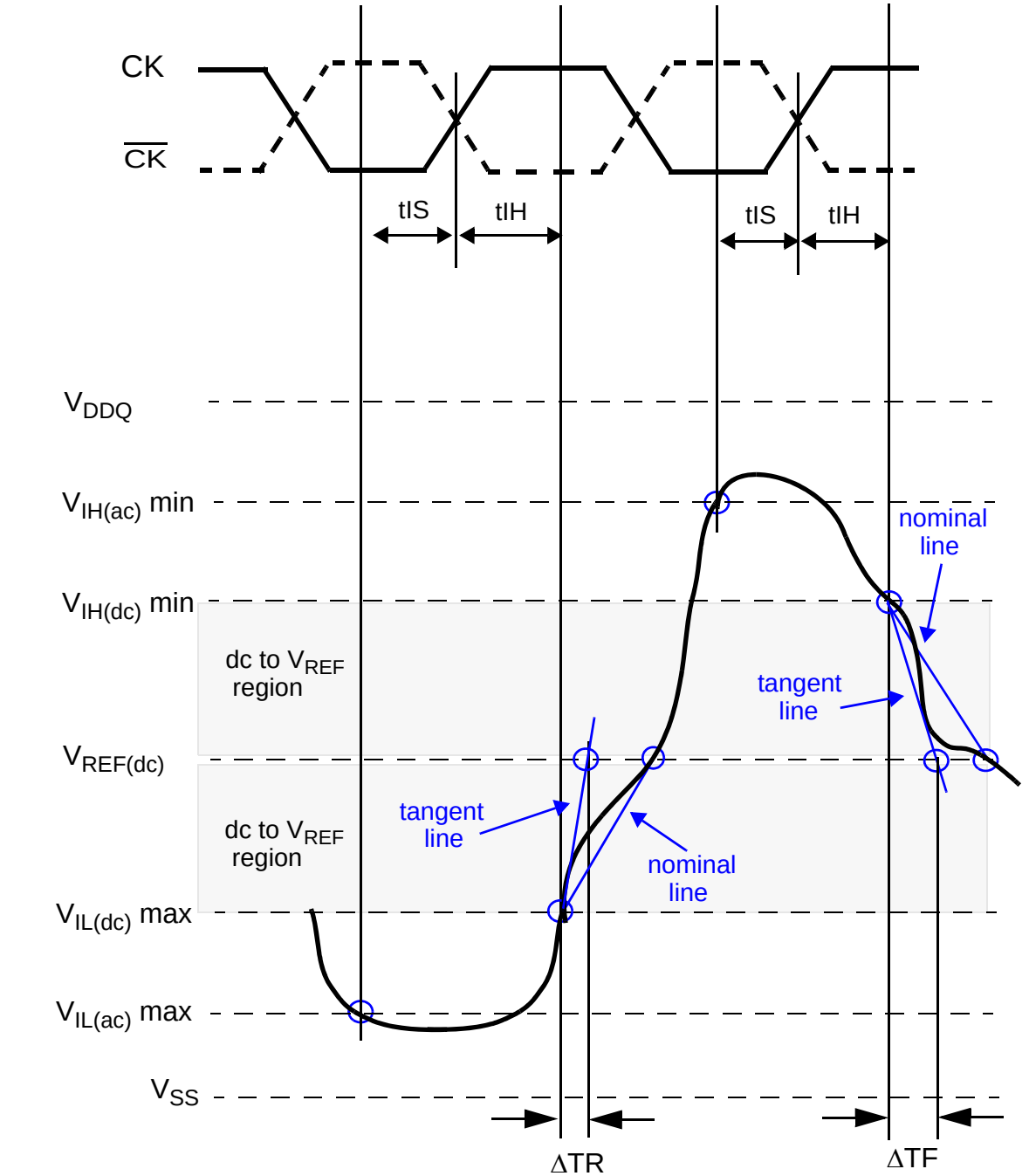


Figure 109. Illustration of tangent line for setup time t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)}\text{min} - V_{REF(dc)}]}{\Delta TF}$$

Figure 110. Illustration of tangent line for setup time t_{IH} (for ADD/CMD with respect to clock).

7.5 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 57) to the ΔtDS and ΔtDH (see Table 58) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 111). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 113).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 112). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 114).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 60).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 57. Data Setup and Hold Base-Values

Symbol	Reference	800MHz	900MHz	1.0GHz	Units
tDS(base) AC175	$V_{IH/L(ac)}$	-	-	-	ps
tDS(base) AC150	$V_{IH/L(ac)}$	10	-	-	ps
tDH(base) DC100	$V_{IH/L(dc)}$	45	45	TBD	ps

Notes:

1. (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

Table 58. Derating values (AC175)

ΔtDS, ΔtDH derating in [ps] AC/DC based[1]																	
		DQS,$\overline{\text{DQS}}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

Notes:

1. Cell contents shaded in red are defined as ‘not supported’.

Table 59. Derating values for (AC150) Derating

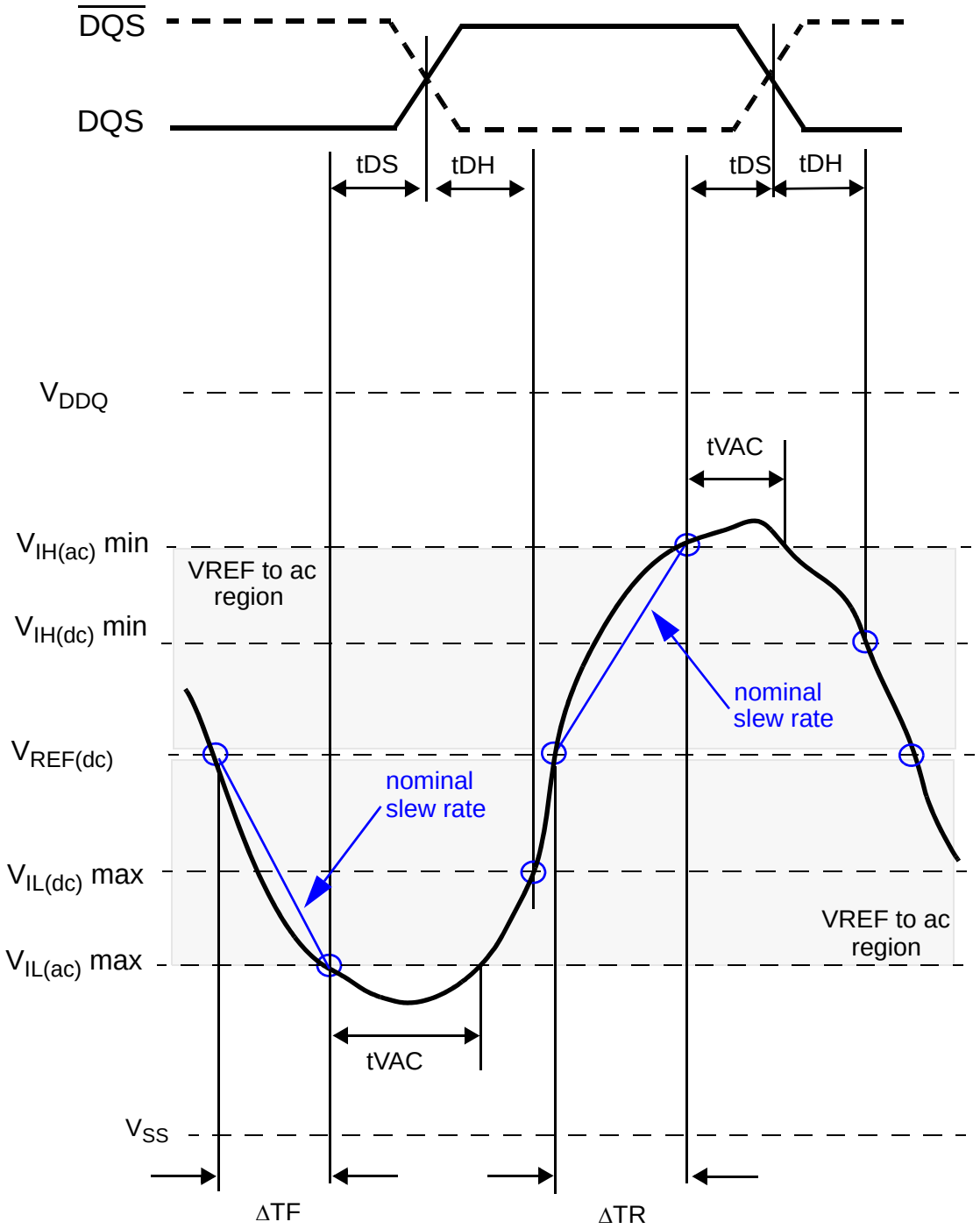
ΔtDS, ΔtDH derating in [ps] AC/DC based[1]																	
		DQS,$\overline{\text{DQS}}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

Notes:

1. Cell contents shaded in red are defined as ‘not supported’.

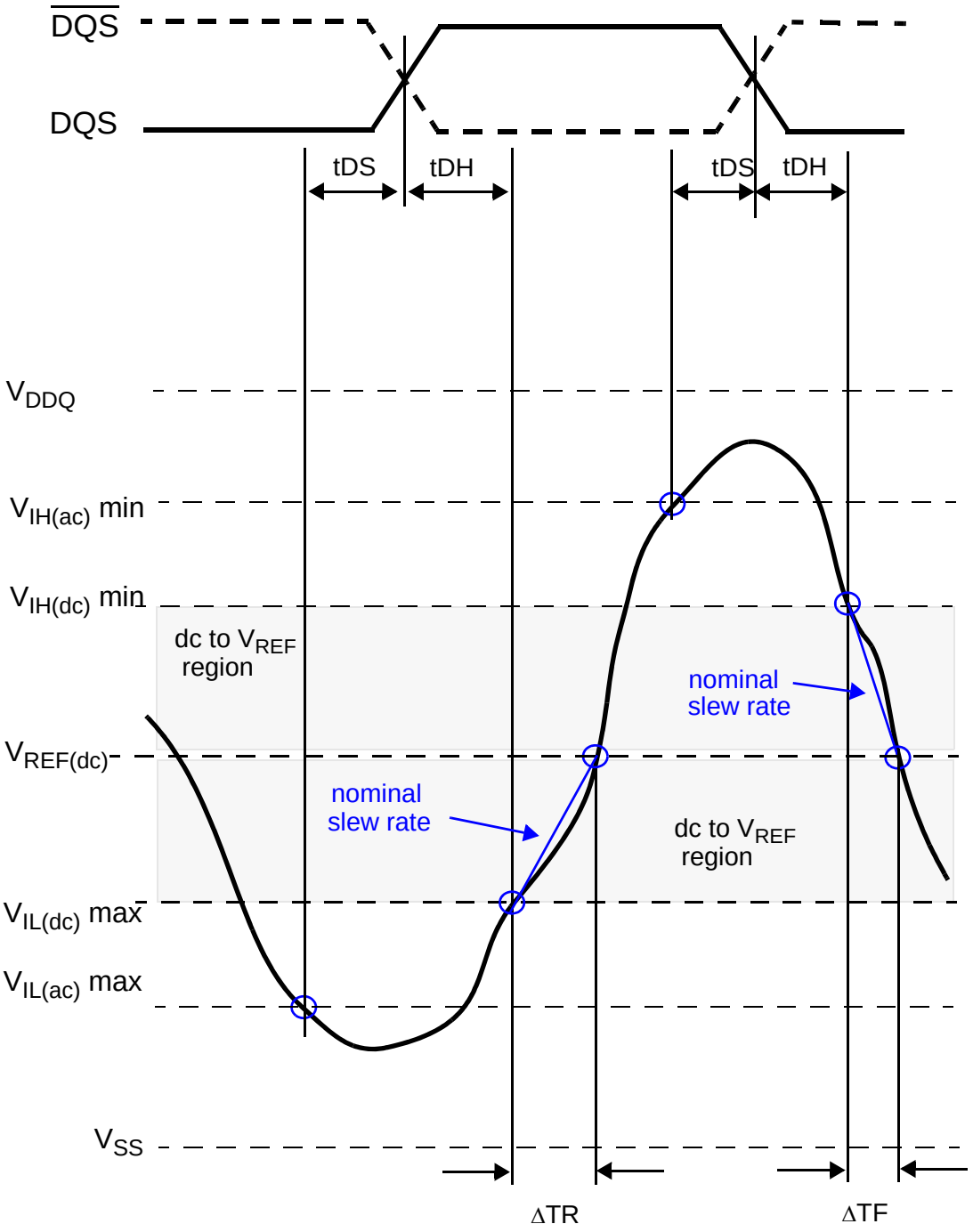
Table 60. Required time t_{AVC} above VIH(ac) {below VIL(ac)} for valid DQ transition

Slew Rate [V/ns]	800MHz (AC175)		800MHz (AC150)		900MHz/1.0GHz	
	t_{VAC} [ps]		t_{VAC} [ps]		t_{VAC} [ps]	
	min	max	min	max	min	max
> 2.0	75	-	175	-	TBD	-
2.0	57	-	170	-	TBD	-
1.5	50	-	167	-	TBD	-
1.0	38	-	163	-	TBD	-
0.9	34	-	162	-	TBD	-
0.8	29	-	161	-	TBD	-
0.7	22	-	159	-	TBD	-
0.6	13	-	155	-	TBD	-
0.5	0	-	155	-	TBD	-
< 0.5	0	-	150	-	TBD	-



$$\text{Setup Slew Rate}_{\text{Falling Signal}} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 111. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 112. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe)

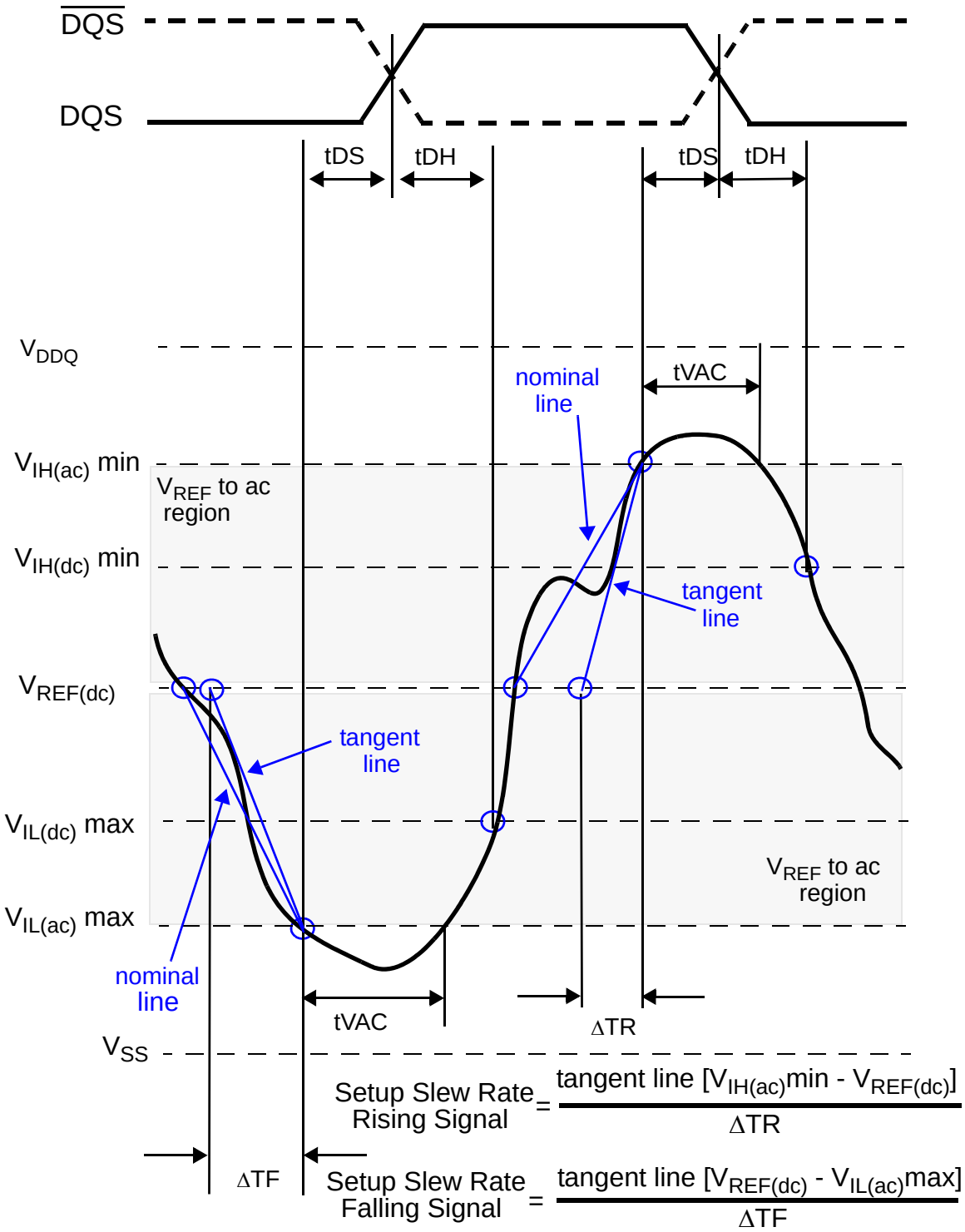
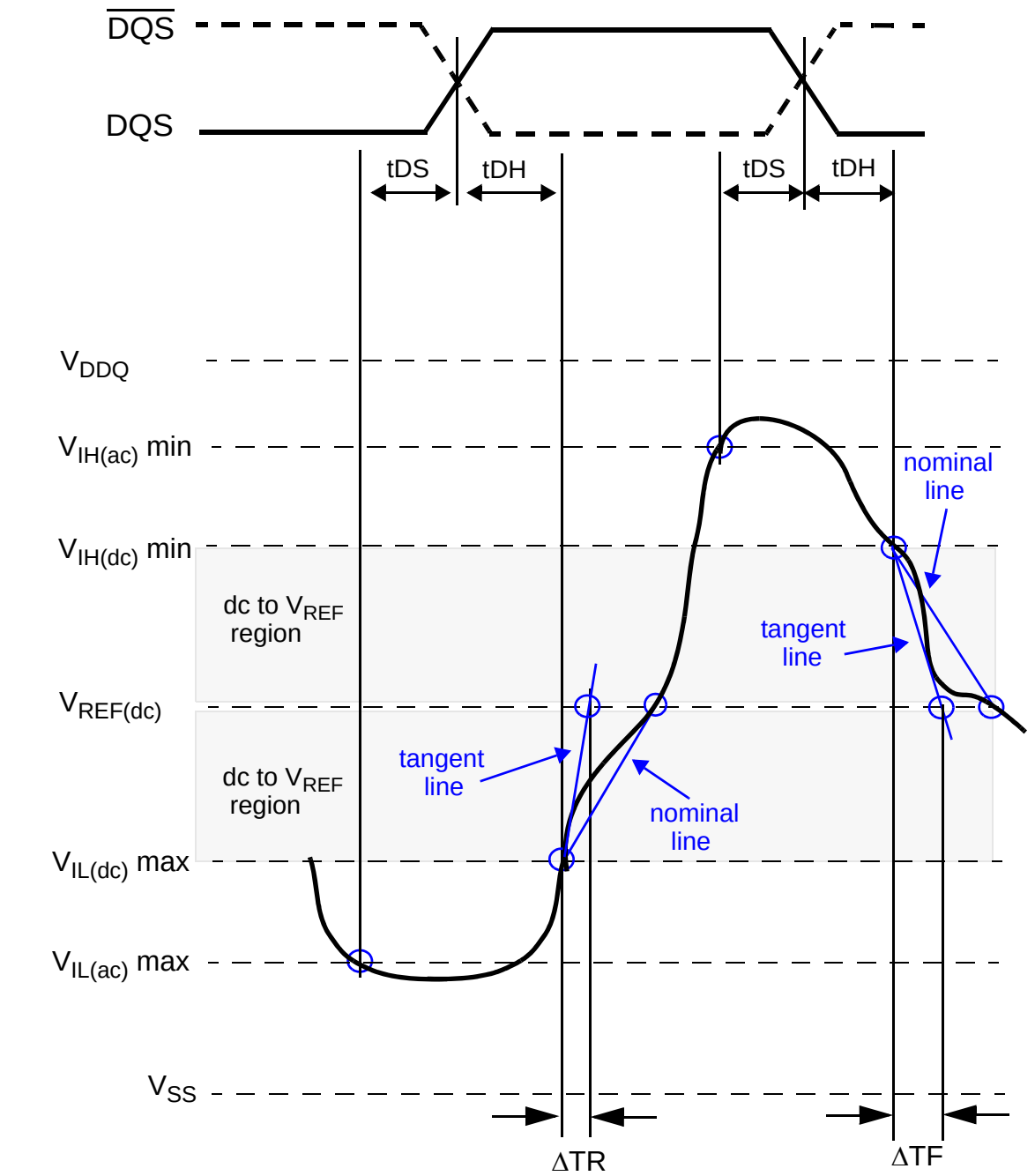


Figure 113. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)}\text{min} - V_{REF(dc)}]}{\Delta TF}$$

Figure 114. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe)