Rockwell

RFX144V12-S and RFX96V12-S MONOFAX® Modems with DigiTalk™ Voice Coder/Decoder and DigiTalk™ Full-Duplex Speakerphone

INTRODUCTION

The Rockwell RFX144V12-S and RFX96V12-S are MONOFAX® facsimile modems featuring Rockwell's DigiTalk™ speech processing technology for voice compression and full-duplex speakerphone capability. The DigiTalk™ voice coder/decoder compresses voice at 5.7 kbps with near toll quality playback, allowing up to 12 minutes of speech to be stored in 4 Mbits of memory. The DigiTalk™ speakerphone provides full-duplex hands-free voice conversation with both acoustic and line echo cancellation.

These functions are supplied in a two-device set: a modem data pump (MDP) packaged in a 100-pin PQFP and a secondary integrated analog codec (SIA) device packaged in a 28-pin PLCC. The MDP contains the primary integrated analog codec (PIA) and is pin-compatible with the RFXxxxV12 MONOFAX modem. This device set enables the OEM to cost-effectively add a digital answering machine and a full-duplex speakerphone to their fax machine design.

The modem can operate at 14400 (RFX144V12-S), 12000 (RFX144V12-S), 9600, 7200, 4800, 2400, or 300 bps, and can perform HDLC framing according to T.30 at the same rates. A programmable DTMF receiver and three programmable tone detectors are provided.

The 5.7 kbps DigiTalk™ voice coder/decoder allows the host controller to efficiently store and playback digital incoming messages (ICMs) and outgoing messages (OGMs). This low-bit-rate voice coder/decoder, employing Rockwell's proprietary speech compression algorithm provides 12 minutes per 4 Mbit of RAM. Selectable error correction coding allows storage in audio grade RAMs (ARAMs). DTMF and tone detection are available during voice coder/decoder operation to support user selectable features. The modem can be programmed to record messages from either the PIA or SIA. Echo cancellation techniques are employed during playback to allow DTMF and tone detection.

The speakerphone algorithm constantly adjusts its parameters to deliver the best performance during real-time conditions, allowing automatic fallback from full-duplex to pseudo-duplex. Therefore, the host controller can easily set up the speakerphone and change the operation such as mute, automatic gain control (AGC) enable/disable, microphone level, speaker volume, tone transmit, and handset functions.

FEATURES

- Group 3 facsimile transmission/reception
  - CCITT V.17 and V.33 (RFX144V12-S)
  - CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4
  - HDLC framing at all speeds
  - Receive dynamic range: 0 dBm to –43 dBm
  - Equalization
    - Automatic adaptive
    - Fixed and programmable digital compromise
- V.27 ter short train
- Caller ID reception
- 5.7 kbps DigiTalk™ voice coder/decoder
  - 12 minutes of voice storage per 4 Mbit memory
  - Near toll quality voice recording and playback of ICMs and OGMs
  - Error correction coding allows ARAM use at 5.9 kbps
  - DTMF and tone detection
  - Pitch synchronized fast and slow playback
  - Near-end echo cancellation
  - Room monitor
- DigiTalk™ full-duplex speakerphone
  - Acoustic echo cancellation
    - 30 dB speech echo return loss enhancement
    - 65 ms echo length
    - Zero processing delay
  - Line echo cancellation
    - 40 dB speech echo return loss enhancement
    - 21 ms echo length
    - Zero processing delay
  - Programmable microphone AGC
  - Programmable speaker AGC
  - Microphone volume selection and muting
  - Speaker volume control and muting
    - 30 dB speaker volume control range in 2 dB steps
  - Two DTMF generators and one tone detector
  - Auto fallback toward pseudo-duplex operation under poor operating conditions
  - Programmable handset echo simulation in handset operation
- Concurrent DTMF, FSK, and tone reception
  Programmable transmit level
- Programmable dual tone generation
- Programmable tone detection

(Continued)

Data Sheet
(Preliminary)

Order No. MD115
Rev. 1, November 8, 1994

FEATURES (CONT'D)

- Programmable interface memory interrupt
- Programmable ring detector
- 8-bit or 16-bit high quality audio mode transmission/ reception
- Eight general purpose input (GPI) and eight general purpose output (GPO) pins for host assignment
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA/TIA-232-E compatible) interface
- TTL and CMOS compatible
- +5V operation
- Power consumption (see Table 10):
  - Normal: 620 mW (typical)
  - Sleep: 10.8 mW (typical)
- Packaging
  - MDP: 100-pin PQFP (plastic quad flat pack)
  - SIA: 28-pin PLCC (plastic leaded chip carrier)
- Software compatible with other MONOFAX modems

TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3400 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.17 (RFX144V12-S), V.33 (RFX144V12-S), V.29, V.27 ter, V.21 Channel 2, and V.23 receive.

Automatic Adaptive Equalizer

An adaptive equalizer in V.17 (RFX144V12-S), V.33 (RFX144V12-S), V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Fixed Digital Cable Compromise Equalizer

Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive and transmit data paths.

Table 1. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits /Symbol	Constellation Points
V.17/V.33 14400[2]	TCM	1700 or 1800	14400	2400	6	128
V.17/V.33 12000[2]	TCM	1700 or 1800	12000	2400	5	64
V.17 9600[2]	TCM	1700 or 1800	9600	2400	4	32
V.17 7200[2]	TCM	1700 or 1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650, 1850	300	300	1	–
V.23 receive HDX	FSK	1300, 2100	1200	1200	1	–
V.23 receive HDX	FSK	1300, 2100	1200	1200	1	–

Notes:

1. Modulation legend: QAM: Quadrature Amplitude Modulation
   DPSK: Differential Phase Shift Keying
   FSK: Frequency Shift Keying
   TCM: Trellis-Coded Modulation
2. RFX144V12-S only.

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response filter (FIR) with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 2.

Turn-off Sequence

Transmitter turn-off sequence times are shown in Table 3.

Transmit Level

The transmitter output (TXA) level is programmable in the DSP RAM from 0 dBm to –15.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Table 2. Turn-On Sequence Times

Configuration	~RTS On to ~CTS On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.17/V.33	1395 ms	1602 ms
V.17 Short Train	144 ms	351 ms
V.29 Long Train	255 ms	443 ms
V.27 ter 4800 bps Long Train	710 ms	917 ms
V.27 ter 4800 bps Short Train	52 ms	259 ms
V.27 ter 2400 bps Long Train	945 ms	1152 ms
V.27 ter 2400 bps Short Train	69 ms	276 ms
V.21 Channel 2 300 bps	≤ 14 ms	≤ 14 ms

Table 3. Turn-Off Sequence Times

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.17/V.33	13.3 ms	20 ms	33.3 ms
V.17 Short Train	13.3 ms	20 ms	33.3 ms
V.29 Long Train	5 ms	20 ms	25 ms
V.27 ter 4800 bps Long Train	7 ms	20 ms	27 ms
V.27 ter 4800 bps Short Train	7 ms	20 ms	27 ms
V.27 ter 2400 bps Long Train	10 ms	20 ms	30 ms
V.27 ter 2400 bps Short Train	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms

Notes:
1. In parallel data mode, the turn-off sequence may be extended by 8 bit times.
2. In HDLC mode, the turn-off sequence may be extended by more than 8 bit times.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.17 (RFX144V12-S), V.33 (RFX144V12-S), V.29, or V.27 ter recommendations, depending on the selected configuration.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable Received Line Signal Detector (~RLSD) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The ~RLSD threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

Receiver Timing

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever ~RLSD is off.

Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the receiver status. The tone detectors operate in all modes, except speakerphone where only tone detector one is operational. The filter coefficients of each filter are host programmable in RAM.

Voice Mode

The voice mode enables the host to efficiently record and playback voice messages. In this mode, the modem can compress a voice message to 5.7 kbps (5.9 kbps with error correction coding), and decompress a voice message at various pitch synchronized playback speeds. A room monitor feature is also supported.

Audio Mode

The audio mode enables the host to transmit and receive 8-bit or 16-bit audio signals. In this mode, the host can access the analog-to-digital (A/D) converter (ADC) and the digital-to-analog (D/A) converter (DAC). Incoming analog audio signals can then be converted to digital format and digital signals can be converted to analog audio output.

Speakerphone Mode

The speakerphone mode provides hands-free full-duplex telephone operation under host control. The host can separately control volume, muting, AGC, and tone generation in microphone and speaker channels. The speakerphone automatically recalculates loop control parameters to maintain duplexity and stability.

HARDWARE INTERFACE SIGNALS

The hardware interface signals are shown in Figure 1.

In Figure 1, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or −12 VDC for EIA/TIA-232-E) is called active low and is represented by a small circle at the signal point. Active low signals are indicated by a tilde (~), e.g., ~RESET. Edge-triggered clocks are indicated by a small triangle (e.g., TDCLK). Open-collector (open-source or open-drain) outputs are denoted by a small half circle (e.g., signal ~IRQ1).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The MDP pin assignments are shown in Figure 2 and hardware interface signals are listed by pin number in Table 4.

The SIA pin assignments are shown in Figure 3 and hardware interface signals are listed by pin number in Table 5.

The MDP hardware interface signals are defined in Table 6.

The SIA hardware interface signals are defined in Table 7.

Digital signal interface characteristics are defined in Table 8.

Analog signal interface characteristics are defined in Table 9.

Power consumption is listed in Table 10.

Absolute maximum ratings are specified in Table 11.

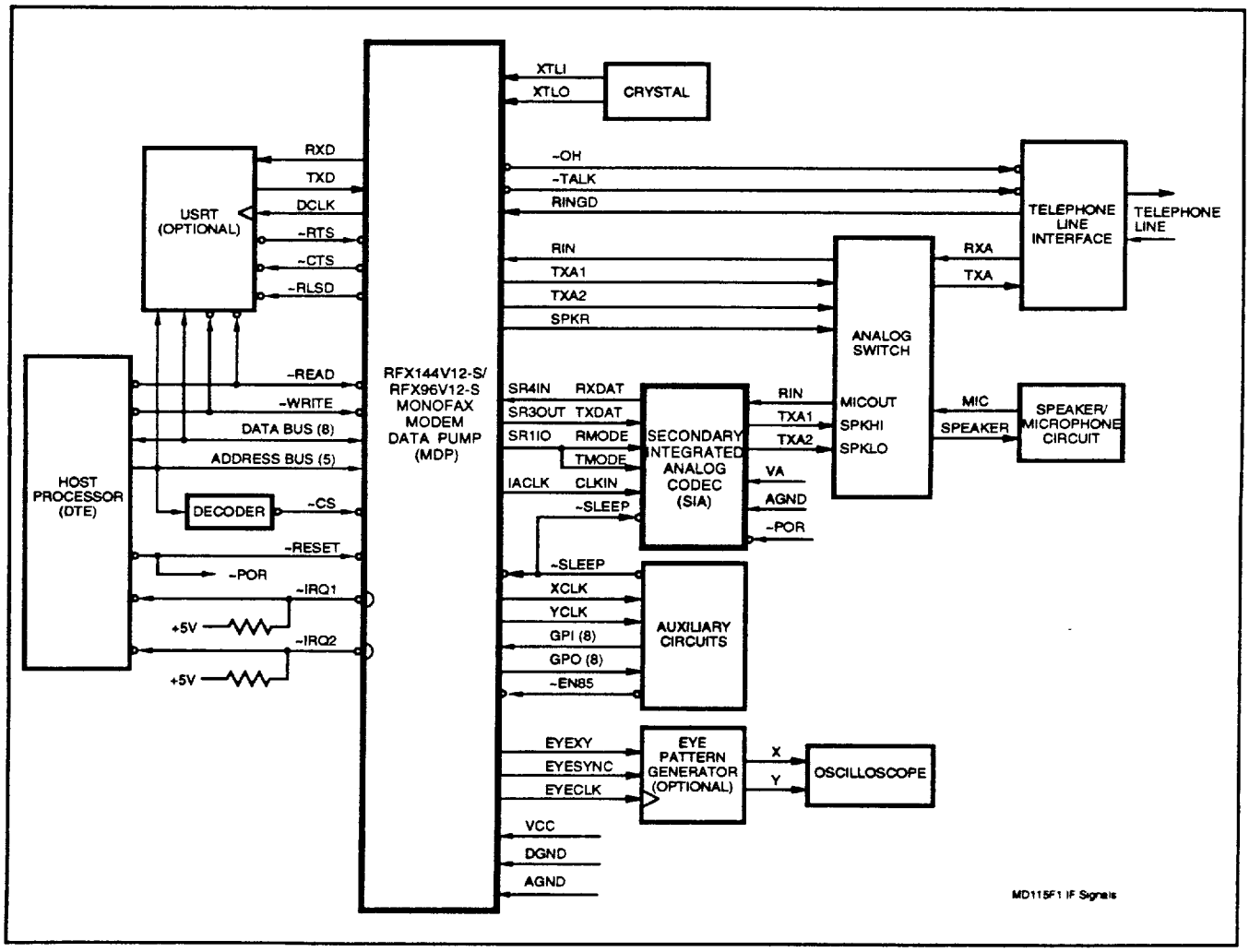


Figure 1. Modem Functional Interconnect Diagram

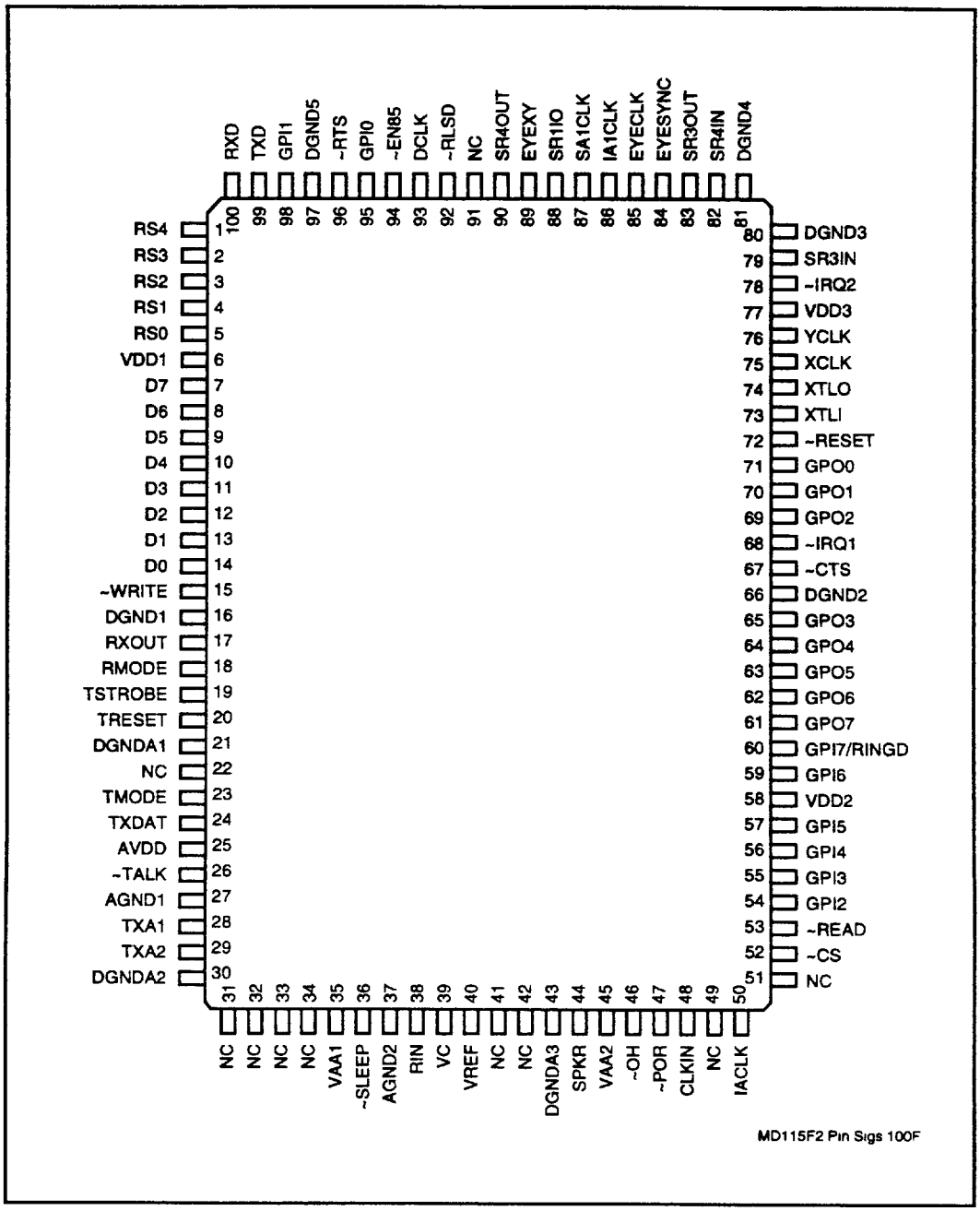


Figure 2. MDP Pin Signals - 100-Pin PQFP

Table 4. MDP Pin Signals - 100-Pin PQFP

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	RS4	IA	Host Parallel Interface	51	NC		
2	RS3	IA	Host Parallel Interface	52	~CS	IA	Host Parallel Interface
3	RS2	IA	Host Parallel Interface	53	~READ	IA	Host Parallel Interface
4	RS1	IA	Host Parallel Interface	54	GPI2	IA	General Purpose Input
5	RS0	IA	Host Parallel Interface	55	GPI3	IA	General Purpose Input
6	VDD1	PWR	VCC	56	GPI4	IA	General Purpose Input
7	D7	IA/OB	Host Parallel Interface	57	GPI5	IA	General Purpose Input
8	D6	IA/OB	Host Parallel Interface	58	VDD2	PWR	VCC
9	D5	IA/OB	Host Parallel Interface	59	GPI6	IA	General Purpose Input
10	D4	IA/OB	Host Parallel Interface	60	GPI7/RINGD	IA	General Purpose Input/Line Interface
11	D3	IA/OB	Host Parallel Interface	61	GPO7	OB	General Purpose Output
12	D2	IA/OB	Host Parallel Interface	62	GPO6	OB	General Purpose Output
13	D1	IA/OB	Host Parallel Interface	63	GPO5	OB	General Purpose Output
14	D0	IA/OB	Host Parallel Interface	64	GPO4	OB	General Purpose Output
15	~WRITE	IA	Host Parallel Interface	65	GPO3	OB	General Purpose Output
16	DGND1	GND	DGND	66	DGND2	GND	DGND
17	RXOUT	MI	MDP: SR3IN (79)	67	~CTS	OA	DTE Serial Interface
18	RMODE	MI	MDP: TMODE (23) & SR1IO (88); SIA: RMODE (7)	68	~IRQ1	OC	Host Parallel Interface
19	TSTROBE	MI	MDP: IA1CLK (86)	69	GPO2	OB	General Purpose Output
20	TRESET	MI	MDP: SA1CLK (87)	70	GPO1	OB	General Purpose Output
21	DGNDA1	GND	AGND	71	GPO0	OB	MDP: ~SLEEP (36)
22	NC			72	~RESET	OA	Reset Circuit
23	TMODE	MI	MDP: RMODE (18)	73	XTLI	I	Crystal/Clock Circuit
24	TXDAT	MI	MDP: SR4OUT (90)	74	XTLO	O	Crystal/Clock Circuit
25	AVDD	PWR	VCC through power decoupling filter	75	XCLK	OD	Diagnostic Circuit
26	~TALK	OD	Line Interface	76	YCLK	OD	Diagnostic Circuit
27	AGND1	GND	AGND	77	VDD3	PWR	VCC
28	TXA1	O(DD)	Analog Switch/Line Interface (TXA1)	78	~IRQ2	OC	Host Parallel Interface
29	TXA2	O(DD)	Analog Switch/Line Interface (TXA2)	79	SR3IN	MI	MDP: RXOUT (17)
30	DGNDA2	GND	AGND	80	DGND3	GND	DGND
31	NC			81	DGND4	GND	DGND
32	NC			82	SR4IN	MI	SIA: RXDAT (6)
33	NC			83	SR3OUT	MI	SIA: TXDAT (13)
34	NC			84	EYESYNC	OA	Eye Pattern Circuit
35	VAA1	PWR	VCC through power decoupling filter	85	EYECLK	OA	Eye Pattern Circuit
36	~SLEEP	MI	MDP: GPO0 (71); SIA: PD (21)	86	IA1CLK	MI	MDP: TSTROBE (19)
37	AGND2	GND	AGND	87	SA1CLK	MI	MDP: TRESET (20)
38	RIN	I(DA)	Analog Switch/Line Interface (RIN)	88	SR1IO	MI	MDP: TMODE (23) & RMODE (18)
39	VC	MI	AGND through capacitors	89	EYEXY	OA	Eye Pattern Circuit
40	VREF	MI	VC through capacitors	90	SR4OUT	MI	MDP: TXDAT (24)
41	NC			91	NC		
42	NC			92	~RLSD	OA	DTE Serial Interface
43	DGNDA3	GND	AGND	93	DCLK	OA	DTE Serial Interface
44	SPKR	O(DF)	Analog Switch/Speaker Circuit (SPKR)	94	~EN85	IA	Auxiliary Circuit
45	VAA2	PWR	VCC through power decoupling filter	95	GPI0	IA	General Purpose Input
46	~OH	OD	Line Interface	96	~RTS	IA	DTE Serial Interface
47	~POR	MI	MDP: ~RESET (72); SIA: ~POR (3)	97	DGND5	GND	DGND
48	CLKIN	MI	MDP: IACLK (50)	98	GPI1	IA	General Purpose Input
49	NC			99	TXD	IA	DTE Serial Interface
50	IACLK	MI	MDP: CLKIN (48); SIA: CLKIN (4)	100	RXD	OA	DTE Serial Interface

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB, IC, ID = digital input (see Table 8.
   - OA, OB, OC, OD = digital output (see Table 8).
   - I(DA) = analog input (see Table 9).
   - O(DD), O(DF) = analog output (see Table 9).
2. NC = No external connection allowed

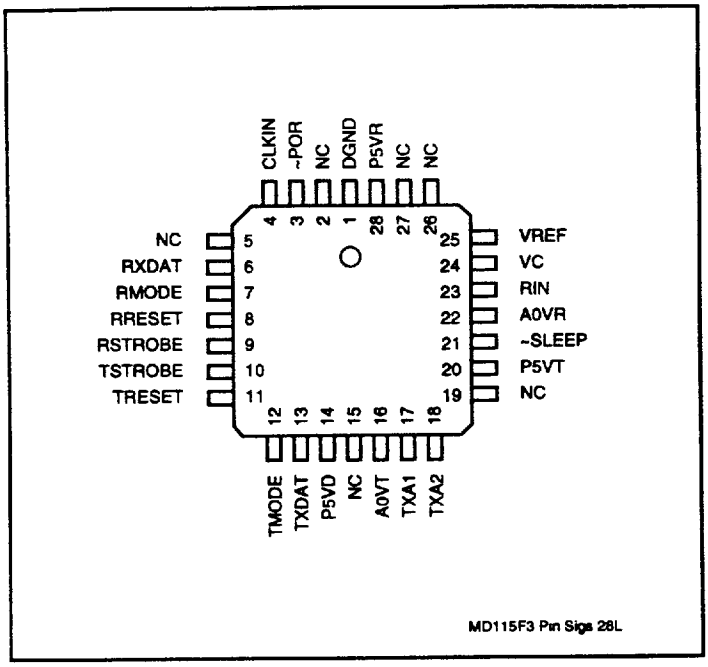


Figure 3. SIA Pin Signals - 28-Pin PLCC

Table 5. SIA Pin Signals - 28-Pin PLCC

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	DGND	GND	AGND	15	NC		NC
2	NC		NC	16	A0VT	GND	AGND
3	~POR	MI	MDP: ~POR (47)	17	TXA1 (SPKHI)	O(DD)	Analog Switch/Line Interface (SPKHI)
4	CLKIN	MI	MDP: IACLK (50)	18	TXA2 (SPKLO)	O(DD)	Analog Switch/Line Interface (SPKLO)
5	NC		NC	19	NC		NC
6	RXDAT	MI	MDP: SR4IN (82)	20	P5VT	PWR	To P5VD (14) & P5VR (28) & to o VCC through a power decoupling filter
7	RMODE	MI	MDP: RMODE (18); SIA: TMODE (12)	21	~SLEEP	MI	MDP: ~SLEEP (36)
8	RRESET		NC	22	A0VR	GND	AGND
9	RSTROBE		NC	23	RIN (MICIN)	I(DA)	Analog Switch/Line Interface (MICOUT)
10	TSTROBE		NC	24	VC	MI	AGND through capacitors
11	TRESET		NC	25	VREF	MI	VC through capacitors
12	TMODE	MI	SIA: RMODE (7)	26	NC		NC
13	TXDAT	MI	MDP. SR3OUT (83)	27	NC		NC
14	P5VD	PWR	To P5VT (20) & P5VR (28) & to VCC through a power decoupling filter	28	P5VR	PWR	To P5VD (14) & P5VT (20) & to o VCC through a power decoupling filter

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - I(DA) = analog input (see Table 9).
   - O(DD), O(DF) = analog output (see Table 9).
2. NC = No external connection allowed

Table 6. MDP Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	R,R	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a fundamental 49.92 MHz crystal, two capacitors, and a resistor, or a third overtone 49.92 MHz crystal, three capacitors, an inductor, and a resistor.
~RESET	ID	**Reset.** After application of +5V power to the modem, ~RESET must be held low for at least 15 ms after the +5V power reaches operating range. The modem is ready to use 25 ms after the low-to-high transition of ~RESET. The reset sequence initializes the modem interface memory (Table 10) to default values.
~POR	IA	**Power-On-Reset.** Connect to ~RESET.
VDDn	PWR	**Supply Voltage for DSP Circuits.** Connect to VCC.
AVDD	PWR	**Supply Voltage for PIA Digital Circuits.** Connect to VCC through decoupling circuit.
VAAn	PWR	**Supply Voltage for PIA Analog Circuits.** Connect to VCC through decoupling circuit.
DGNDn	GND	**Ground for DSP Circuits.** Connect to digital ground.
DGNDAn	GND	**Ground for PIA Digital Circuits.** Connect to analog ground.
AGNDn	GND	**Ground for PIA Analog Circuits.** Connect to analog ground.
		MICROPROCESSOR BUS INTERFACE
		Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. Note that the modem should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 2 YCLK cycles from a preceding write cycle.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (~READ-ø2) and Write Enable (~WRITE-R/~W) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when ~CS is low. These lines are typically connected to address lines A0-A4. When selected by ~CS low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
~CS	IA	**Chip Select.** The active low ~CS input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.

Table 6. MDP Hardware Interface Signal Definitions (Cont'd)

<table>
<tr><th>Label</th><th>I/O Type</th><th>Signal/Definition</th></tr>
<tr><td>~READ–ø2</td><td>IA</td><td>Read Enable–ø2. When ~EN85 is low (8085 bus selected), reading is controlled by the host pulsing ~READ input low during the microprocessor bus access cycle. The read timing is:
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Units</th></tr>
<tr><td>~CS Setup Time</td><td>TCS</td><td>0</td><td>–</td><td>ns</td></tr>
<tr><td>RSi Setup Time</td><td>TRS</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Data Access Time</td><td>TDA</td><td>–</td><td>45</td><td>ns</td></tr>
<tr><td>Data Hold Time</td><td>TDHR</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Control Hold Time</td><td>THC</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Phase 2 (ø2) Clock High</td><td>TP2CH</td><td>70</td><td>–</td><td>ns</td></tr>
</table>
Notes:
1. ~CS and ~READ must not both be active continuously.
2. A read or write operation following a read operation must be delayed by at least 1 YCLK cycle.</td></tr>
<tr><td>~WRITE–R/~W</td><td>IA</td><td>Write Enable–R/~W. When ~EN85 is low (8085 bus selected), writing is controlled by the host pulsing ~WRITE input low during the microprocessor bus access cycle. The write timing is:
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Units</th></tr>
<tr><td>~CS Setup Time</td><td>TCS</td><td>0</td><td>–</td><td>ns</td></tr>
<tr><td>RSi Setup Time</td><td>TRS</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Control Hold Time</td><td>THC</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Write Data Setup Time</td><td>TWDS</td><td>20</td><td>–</td><td>ns</td></tr>
<tr><td>Write Data Hold Time</td><td>TDHW</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Phase 2 (ø2) Clock High</td><td>TP2CH</td><td>70</td><td>–</td><td>ns</td></tr>
</table>
Notes:
1. A read or write operation following a write operation must be delayed by at least 2 YCLK cycles.</td></tr>
<tr><td>~IRQ1,
~IRQ2</td><td>OC,
OC</td><td>Interrupt Request. ~IRQ1 and ~IRQ2 interrupt request outputs may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. (The term, "~IRQ," refers to both the ~IRQ1 and ~IRQ2 output lines in the following discussion.) The ~IRQ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of ~IRQ is optional depending upon modem application.

The ~IRQ output structure is an open-drain field-effect-transistor (FET). The ~IRQ output can be wire-ORed with other ~IRQ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all ~IRQ lines have returned high).

Because of the open-drain structure of ~IRQ, an external pull-up resistor to +5V is required at some point on the ~IRQ line. The resistor value should be small enough to pull the ~IRQ line high when all ~IRQ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem ~IRQ output is used, a resistor value of 5.6K ohms, 20%, 0.25 W, is sufficient.</td></tr>
</table>

Table 6. MDP Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		V.24 SERIAL INTERFACE
		These pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/TIA-232-E voltage levels.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (PDM bit = 0), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (PDM bit = 1).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in parallel data mode.
~RTS	IA	**Request to Send.** The active low ~RTS input allows the modem to transmit data present at TXD in the serial data mode (PDM bit = 0), or in DBUFF in the parallel data mode (PDM bit = 1), when ~CTS becomes active. The ~RTS hardware control input is logically ORed with the RTSP bit (Table 10) by the modem to form the resultant control signal.
~CTS	OA	**Clear To Send.** ~CTS active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. ~CTS response times from ~RTS on are shown in Table 2. The ~CTS hardware status output parallels the operation of the CTSP bit (Table 10).
~RLSD	OA	**Received Line Signal Detector.** For V.17, V.33, V.29, and V.27 ter; ~RLSD goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the ~RLSD off-to-on response time is 816 baud times for V.17/V.33, V.29, and V.27 ter long train; 492 baud times for V.17/V.33; and 486 baud times for V.27 ter short train. The ~RLSD on-to-off time is 40 ± 5 ms for V.17/V.33, 35 ± 5 ms for V.29 or 11.6 ± 5 ms for V.27 ter. The ~RLSD on-to-off time ensures that all valid data bits have appeared on RXD. The ~RLSD programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a synchronous Data Clock (DCLK) for USRT timing. The DCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The DCLK low-to-high transitions coincide with the center of the data bits. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
		AUXILIARY SIGNALS
~EN85	IA	**Enable 85 Bus.** The ~EN85 input selects the modem microprocessor bus compatibility. When ~EN85 is low, the modem can interface directly to an 8085 compatible microprocessor bus using ~READ and ~WRITE. When ~EN85 is high, the modem can interface directly to a 6500 compatible microprocessor bus using ø2 and R/~W. In the 6500 configuration, the ~READ input becomes ø2 and the ~WRITE input becomes R/~W. This selection is performed only during initialization, i.e., when ~POR is asserted.
XCLK	OD	**XCLK Output.** XCLK is a 49.92 MHz square wave output derived from XTLI.
YCLK	OD	**YCLK Output.** YCLK is an 24.96 MHz square wave output derived from XTLI (XTLI divided by 2).
~SLEEP	IA	**Sleep.** A low on the ~SLEEP input causes the analog codec circuit to enter Sleep mode; a high wakes up the analog codec circuit. The ~SLEEP input should be connected to the GPO0 output pin. Entry into the modem Sleep mode is controlled by writing a 0 into the Sleep Mode Enable RAM parameter (see Table 13, item 50).

Table 6. MDP Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		TELEPHONE LINE INTERFACE
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. The output characteristics are the same as a 1458 type op amp.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit. The input impedance is > 70k ohms.
~OH	OD	**Off-Hook Relay Control.** The ~OH output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~OH is controlled by the RA bit in interface memory. In a typical application, ~OH is connected to the normally open Off-Hook relay. In this case, ~OH active closes the relay to connect the modem to the telephone line.
~TALK	OD	**Talk/Data Relay Control.** The ~TALK output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~TALK is controlled by the RB bit in interface memory. In a typical application, ~TALK is connected to the normally closed Talk/Data relay. In this case, ~TALK active opens the relay to disconnect the handset from the telephone line.
		SPEAKER INTERFACE
SPKR	O(DF)	**Received Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external audio power amplifier.
		GENERAL PURPOSE INPUT/OUTPUT LINES
GPI0-GPI7	IA	**General Purpose Inputs.** Eight general purpose input (GPI) pins are available to the host for programming via the modem interface memory.
RINGD (GPI7)	IA	**Ring Frequency Detected.** The RINGD signal from the DAA, when connected to the GPI7 input, is monitored for pulses in the range of 15 Hz to 68 Hz (with an 8000 Hz sample rate). The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. The RI status bit in the interface memory reflects the logic level on the GPI7 pin.
GPO0-GPO7	OB	**General Purpose Outputs.** Eight general purpose output (GPO) pins are available to the host for programming via the modem interface memory. GPO0 is used by the modem to control power down mode for the SIA (unless disabled by the host). In this case, connect the GPO0 output to the ~SLEEP input. GPO0-GPO7 are all set to a 1 state by a POR (power-on reset).
SPEAK (GPO5)	OB	**Speaker Line Select.** The SPEAK output is used to enable (SPEAK high) or disable (SPEAK low) the SPKR output from the MDP PIA to the speaker amplifier circuit in the analog switch (see Figures 5 and 9).

Table 6. MDP Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		EYE DIAGNOSTIC INTERFACE
		Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output. Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 16-bit diagnostic words (EYEX and EYEY) for display on an oscilloscope. EYEX data is the first 16 bits, MSB first, that are shifted out on the high portion of the EYESYNC clock. EYEX is a serial bit stream that is the equivalent of modem interface memory register XDAM1 followed by XDAL1. EYEY data is the second 16 bits, MSB first, that are shifted out on the low portion of the EYESYNC clock. EYEY is a serial bit stream that is the equivalent of modem interface memory register YDAM1 followed by YDAL1.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 345.6 KHz clock. Since the EYEXY data is shifted out on the rising edge of EYECLK, any eye pattern generator circuitry should sample EYEXY on the falling edge of EYECLK.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe that indicates whether the EYEX or EYEY portion of EYEXY is being shifted. The EYESYNC frequency is equal to the sample rate of the modem configuration.
		REFERENCE SIGNALS AND MODEM INTERCONNECT
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
SR1IO	MI	**SR1IO.** Connect to MDP: TMODE (23) & RMODE (18).
TMODE	MI	**Transmitter Mode.** Connect to MDP: RMODE (18).
RMODE	MI	**Receiver Mode.** Connect to MDP: TMODE (23) & SR1IO (88), and to SIA: RMODE (7).
SR3IN	MI	**SR3IN.** Connect to MDP: RXOUT (17).
RXOUT	MI	**Receive Data Out.** Connect to MDP: SR3IN (79).
SR4OUT	MI	**SR4OUT.** Connect to MDP: TXDAT (24).
TXDAT	MI	**Transmit Data In.** Connect to MDP: SR4OUT (90).
IACLK	MI	**IACLK.** Connect to MDP: CLKIN (48) and to SIA: CLKIN (4).
CLKIN	MI	**CLKIN.** Connect to MDP: IACLK (50).
IA1CLK	MI	**IA1CLK.** Connect to MDP: TSTROBE (19).
TSTROBE	MI	**Transmitter Strobe.** Connect to MDP: IA1CLK (86).
SA1CLK	MI	**SA1CLK.** Connect to MDP: TRESET (20).
TRESET	MI	**Transmitter Reset.** Connect to MDP: SA1CLK (87).
SR4IN	MI	**SR4IN.** Connect to SIA: RXDAT (6).
SR3OUT	MI	**SR3OUT.** Connect to SIA: TXDAT (13).

Notes:
1. I/O types:
   MI = Modem interconnect.
   IA, IB, IC, ID = digital input (see Table 8).
   OA, OB, OC, OD = digital output (see Table 8).
   I(DA) = analog input (see Table 9).
   O(DD), O(DF) = analog output (see Table 9).

Table 7. SIA Hardware Interface Signal Definitions

Label	I/O Type	Signal Name/Description
		OVERHEAD SIGNALS
P5VD, P5VT, P5VR	PWR	**Supply Voltage.** Connect to VCC through a power decoupling filter.
DGND, A0VT, A0VR	GND	**Ground.** Connect to analog ground.
		REFERENCE SIGNALS AND MODEM INTERCONNECT
TXA1 (SPKHI), TXA2 (SPKLO)	O(DF)	**Transmit Analog 1 and 2 (Speaker Output).** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. The output characteristics are the same as a 1458 type op amp.
RIN (MICOUT)	I(DA)	**Receive Analog (Microphone Output).** RIN is a single-ended microphone input from the analog switch circuit. The input impedance is > 70k ohms.
		REFERENCE SIGNALS AND MODEM INTERCONNECT
~POR	MI	**Power-On-Reset.** Connect to MDP: ~POR (47).
~SLEEP	MI	**Sleep.** Connect to MDP: ~SLEEP (36).
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
RXDAT	MI	**Receive Data In.** Connect to MDP: SR4IN (82).
TXDAT	MI	**Transmit Data In.** Connect to MDP: SR3OUT (83).
TMODE	MI	**Transmitter Mode.** Connect to SIA: RMODE (7).
RMODE	MI	**Receiver Mode.** Connect to MDP: RMODE (18) and SIA: TMODE (12).
CLKIN	MI	**CLKIN.** Connect to MDP: IACLK (50).

Notes:
1. I/O types:
   MI = Modem interconnect.
   I(DA) = analog input (see Table 9).
   O(DD), O(DF) = analog output (see Table 9).

Table 8. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA and IB		2.0	–	V_{CC}		
Type IC and ID		0.8 V_{CC}	–	V_{CC}		
Input High Current	I_{IH}				µA	VCC = 5.25 V, V_{IN}= 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}				VDC	
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (V_{CC})		
Input Low Current	I_{IL}				µA	VCC = 5.25 V
Type IB and IC		–	–	–400		
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0 to +5V, VCC = 5.25V
Types IA and ID						
Output High Voltage	V_{OH}		–	–	VDC	
Type OA and OB		3.5	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD						I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD}= 15 mA
Output Leakage Current	I_{LO}			±10	µADC	V_{IN} = 0.4 to VCC-1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID			–	10		
Type IB			–	20		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC			–	10		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Relay driver

Table 9. Analog Electrical Characteristics

Name	Type	Characteristic	Value
		MDP	
RIN	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 70K Ω 1.7 VP-P +2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 Ω 0.01 µF 10 Ω 1.2 VP-P @9600 Hz sample rate 2.7 VP-P @8000 Hz sample rate +2.5 VDC ± 200 mV
SPKR	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 Ω 0.01 µF 10 Ω 2.0 VP-P +2.5 VDC ± 20 mV
		SIA	
RIN (MICOUT)	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 70K Ω 1.7 VP-P +2.5 VDC
TXA1 (SPKHI), TXA2 (SPKLO)	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	300 Ω 0.01 µF 10 Ω 2.7 VP-P +2.5 VDC ± 200 mV
* Reference voltage provided internal to the device.			

Table 10. Current and Power Requirements

Mode	Current (ID)			Power (PD)			Notes
	Typical @ 25° (mA)	Maximum @ 0°C (mA)	Maximum @ -40°C[1] (mA)	Typical @ 25°C (mW)	Maximum @ 0°C (mW)	Maximum @ -40°C[1] (mW)	
MDP							
Normal mode	114	136	147	570	713	770	
Sleep mode	2.0	2.5	3.0	10.0	13.1	15.8	
SIA							
Normal mode	10	13	16	50	68	85	
Sleep mode	0.15	0.3	0.45	0.8	1.6	2.4	
Total							
Normal mode	124	149	163	620	781	855	
Sleep mode	2.15	2.80	3.45	10.8	14.7	18.2	

Notes:
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA
Operating Temperature Range	T_A		°C
Commercial		0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
Speakerphone Parameters			
Line Echo Return Loss	LERL	+6	dB
Room Echo Return Loss	RERL	+12	dB

Note: Echo Return Loss is measured between TXA1 or TXA2 and RIN at all in-band frequencies.

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the MDP DSP.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 4). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

The interface memory bits are defined in Table 12. The interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = least significant bit).

DSP RAM ACCESS

The DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM. The DSP also contains a single bank RAM (SBADxy) which the host can read or write.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud (frame in voice and sample in speakerphone), or sample time, as selected by the BR1 and BR2 bits. The baud (frame) rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz (8000 Hz in voice and speakerphone).

The DSP RAM access functions, codes, and registers are identified in Table 13.

MODEM INTERFACE CIRCUIT

CIRCUIT AND COMPONENTS

The modem is supplied in a 100-pin PQFP (MDP) and a 28-pin PLCC (SIA) for design into OEM circuit boards. The recommended modem interface circuits shown in Figure 5 illustrate the connections and components required to connect the modem to the OEM electronics.

Figure 6 shows a typical line interface.

Figure 7 shows a typical line interface using an external hybrid. In Figure 7, resistors R7 and R9 can be used to trim the transmit level and receive threshold, respectively, to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

Figure 8 shows a recommended microphone circuit.

Figure 9 shows a typical speaker circuit.

Register Function	Reg. Addr.	Bit 7	6	5	4	3	2	1	0	Default
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	XX0-XX0
	1E	B2IA	B1IA	B2I1E	B2I2E	B2A	B1I1E	B1I2E	B1A	--00-00-
High Speed Control & Status	1D	SHPR	ASPEED	PR*	PRDET*	—	—	—	—	0000XXXX
DTMF Status	1C	EDET	DTDET	OTS	DTMFD	DTMF				--------
General Purpose Outputs	1B	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0	11111111
RAM Access and Voice/Relay Control	1A	SBRAM2	SBRAM1	DCDEN	CDEN	VOXREC	AGCDIS	RB	RA	00000X00
Not Available	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
Voice Mode Status	17	EDETC	DTDETC	OTSC	DTMFDC	VOX	RI	FRx	VOVUN	--------
General Purpose Inputs	16	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0	--------
RAM Access 2 Control and HDLC Control	15	ACC2	AREX2	AEOF	DR2	IO2	BR2	WRT2	CR2	00000000
Voice Decoder Mode	14	—	—	—	0	FAST50	FAST33	SLOW	NORM	---00001
RAM Access 2 Address/Data	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)/SINGLE BANK RAM ADDRESS 2 MSB (SBAD2M)								--------
	12	X RAM DATA 2 LSB (XDAL2)/SINGLE BANK RAM ADDRESS 2 LSB (SBAD2L)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
Speakerphone Control	0F		TONEPE	TONESE	AGCPE	AGCSE	—	ECHOAT		-0011-00
	0E	TTONEE	VOLUP	VOLDWN	SP/HS	MUTEP	MUTES	MICLVL		-0010101
High Speed Status	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	FSKFLS	—	—	—	—	—	—	—	-XXXXXXX
	0D	RX	PNDET	—	—	—	HPFEN	—	—	--XXX0XX
	0C	—	—	DATA	SCR1	PN	P2	P1	—	XX-----X
Programmable Interrupts	0B	ITBMSK								00000000
	0A	TRIG	ANDOR	ITADRS						00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC	FSK7E	DCABLE	PDEQZ	0000-000
Mode Control**	07	RTSP	TDIS/ CODECS	PDM/ RMM	SHTR	EPT	SQEXT	0	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control and Programmable Interrupt Control	05	ACC1	AREX1	PIDR	DR1	IO1	BR1	WRT1	CR1	10000101
RAM Access 1 Address/Data	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)/SINGLE BANK RAM ADDRESS 1 MSB (SBAD1M)								--------
	02	X RAM DATA 1 LSB (XDAL1)/SINGLE BANK RAM ADDRESS 1 LSB (SBAD1L)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

Notes:
* RFX144V12-S only.
** A changed value in these registers (except RTSP and TDIS) require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- This symbol in the "Default Value" column indicates that the value is determined by operating conditions.

Figure 4. Modem Interface Memory Map

Table 12. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
12TH	08:4	0	**Select 12th Order.** When control bit 12TH is a 1, the tone detectors operate as one 12th order filter (uses FR3).When 12TH is a 0, the tone detectors operate as three parallel independent 4th order filters (FR1, FR2, FR3).The 12th bit is valid in all reception modes.
ABIDL	09:3	–	**Abort/Idle.** In HDLC mode, when the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is a 1) and the modem will send at least eight continuous ones (if ZEROC is a 0) or eight continuous zeros (if ZEROC is a 1).To stop continuous ones or zeros transmission, ABIDL must be reset by the host. In HDLC mode, when the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host.
ACC1	05:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in ADD1, and the AREX1 and CR1 bits. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in ADD2, and the AREX2 and CR2 bits. WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1, in conjunction with AREX1, contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 least significant byte (LSB) and most significant byte (MSB) words (02:0-7 and 03:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2, in conjunction with AREX2, contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
AEOF	15:5	0	**Automatic End of Frame.** When the modem is configured as an HDLC transmitter and AEOF control bit is a 1, the modem interprets an underrun condition as an end of frame and outputs the FCS and at least one ending flag. (HDLC mode.)
AGCDIS	1A:2	0	**AGC Disable.** When the modem is configured for Voice Mode (CONF = 90h), the AGCDIS control bit disables (AGCDIS = 1) or enables (AGCDIS = 0) the AGC in the voice coder.
AGCPE	0F:4	1	**AGC in PIA ADC Enable.** In speakerphone mode, the AGC in the PIA ADC is enabled when control bit AGCPE is a 1; the AGC gain is forced to 0 dB when AGCPE is a 0.
AGCSE	0F:3	1	**AGC in SIA ADC Enable.** In speakerphone mode, the AGC in the SIA ADC is enabled when control bit AGCSE is a 1; the AGC gain is forced to 0 dB when AGCSE is a 0.
ANDOR	0A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled (PIE bit = 1), the modem will assert ~IRQ1 if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert ~IRQ1 if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a 1.
AREX1	05:6	0	**RAM Access 1 Code Extension Select.** When control bit AREX1 is a 1, the upper part (80h-FFh) of the RAM is selected. When AREX1 is a 0, the lower part (0-7Fh) is selected.
AREX2	15:6	0	**RAM Access 2 Code Extension Select.** When control bit AREX2 is a 1, the upper part (80h-FFh) of the RAM is selected. When AREX2 is a 0, the lower part (0-7Fh) is selected.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
ASPEED	1D:6	0	**Auto Speed Change Enable.** When control bit ASPEED is a 0, the modem transmitter sends the default V.17 rate sequence. The modem receiver stores the rate sequence in RAM. (V.17 modes.) **ASPEED — Data Rate — Rate Sequence Pattern** 0 — V.17, all rates — 0111h 1 — 14400 bps — 0171h 1 — 12000 bps — 01B1h 1 — 9600 bps — 01F1h 1 — 7200 bps — 0331h When set to a 1, the modem transmitter sends a different rate sequence depending on the selected TCM configuration. When receiving in a TCM configuration, the modem reconfigures to the received rate sequence. The new configuration is reflected in the receiver CONF register.
B1A	1E:0	–	**Buffer 1 Available.** When set to a 1, status bit B1A signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (00:0-7). This condition can also cause ~IRQ1 or ~IRQ2 to be asserted. The host writing to or reading from register 00 resets the B1A and B1IA bits to 0. (See B1I1E, B1I2E, and B1IA.)
B1I1E	1E:2	0	**Buffer 1 Interrupt 1 Enable.** When control bit B1I1E is a 1, ~IRQ1 is enabled for Buffer 1, i.e., the modem will assert ~IRQ1 and set B1IA to a 1 when B1A is set to 1 by the modem. When B1I1E is a 0, B1A has no effect on ~IRQ1 and B1IA. (See B1A and B1IA.)
B1I2E	1E:1	0	**Buffer 1 Interrupt 2 Enable.** When control bit B1I2E is a 1, ~IRQ2 is enabled for Buffer 1, i.e., the modem will assert ~IRQ2 when B1A is set to 1 by the modem. When B1I2E is a 0, B1A has no effect on ~IRQ2. (See B1A.)
B1IA	1E:6	–	**Buffer 1 Interrupt Active.** When Buffer 1 interrupt is enabled (B1I1E is a 1) and B1A is set to a 1 by the modem, the modem asserts ~IRQ1 and sets status bit B1IA to a 1 to indicate that B1A caused the interrupt. The host writing to or reading from register 00 resets B1IA to a 0. (See B1I1E and B1A.)
B2A	1E:3	–	**Buffer 2 Available.** When set to a 1, status bit B2A signifies that, when the modem is in the parallel data mode (with or without HDLC selected), it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of B2A to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). When the modem is configured for voice mode (CONF = 90h), the modem sets B2A to indicate that the modem has loaded encoder output data into DBUFF (coder enabled, i.e., CDEN = 1 and DCDEN = 0)) or that the modem has read decoder input data from DBUFF (decoder enabled, i.e., DCDEN = 1 and CDEN = 0). The modem setting B2A can also cause ~IRQ1 or ~IRQ2 to be asserted. The host writing to or reading from register 10h resets the B2A and B2IA bits to 0. (See B2I1E, B2I2E, and B2IA.)
B2I1E	1E:5	0	**Buffer 2 Interrupt 1 Enable.** When control bit B2I1E is a 1, ~IRQ1 is enabled for Buffer 2, i.e., the modem will assert ~IRQ1 and set B2IA to a 1 when B2A is set to a 1 by the modem. When B2I1E is a 0, B2A has no effect on ~IRQ1 and B2IA. (See B2A and B2IA.)
B2I2E	1E:4	0	**Buffer 2 Interrupt 2 Enable.** When control bit B2I2E is a 1, ~IRQ2 is enabled for Buffer 2, i.e., the modem will assert ~IRQ2 when B2A is set to a 1 by the modem. When B2I2E is a 0, B2A has no effect on ~IRQ2. (See B2A.)
B2IA	1E:7	–	**Buffer 2 Interrupt Active.** When Buffer 2 interrupt is enabled (B2I1E is a 1) and B2A is set to a 1 by the modem, the modem asserts ~IRQ1 and sets status bit B2IA to a 1 to indicate that B2A caused the interrupt. The host writing to or reading from register 10 resets B2IA to a 0. (See B2I1E and B2A.)

Table 12. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
BR1	05:2	1	**Baud Rate 1.** In high speed modem modes, when control bit BR1 is a 1, RAM access for ADD1 occurs at the baud rate regardless of the state of DR1. When BR1 is a 0, RAM access occurs at the sample rate or data rate (See DR1). The BR1 bit must be reset to a 0 for tone, audio, or speakerphone mode. In voice mode, when control bit BR1 is a 1, RAM access for ADD1 or SBAD1x (x = L and M) occurs at the frame rate regardless of the state of DR1. When BR1 is a 0, RAM access occurs at the sample rate (8000 Hz).
BR2	15:2	0	**Baud Rate 2.** In high speed modem modes, when control bit BR2 is a 1, RAM access for ADD2 occurs at the baud rate regardless of the state of DR2. When BR2 is a 0, RAM access occurs at the sample rate or data rate (See DR2). The BR2 bit must be reset to a 0 for tone, audio, or speakerphone mode. In voice mode, when control bit BR2 is a 1, RAM access for ADD2 or SBAD2x (x = L and M) occurs at the frame rate regardless of the state of DR2. When BR2 is a 0, RAM access occurs at the sample rate (8000 Hz).
CDEN	1A:4	0	**Coder Enable.** In voice mode, the modem performs voice coding when control bit CDEN is a 1. The coder output is placed into DBUFF. Status bit B2A will be set by the modem when the coder output buffer becomes full (DBUFF). ACC2 must be reset. DCDEN must be a 0 when CDEN is a 1.
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or is in the process of training.
CODECS	07:6	0	**Codec Select.** In voice mode, the CODECS control bit selects data input source and output destination. When CODECS is a 1, the SIA ADC signal is recorded and the playback is sent to both the PIA and SIA. When CODECS is a 0, only the PIA ADC is activated.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	06:0-7	14	**Configuration.** The CONF control bits select one of the following configurations: **CONF (Hex) — Configuration** 31 — V.17/V.33 14400 bps. (RFX144V12-S only.)* 32 — V.17/V.33 12000 bps. (RFX144V12-S only.)* 34 — V.17 9600 bps. (RFX144V12-S only.)* 38 — V.17 7200 bps. (RFX144V12-S only.)* 71 — 14400 bps with 1700 Hz carrier (non-standard TCM). (RFX144V12-S only.)* 72 — 12000 bps with 1700 Hz carrier (non-standard TCM). (RFX144V12-S only.)* 74 — 9600 bps with 1700 Hz carrier (non-standard TCM). (RFX144V12-S only.)* 78 — 7200 bps with 1700 Hz carrier (non-standard TCM). (RFX144V12-S only.)* 14 — V.29 9600 bps. * 12 — V.29 7200 bps. * 11 — V.29 4800 bps. * 0A — V.27 ter 4800 bps. * 09 — V.27 ter 2400 bps. * 20 — RTS on: V.21 Ch. 2 300 bps FSK transmit. * RTS off: V.21 Ch. 2 300 bps FSK receive and tone detect. * 21 — RTS on: V.21 Ch. 2 300 bps FSK transmit. * RTS off: V.21 Ch. 2 300 bps FSK receive, tone detect, and DTMF. * 22 — V.23 receive 1200 bps. * 80 — RTS on: Dual/single tone transmit. * RTS off: Tone detectors. * 82 — RTS on: 8-bit audio mode transmit. ** RTS off: 8-bit audio mode receive and tone detect. ** 86 — RTS on: 16-bit audio mode transmit. ** RTS off: 16-bit audio mode receive and tone detect. ** 90 — Voice mode. *** DCDEN on & HDLC off: 5.7 kbps voice decoder without error correction, DTMF, and tone detect. DCDEN on & HDLC on: 5.9 kbps voice decoder with error correction, DTMF, and tone detect. CDEN on & HDLC off: 5.7 kbps voice coder without error correction, DTMF, and tone detect. CDEN on & HDLC on: 5.9 kbps voice coder with error correction, DTMF, and tone detect. CDEN off & DCDEN off: DTMF and tone detect. CODECS on & RMM on: Room monitor, DTMF, and tone detect. CODECS on & RMM off: Changing recording source to SIA, DTMF, and tone detect. 91 — Full-duplex speakerphone. *** SP/HS on: Full-duplex (FDX) speakerphone operation SP/HS off: Handset operation * Sample rate is 9600 Hz. ** Sample rate is 8000 Hz. *** Sample rate is 8000 Hz. For tone detectors only, the sample rate is 4000 Hz. **Configuration Definitions:** **V.17.** The modem operates as specified in CCITT Recommendation V.17. **V.33.** The modem operates as specified in CCITT Recommendation V.33. **V.29.** The modem operates as specified in CCITT Recommendation V.29. **V.27 ter.** The modem operates as specified in CCITT Recommendation V.27 ter. **V.23 Receive.** The modem operates as specified in CCITT Recommendation V.23. **V.21 Channel 2.** The modem operates as specified in CCITT Recommendation V.21 Channel 2. **V.21 Channel 2 and DTMF Receiver.** The modem operates as specified in CCITT Recommendation V.21 Channel 2 and detects DTMF transmissions.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
			Configuration Definitions: (Cont'd) **Tone Transmit.** The modem transmits single or dual frequency tones in response to the RTS input pin or RTSP bit. Tone frequencies and amplitudes are programmable in the DSP RAM. **Tone Detect.** When the Tone Detect configuration is selected and 12TH is a 1, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12TH is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable. **High Speed Modes.** The 2400 bps through 14400 bps modes. **Voice Mode.** DTMF and three tone detectors are available. During the decoder operation a local echo canceller is used to improve DTMF and tone detector operation. Control bits FAST50, FAST33, and SLOW can be configured at anytime to select the decoder playback speed to be 50% faster, 33% faster, or 50% slower than normal playback speed. The NORM control bit selects normal playback speed. The state of RTS and RTSP have no effect on the operation in CONF 90. The SETUP bit must be set to change configurations. **Full-duplex Speakerphone Mode.** Two DTMF generators and one tone detector are available. Control bits at register locations 0E and 0F can be configured at anytime to select speakerphone functions such as AGC enable/disable, muting, tone transmit, volume control, and speakerphone/handset switch.
CR1	05:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, AREX1 and ADD1 address Coefficient RAM. When CR1 is a 0, AREX1 and ADD1 address Data RAM. This bit must be set according to the desired RAM address (Table 13).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, AREX2 and ADD2 address Coefficient RAM. When CR2 is a 0, AREX2 and ADD2 address Data RAM. This bit must be set according to the desired RAM address (Table 13).
CRC	09:1	–	**Cyclic Redundancy Check Error.** In HDLC mode, when status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC changes immediately before EOF is set to a 1. In Caller ID mode (CONF = 22h), the modem sets the CRC bit if the stop bit is detected to be a 1.
CTSP	0F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD (PDM = 0) or DBUFF (PDM = 1) will be transmitted. CTSP parallels the operation of the ~CTS pin.
DATA	0C:5	–	**Data Mode.** When status bit DATA is a 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode (PDM bit = 1), the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first. The modem reading (taking data) or writing (sending data) to this register sets the B2A bit. The host reading (taking data) or writing (sending data) to this register resets the B2A bit. By setting B2IxE (x=1 or 2), the host can enable the assertion of ~IRQx upon the setting of B2A. Bit 0 of DBUFF is the first bit of the 8-bit input or output. In voice mode, DBUFF is the 8-bit voice decoder input buffer (DCDEN = 1 and CDEN = 0) or voice coder output buffer (CDEN = 1 and DCDEN = 0).
DCABLE	08:1	0	**Digital Cable Equalizer Enable.** Control bit DCABLE enables (1) or disables (0) insertion of the digital cable equalizer into the high speed receive and transmit paths.
DCDEN	1A:5	0	**Decoder Enable.** When control bit DCDEN is a 1 and bit CDEN is a 0, the modem performs voice decoding on the DBUFF input. The decoder output is sent to TXA1/TXA2. Status bit B2A is set by the modem when the decoder's input buffer is empty. CDEN must be reset when DCDEN is a 1. ACC2 must be reset. (Voice mode.)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DR1	05:4	0	**Data Rate 1.** In high speed, FSK/DTMF, or FSK modes, when control bit DR1 is a 1, RAM access associated with ADD1 occurs at the modem data rate if BR1 = 0. When DR1 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR1.
DR2	15:4	0	**Data Rate 2.** In high speed, FSK/DTMF, or FSK modes, when control bit DR2 is a 1, RAM access associated with ADD2 occurs at the modem data rate if BR2 = 0. When DR2 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR2.
DTDET	1C:6	–	**Dual Tone Detected.** When configured as an DTMF receiver, the modem sets status bit DTDET to a 1 when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMF Output Word (1C:0-3) value is available when DTDET is a 1. If the received signal is a valid DTMF signal, then DTDET will be set to a 1 approximately 11 ms following EDET setting to a 1. The DTDET bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
DTDETC	17:6	0	**Dual Tone Detected Copy.** In DTMF modes, DTDETC is a copy of the DTDET bit for programmable interrupt control.
DTMF	1C:0-3	–	**DTMF Output Word.** When configured as an DTMF receiver and a DTMF signal is present such that status bit DTDET is set by the modem, the encoded DTMF output is written to 1C:0-3. The DTMF symbol codes are: DTMF Symbol / Encoded Output (Hex): 1→0, 4→1, 7→2, *→3, 2→4, 5→5, 8→6, 0→7, 3→8, 6→9, 9→A, #→B, A→C, B→D, C→E, D→F
DTMFD	1C:4	–	**DTMF Signal Detected.** When configured as an DTMF receiver, the modem sets status bit DTMFD to a 1 when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading the DTMF Output Word (1C:0-7), otherwise two or more detections of the same symbol may be missed by the host.
DTMFDC	17:4	0	**DTMF Detected Copy.** In DTMF modes, DTMFDC is a copy of the DTMFD bit for programmable interrupt control.
ECHOAT	0F:0-1	00	**Handset Echo Attenuation.** In speakerphone mode, ECHOAT bits control the level of the simulated echo for handset operation when the SP/HS bit is a 0. The signal entering the SIA ADC is attenuated and retransmitted to the SIA DAC as follows: Bit 1 / Bit 0 / Attenuation: 0 0 → -∞ dB; 0 1 → -18 dB; 1 0 → -12 dB; 1 1 → -06 dB
EDET	1C:7	–	**DTMF Early Detection.** When configured as an DTMF receiver, the modem sets status bit EDET to a 1 approximately 20 ms after the DTMF signal energy is detected to indicate that the received signal is probably a DTMF signal. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
EDETC	17:7	0	**Early Detection Copy.** In DTMF modes, EDETC is a copy of the EDET bit for programmable interrupt control.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
EOF	09:2	–	**End of Frame.** In HDLC mode, when the modem is configured as a transmitter and bit AEOF is a 0, the EOF bit is a control bit. When AEOF is a 0, to convey to the modem that it is time to send the 16-bit FCS and ending flag of an HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (B2A sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a transmitter and bit AEOF is a 1, EOF is a status bit. In this case, the modem will interpret the underrun condition as the end of the frame, set EOF, and will output the 16-bit FCS and at least one ending flag. EOF is reset whenever a flag is transmitted. When the modem is configured as a receiver and bit AEOF is a 1, the modem has received a frame ending flag and the CRC bit is updated. EOF must be reset by the host before receiving the ending flag of a following frame.
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 long train which transmits 20 ms of silence at the beginning of training. (See status bit P1.)
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. For short train only, this bit is used in conjunction with the SHTR bit.
FAST33	14:2	0	**Faster by 33% Playback Speed.** When control bit FAST33 is a 1 and the FAST50, SLOW, and NORM control bits are reset, 33% faster than normal playback speed is selected, i.e., playback time is 67% of normal playback time. FAST33 must be reset when another speed is selected.
FAST50	14:3	0	**Faster by 50% Playback Speed.** When control bit FAST50 is a 1 and the FAST33, SLOW, and NORM control bits are reset, 50% faster than normal playback speed is selected, i.e., playback time is 50% of normal playback time. FAST50 must be reset when another speed is selected.
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes: Bit 7 / Bit 6 / Energy Level 0 / 0 / No energy (idle mode) 0 / 1 / Invalid 1 / 0 / Above Turn-off Threshold 1 / 1 / Above Turn-on Threshold
FLAG	09:0	–	**FLAG Mode.** When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode.)
FR1	08:5	–	**Frequency No. 1.** The modem sets status bit FR1 to a 1 when energy above tone detector 1's turn-on threshold is detected. The default detection range = 2100 Hz ± 25 Hz for all configurations except voice mode. In voice mode, the FR1 tone detector sampling rate is 4000 Hz versus 9600 Hz in the other configurations. The FR1 detector must be reprogrammed in voice mode.
FR2	08:6	–	**Frequency No. 2.** The modem sets status bit FR2 to a 1 when energy above tone detector 2's turn-on threshold is detected. The default detection range = 1100 Hz ± 30 Hz for all configurations except voice mode. In voice mode, the FR2 tone detector sampling rate is 4000 Hz versus 9600 Hz in the other configurations. The FR2 detector must be reprogrammed in voice mode.
FR3	08:7	–	**Frequency No. 3.** The modem sets status bit FR3 to a 1 when energy above tone detector 3's turn-on threshold is detected, The default detection range = 462 Hz ±14 Hz for all configurations except voice mode. In voice mode, the FR3 tone detector sampling rate is 4000 Hz versus 9600 Hz in the other configurations. The FR3 detector must be reprogrammed in voice mode

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
FRx	17:1	-	**Frequency No. 1, 2, or 3.** Status bit FRx is set by the modem if FR1, FR2, or FR3 is set. FRx is reset by the modem if FR1, FR2, and FR3 are reset.
FSK7E	08:2	–	**FSK FLAG (7E) Detected.** The modem sets status bit FSK7E to a 1 when FSK flags have been detected in a high speed receiver mode. FSK7E is valid after bit FSKFLS transitions from 1 to 0. FSK7E is not valid in V.27 ter short train mode.
FSKFLS	0E:7	0	**FSK FLAG (7E) Search.** When status bit FSKFLS is a 1, the modem is searching for FSK flags in high speed receiver modes except V.27 ter short train. This bit is reset by the modem when the FSK flag search is completed.
GPIx	16:0-7	-	**General Purpose Inputs.** The modem sets/resets bits 0 -7 in the GPIx register to represent the corresponding logic level (1 = high, 0 = low) appearing on signals GPI0 - GPI7, respectively, within 125 µs of signal transition. GPI7 is typically connected to the DAA ring detection circuitry, and bit RI in the interface memory represents a valid ring frequency if it is so connected.
GPOx	1B:0-7	1	**General Purpose Outputs.** Bits 0-7 in the GPOx register, set/reset by the host, are reflected by logic level outputs (1 = high, 0 = low) appearing on signals GPO0 - GPO7, respectively, within 125 µs of bit transition.
HDLC	07:0	0	**HDLC Mode.** When control bit HDLC is a 1 and the PDM bit is a 1, the modem performs HDLC framing in parallel data mode. When the HDLC bit is a 0 or the PDM bit is a 0, the modem does not perform HDLC framing. (See the SETUP bit.) In the voice mode (CONF = 90h), error correction is enabled (HDLC = 1) or disabled (HDLC = 0).
HPFEN	0D:2	0	**High Pass Filter Enable.** When control bit HPFEN is a 1, the Pre-AGC high pass filter is enabled in the receive path.
IO1	05:3	0	**Input/Output RAM 1 Select.** When control bit IO1 is a 1, ADD1 addresses IO RAM. When IO1 is a 0, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 13.)
IO2	15:3	0	**Input/Output RAM 2 Select.** When control bit IO2 is a 1, ADD2 addresses IO RAM. When IO2 is a 0, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 13.)
ITADRS	0A:0-4	0	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take effect. The address of the byte on which the modem asserts –IRQ1 on a bit or bits in that byte is:

Host Register (Hex)	ITADRS (Hex)	Host Register (Hex)	ITADRS (Hex)
00	00	10	08
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
ITBMSK	0B:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert -IRQ1 on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
MICLVL	0E:0-1	01	**Microphone Volume Level.** In speakerphone mode, The MICLVL bits control the SIA ADC signal gain as follows: Bit 1 / Bit 0 / Gain 0 / 0 / 0 dB 0 / 1 / 6 dB 1 / 0 / 9.5 dB 1 / 1 / 12 dB
MUTEP	0E:3	0	**Mute PIA ADC.** In speakerphone mode, control bit MUTEP enables (MUTEP = 1) or disables (MUTEP = 0) muting of the PIA ADC signal.
MUTES	0E:2	1	**Mute SIA ADC.** In speakerphone mode, control bit MUTES enables (MUTES = 1) or disables (MUTES = 0) muting of the SIA ADC signal.
NORM	14:0	1	**Normal Playback Speed.** When control bit NORM is a 1 and the FAST50, FAST33, and SLOW control bits are reset, normal playback speed is selected. NORM must be reset when another speed is selected.
OTS	1C:5	–	**On-Time Satisfied.** When configured as an DTMF receiver, the modem sets status bit OTS to 1 after the DTMF on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy the DTMF off-time criteria.
OTSC	17:5	0	**On-Time Satisfied Copy.** In DTMF modes, OTSC is a copy of the OTS bit for programmable interrupt control.
OVRUN	09:7	–	**Overrun/Underrun.** In HDLC mode, when configured as a transmitter and control bit AEOF is a 0, the modem sets status bit OVRUN to a 1 if a transmit underrun condition occurs. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL bits will be set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if B2A is a 0) or will transmit continuous flags. The modem will reset OVRUN every time it sets B2A. If AEOF is a 1, OVRUN is disabled. When configured as a receiver or in Caller ID mode, the modem sets the OVRUN bit to a 1 if a receive overrun condition occurs. To detect the next overrun condition, the host must reset this bit.
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being sent. The P1 sequence is an echo protection tone. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being sent. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PDEQZ	08:0	0	**Programmable Digital Equalizer.** When the host has configured the modem as a high speed receiver or transmitter and has set control bit PDEQZ, the programmable digital equalizer is enabled. When control bit PDEQZ is a 0, the programmable digital equalizer is disabled. The programmable digital equalizer defaults to a Japanese 2 link delay equalizer.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
PDM	07:5	0	**Parallel Data Mode.** When control bit PDM is a 1, parallel data mode is selected. If the modem is a transmitter, data for transmission is accepted from DBUFF (10:0-7). If the modem is a receiver, the modem provides received data to DBUFF (10:0-7) and to the RXD output pin. When the PDM bit is a 0, serial data mode is selected. If the modem is a transmitter, data for transmission is accepted from the TXD input pin. When the modem is a receiver, the modem provides the received data only to the RXD output pin.
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts ~IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIDR	05:5	0	**Programmable Interrupt at Data Rate.** When control bit PIDR is a 1, the programmable interrupt runs at the data rate. When PIDR is a 0, the programmable interrupt runs at the sample rate (9600 Hz). The PIDR bit is valid in all modes except tone, audio, and speakerphone.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts ~IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is a 0 (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on ~IRQ and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts ~IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert ~IRQ.
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is a 1, the receiver has detected the PN portion of the training sequence. When PNDET is a 0, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is a 1, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is a 0, a successful training has not occurred. PNSUC is still valid after the CDET bit is set to a 1.
PR	1D:5	–	**Rate Sequence Period.** When status bit PR is a 1 during transmit, the modem is sending the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being sent. When set to a 1 during receive, the modem is receiving the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being received. (V.17 or V.33 modes.)
PRDET	1D:4	–	**Rate Sequence Detection.** When status bit PRDET is a 1, the modem receiver has detected a rate sequence pattern containing a proper synchronization bit pattern. (V.17 or V.33 modes.)
RA	1A:0	0	**Relay A Active.** When control bit RA is a 1, the ~OH output is activated to close the normally open relay (off-hook); when RA is a 0, the ~OH is turned off to allow the normally open relay to open (on-hook). **Note:** The host has exclusive control of ~OH output through the RA bit. The delay between activation and actual toggling of the external control line will be two sample periods.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RB	1A:1	0	**Relay B Active.** When control bit RB is a 1, the ~TALK output is activated to open the normally closed relay (data); when RB is a 0, the ~TALK is turned off to allow the normally closed relay to close (talk). **Note:** The host has exclusive control of ~TALK output through the RB bit. The delay between activation and actual toggling of the external control line will be two sample periods.
RI	17:2	0	**Ring Indicator.** Status bit RI is set when a valid ringing signal is being detected. RI is reset when a valid ringing signal is not being detected. Ringing is selected if pulses are present on GPI7 input in the 15-68 Hz frequency range (default frequency range) for the 8000 Hz sampling rate modes. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time. The minimum and maximum valid ring frequencies are host programmable in DSP RAM. The RI bit is cleared to 0 when the RA bit = 1.
RMM	07:5	0	**Room Monitor.** In voice mode, setting both the CODECS and RMM bits enables the room monitor, which routes the SIA ADC signal to the PIA DAC.
RTSP	07:7	0	**Request To Send Parallel.** The one state of control bit RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset to a 0 (or ~RTS is turned off) and the turn-off sequence has been completed. RTSP parallels the operation of the ~RTS hardware input pin. These inputs are "ORed" by the modem.
RX	0D:7	–	**Receive State.** In high speed modes, the modem is in the receive state when status bit RX is a 1; the modem is in the transmit state when RX is a 0.
SBAD1L	02:0-7	–	**Single Bank RAM Address 1 LSB.** When control bits ACC1 and SBRAM1 are both a 1, SBAD1L contains the LSB of the address used to access the modem's single bank RAM via the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
SBAD1M	03:0-7	–	**Single Bank RAM Address 1 MSB.** When control bits ACC1 and SBRAM1 are both a 1, SBAD1M contains the MSB of the address used to access the modem's single bank RAM via the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
SBAD2L	12:0-7	–	**Single Bank RAM Address 2 LSB.** When control bits ACC2 and SBRAM2 are both a 1, SBAD2L contains the LSB of the address used to access the modem's single bank RAM via the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
SBAD2M	13:0-7	–	**Single Bank RAM Address 2 MSB.** When control bits ACC2 and SBRAM2 are both a 1, SBAD2M contains the MSB of the address used to access the modem's single bank RAM via the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
SBRAM1	1A:6	0	**Single Bank RAM Access 1.** When control bit SBRAM1 is a 1, the modem accesses the single bank RAM associated with the address in SBAD1M and SBAD1L (BR1, CR1, DR1, IO1, and AREX1 must be 0). WRT1 determines if a read or write is performed.
SBRAM2	1A:7	0	**Single Bank RAM Access 2.** When control bit SBRAM2 is a 1, the modem accesses the single bank RAM associated with the address in SBAD2M and SBAD2L (BR2, CR2, DR2, IO2, and AREX2 must be 0). WRT2 determines if a read or write is performed.
SCR1	0E:6	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1 = 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being sent. When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP must be set to a 1 by the host after the host writes a configuration code into the CONF bits (06:0-7) or changes any of bits 0 through 6 in register 07 (07:0-6). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change request is recognized.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SHPR	1D:7	0	**Short Train Rate Sequence.** When control bit SHPR is a 1, the V.17/V.33 rate sequence is included in the short training sequence, which extends the training by 64 bauds.
SHTR	07:4	0	**Short Train Mode.** When control bit SHTR is a 1 and CONF is 14h, 12h, 11h, 0Ah, or 09h, the modem will perform a short training sequence. A successful long train at the same data rate must precede its short train. A successful V.17 long train at any data rate must precede its short train. The setting of the SHTR bit must be followed by the setting of the SETUP bit. The EQSV bit must be set and the EQFZ bit may optionally be set for Short Train operation. (RFX144V12-S only.)
SLOW	14:1	0	**Slower by 50% Playback Speed.** When control bit SLOW is a 1 and the FAST50, FAST33, and NORM control bits are reset, 50% slower than normal playback speed is selected, i.e., playback time is 150% of normal playback time. SLOW must be reset when another speed is selected.
SP/HS	0E:4	1	**Speakerphone/Handset Switch.** In speakerphone mode, when control bit SP/HS is a 1, microphone/speaker operation is enabled; when SP/HS is a 0, handset in place of microphone/speaker is assumed for handset operation.
SQEXT	07:2	0	**Squelch Extend.** Control bit SQEXT determines the length of time the modem receiver is inhibited from receiving any signal after transmitter turn-off. The length of time is either 20 ms (SQEXT = 0) or 140 ms (SQEXT = 1).
TDIS	07:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when the ~RTS pin or RTSP bit is activated.
TONEPE	0F:6	0	**PIA Tone Enable.** In speakerphone mode, control bit TONEPE enables (TONEPE = 1) or disables (TONEPE = 0) tone to the PIA DAC while in tone transmit mode (TTONEE = 1).
TONESE	0F:5	0	**SIA Tone Enable.** In speakerphone mode, control bit TONESE enables (TONESE = 1) or disables (TONESE = 0) tone to the SIA DAC while in tone transmit mode (TTONEE = 1).
TTONEE	0E:7	0	**Tone Transmit Enable.** In speakerphone mode, control bit TTONEE enables (TTONEE = 1) or disables (TTONEE = 0) tone transmit mode. Depending upon the status of TONEPE and TONESE, the corresponding voice channel will be muted for the whole period of the tone transmit mode. TTONEE must be reset in order to re-activate voice channel.
TRIG	0A:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE bit = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC level triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **Bit 7 / Bit 6 / Description** 0 / 0 / DC Level Triggered 0 / 1 / Positive Edge Triggered 1 / 0 / Negative Edge Triggered 1 / 1 / Edge Triggered
VOLDWN	0E:5	0	**Volume Down.** In speakerphone mode, the volume control to the SIA DAC is decreased by 2 dB each time the VOLDWN bit is set. The VOLDWN bit is automatically reset by the modem.
VOLUP	0E:6	0	**Volume Up.** In speakerphone mode, the volume control to the SIA DAC is increased by 2 dB each time control bit VOLUP is set. The VOLUP bit is automatically reset by the modem.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
VOVUN	17:0	0	**Voice Overrun or Underrun.** In voice mode, status bit VOVUN is set when the host fails to access the DBUFF input or output before new data is needed or available. VOVUN is reset when the voice coder/decoder data buffer is available for proper data transfer. An overrun condition in the voice coder suspends recording of new samples until the host reads DBUFF. An underrun condition in the voice decoder suspends playback of data until the host writes DBUFF samples.
VOX	17:3	0	**Voice Detected.** In voice mode, status bit VOX is set when the voice coder is detecting speech and is reset when the voice coder is not detecting speech.
VOXREC	1A:3	0	**Voice Activated Recording.** In voice mode, when control bit VOXREC is a 1 and CDEN is a 1, message encoding is delayed until status bit VOX is set (thus eliminating encoding of beginning message silence). Voice activated recording provides maximum RAM storage efficiency. When VOXREC is a 0, message encoding is not delayed.
WRT1	05:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by AREX1, ADD1, and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by AREX1, ADD1, and CR1, and stores the data into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is a 1 and ACC2 is a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by AREX2, ADD2, and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is a 1, the modem reads data from its internal RAM from the locations addressed by AREX2, ADD2, and CR2, and stores the data into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the LSB of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the LSB of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the LSB of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the LSB of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the MSB of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the MSB of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** In HDLC mode, when control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is a 0, ZEROC is disabled.

Table 13a. Modem DSP RAM Access Codes

No.[1]	Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.[4]
1a	Received Signal Sample (Pre-AGC and Pre-Optional High Pass Filter)	0	0	1	0	0	55	2,3
1b	Received Signal Sample (Post-AGC)	0	0	0	0	0	15	2,3
2	Received Signal Sample - 8-bit Audio Mode (Post-AGC)	0	0	0	0	0	A0	0
3	Average Energy	0	0	0	0	0	14	2,3
4	AGC Gain Word	0	0	1	0	0	15	2,3
5	AGC Slew Rate Word	0	0	0	0	0	95	0,1
6	PIA Tone 1 Frequency	0	0	1	0	0	21	2,3
	SIA Tone 1 Frequency	0	0	1	0	0	1A	2,3
7	PIA Tone 1 Transmit Output Level	0	0	0	0	0	22	2,3
	SIA Tone 1 Transmit Output Level	0	0	0	0	0	1B	2,3
8	PIA Tone 2 Frequency	0	0	1	0	0	22	2,3
	SIA Tone 2 Frequency	0	0	1	0	0	1B	2,3
9	PIA Tone 2 Transmit Output Level	0	0	0	0	0	23	2,3
	SIA Tone 2 Transmit Output Level	0	0	0	0	0	1C	2,3
10	Transmit Output Level/Scaling	0	0	0	0	0	21	2,3
11	Equalizer Tap Coefficients	0	1	1	0	1	50 - 7F	0,1,2,3
12	Rotated Equalizer Output, Eye Pattern	0	1	1	0	0	17	0,1,2,3
13	Decision Points, Ideal	0	1	0	0	0	17	0,1,2,3
14	Error Vector	0	1	1	0	0	1D	0,1,2,3
15	Rotation Angle	0	1	1	0	0	8C	0,1
16	Frequency Correction	0	1	1	0	0	18	2,3
17	Eye Quality Monitor (EQM), Hard Decision	0	1	1	0	0	0D	2,3
18	Eye Quality Monitor (EQM), TCM Min. Metric[3]	0	1	1	0	0	B8	0,1
19	RLSD Turn-on Threshold	0	0	1	0	0	37	2,3
20	RLSD Turn-off Threshold	0	0	1	0	0	B7	0,1
21	Receiver Sensitivity, MAXG	0	0	1	0	0	24	2,3
29	Minimum On Time (DTMF)	0	0	1	0	0	1F	2,3
30	Minimum Off Time (DTMF)	0	0	0	0	0	1F	2,3
31	Minimum Cycle Time (DTMF)	0	0	0	0	0	9F	0,1
32	Maximum Dropout Time (DTMF)	0	0	1	0	0	9F	0,1
33	Maximum Speech Energy (DTMF)	0	0	1	0	0	1E	2,3
34	Frequency Deviation, Low Group (DTMF)	0	0	0	0	0	1D	2,3
35	Frequency Deviation, High Group (DTMF)	0	0	1	0	0	1D	2,3
36	Negative Twist Control (DTMF)	0	0	0	0	0	1E	2,3
37	Positive Twist Control (DTMF)	0	0	0	0	0	9E	0,1
38	Maximum Energy Hit Time (DTMF)	0	0	1	0	0	A3	0,1
39	Number of Additional Flags, NFLAG (HDLC)	0	0	1	0	0	85	0,1
40	Transmitter Rate Sequence Pattern	0	0	0	0	0	6B	2,3
41	Receiver Rate Sequence Pattern	0	0	1	0	0	9A	0,1
42	FR1 Tone Detector Coefficients	0	0	1	0	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	0	1	0	0	A5-AA	0,1
43	FR2 Tone Detector Coefficients	0	0	1	0	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	0	1	0	0	AB-B0	0,1
44	FR3 Tone Detector Coefficients	0	0	1	0	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	0	1	0	0	B1-B6	0,1
47	Tone Detector Threshold	0	0	0	0	0	9D	0,1
48	Maximum Samples per Ring Frequency Period	0	0	0	0	0	53	2,3
49	Minimum Samples per Ring Frequency Period	0	0	0	0	0	52	2,3
50	Sleep Mode Enable	0	0	0	1	0	3E	0,1

Table 13a. Modem DSP RAM Access Codes (Cont'd)

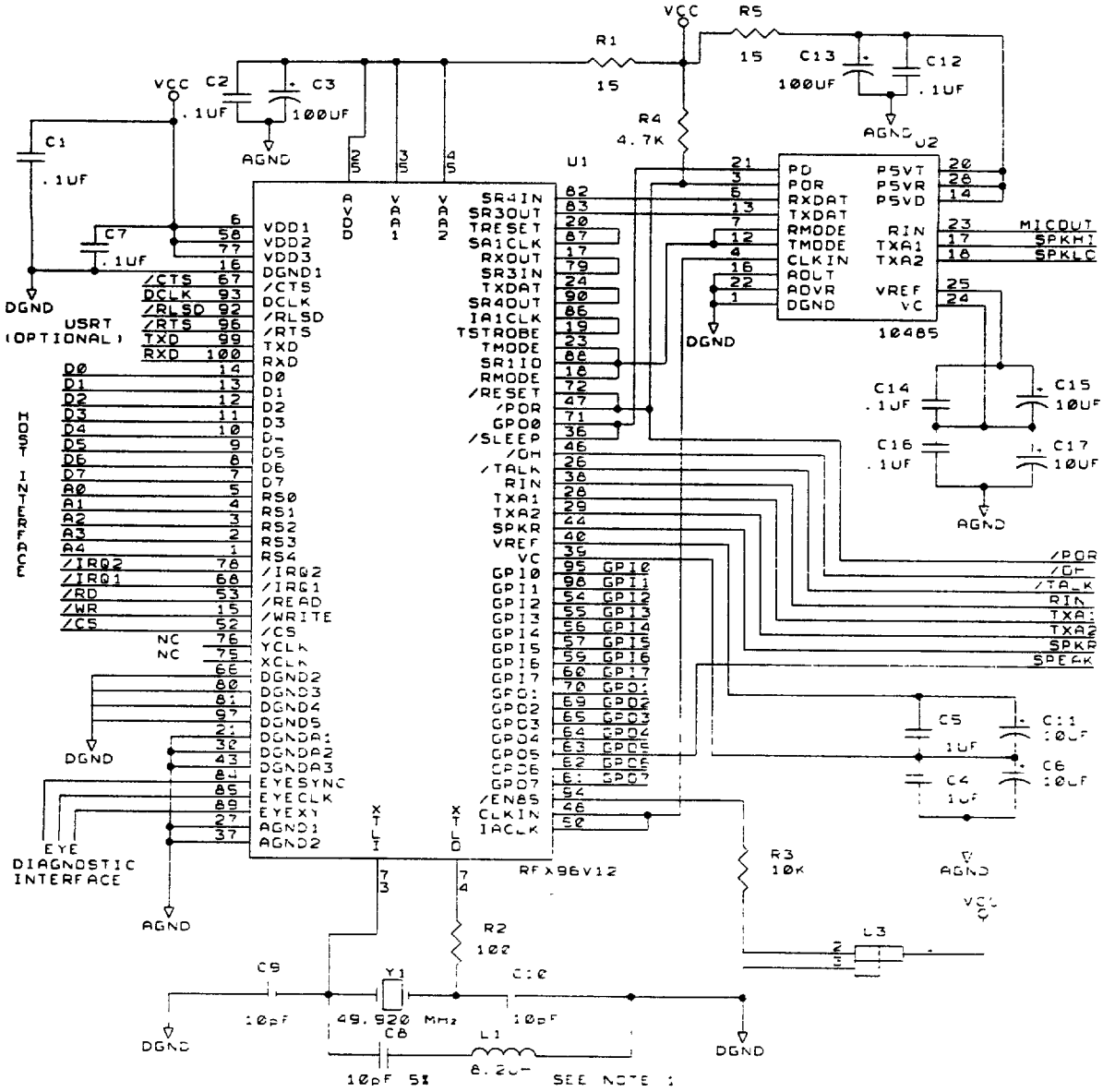
No.[1]	Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.[4]
51	Voice mode VOX Turn-On Threshold	0	0	1	0	0	57	2,3
52	Voice mode VOX Turn-Off Threshold	0	0	1	0	0	D7	0,1
53	Voice mode VOX A0 Filter Coefficient	0	0	1	0	0	D6	0,1
54	Voice mode VOX A1 Filter Coefficient	0	0	1	0	0	56	2,3
55	Voice mode AGC Energy Reference Level	0	0	0	0	0	9A	0,1
56	Voice mode AGC Slew Rate	0	0	1	0	0	1A	2,3
57	Voice mode AGC Gain Adaptation Threshold	0	0	0	0	0	1A	2,3
58	Voice mode AGC Maximum Gain	0	0	0	0	0	9B	0,1
59	Voice mode AGC Gain Word	0	0	1	0	0	1B	2,3
60	Voice mode Data Transfer Interrupt Interval	0	0	1	0	0	03	2,3
61	Speaker Volume Control (SPKR output pin)	0	0	0	1	0	1C	0,1
62	Speakerphone Room Monitor Volume Control	0	0	1	0	0	85	0,1
63	Speakerphone Transmit Speech Active (1 = Transmit speech active; 0 = Transmit speech inactive)	0	0	0	1	0	1E	0: 7
64	Speakerphone Receive Speech Active (1 = Receive speech active; 0 = Receive speech inactive)	0	0	0	1	0	1E	0:6

Notes:
1. Parameter numbers refer to corresponding numbers in Section 4 of the RFX96V12-S and RFX144V12-S Modem Designer's Guide (Order No. 1045).
2. For all accesses, DRx = 0.
3. RFX144V12-S only.
4. Read Reg. No. column only shows the registers to use when x = 1. When x = 2, the Read Reg. No. column value must be added to 10h.

Table 13b. Modem DSP RAM Access Codes - SBRAM

No.[1]	Function	SBRAMx	BRx	CRx	IOx	AREXx	SBADxM	SBADxL	Read Reg. No.[4]
65	Speakerphone Line Echo Suppressor	1	0	0	0	0	04	25	0,1
66	Speakerphone Transmit AGC Reference Level	1	0	0	0	0	04	36	0,1
67	Speakerphone Transmit AGC Slew Rate	1	0	0	0	0	04	47	0,1
68	Speakerphone Receive AGC Reference Level	1	0	0	0	0	04	51	0,1
69	Speakerphone Receive AGC Slew Rate	1	0	0	0	0	04	62	0,1
70	Speakerphone Transmit Speech Hangover	1	0	0	0	0	04	79	0,1
71	Speakerphone Receive Speech Hangover	1	0	0	0	0	04	88	0,1

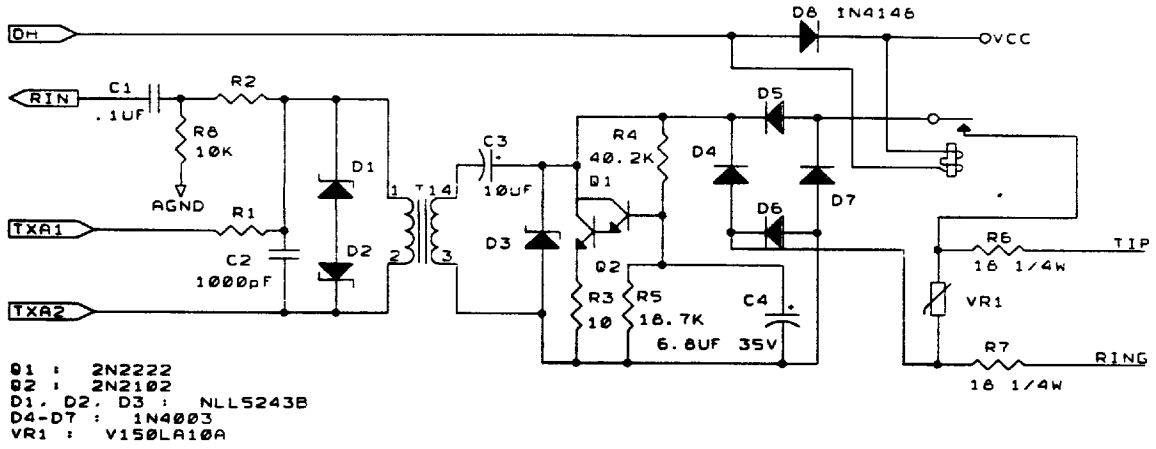
Notes:
1. Parameter numbers refer to corresponding numbers in Section 4 of the RFX96V12-S and RFX144V12-S Modem Designer's Guide (Order No. 1045).
2. For all accesses, DRx = 0.
3. RFX144V12-S only.
4. Read Reg. No. column only shows the registers to use when x = 1. When x = 2, the Read Reg. No. column value must be added to 10h.



NOTES:

1. THIRD OVERTONE CRYSTAL CONNECTION.
2. PINS 41, 42, 49, 51 ARE NO CONNECTS ON L1.
3. PINS 2, 5, 6, 9, 10, 11, 15, 19, 26 AND 27 ARE NO CONNECTS ON U2.

Figure 5. Recommended Modem/Speakerphone Interface Circuit



NOTES:
1. CHOOSE R1 VALUE TO OBTAIN 600 OHM INTERNAL IMPEDANCE.
2. CHOOSE R2 VALUE TO OBTAIN A 6DB LOSS FROM TIP AND RING TO RIN.
3. THIS CIRCUIT PROVIDES A MAXIMUM OUTPUT LEVEL OF -13 dBm.
4. SEE 'TYPICAL INTERFACE TO EXTERNAL HYBRID' FOR SPEAKERPHONE APPLICATION

Figure 6. Typical Line Interface Circuit

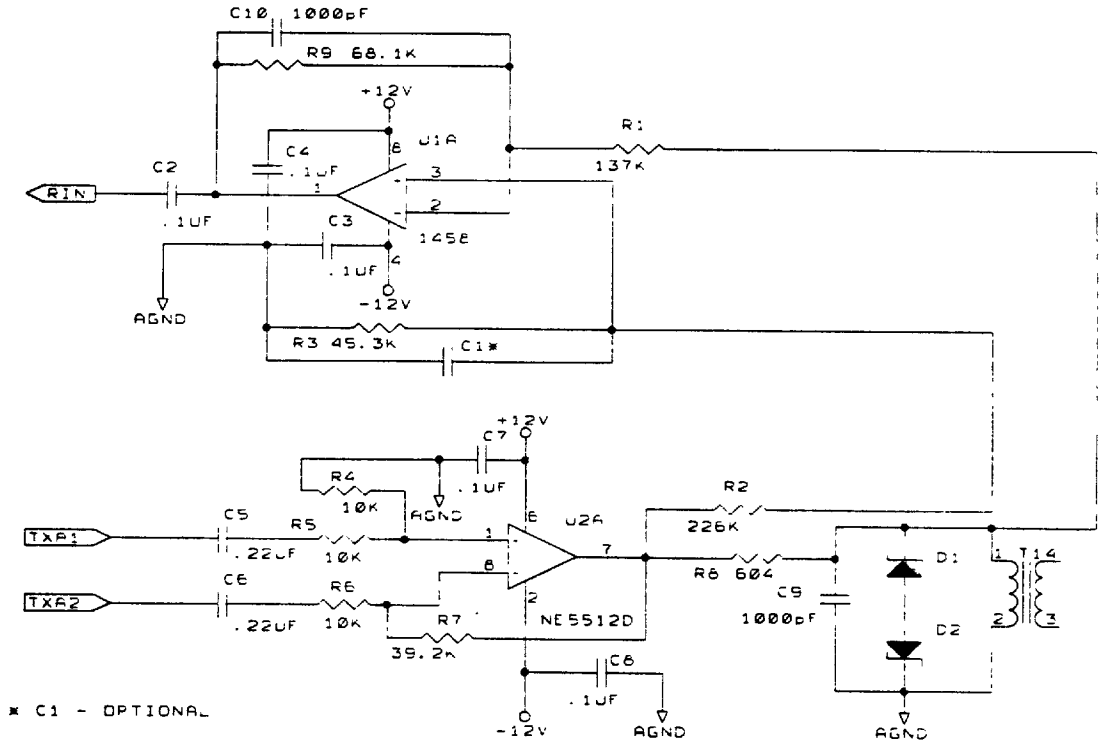
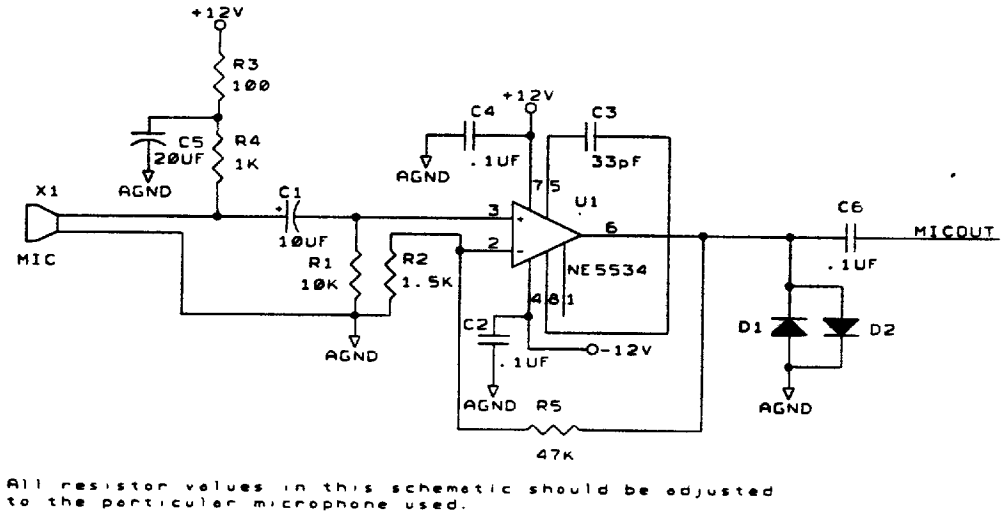


Figure 7. Typical Interface to External Hybrid



All resistor values in this schematic should be adjusted to the particular microphone used.

Figure 8. Typical Microphone Circuit

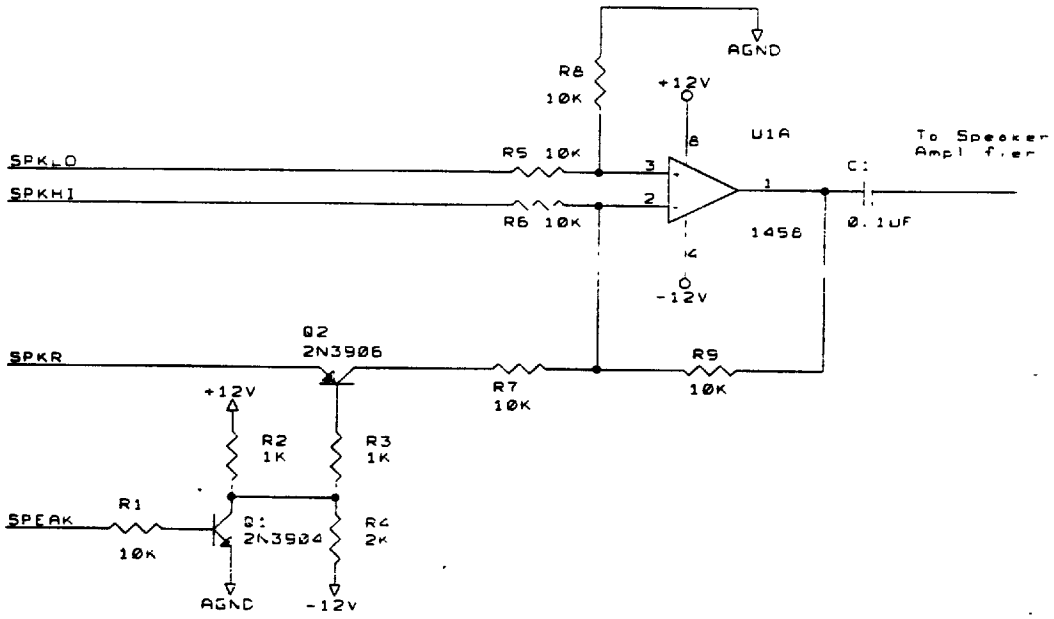
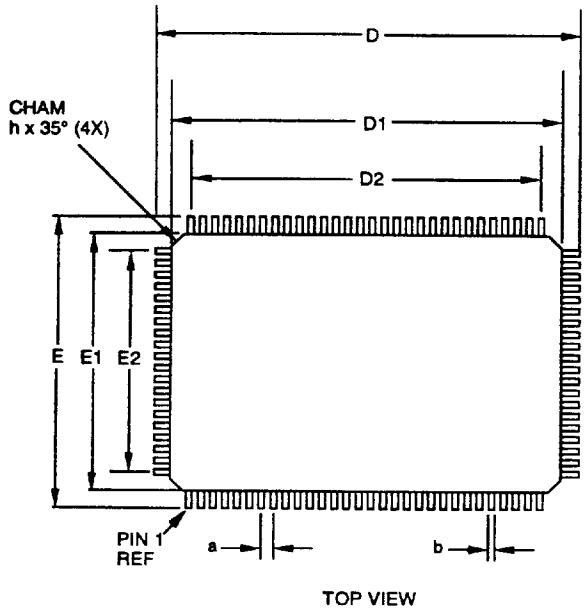


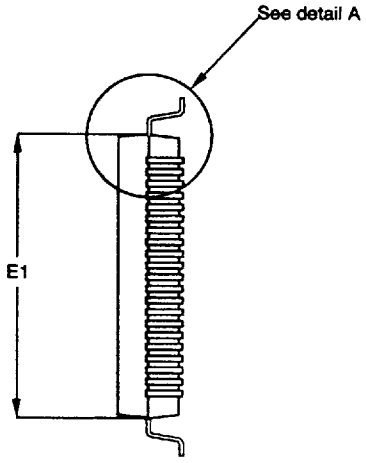
Figure 9. Typical Speaker Circuit

PACKAGE DIMENSIONS

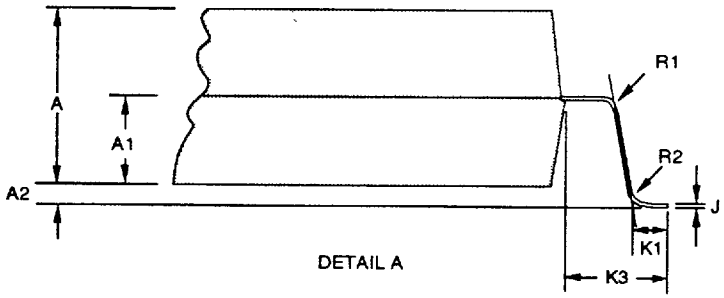
Package dimensions are shown in Figure 10.



TOP VIEW



SIDE VIEW



DETAIL A

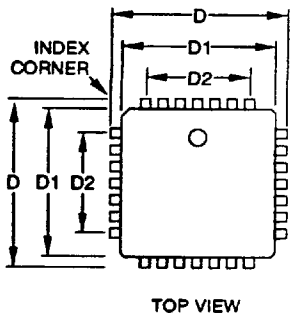
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.95	2.05	0.077	0.081
A1	0.95	1.05	0.037	0.041
A2	0.25 REF		0.0098	
D	23.05	23.35	0.907	0.919
D1	19.95	20.05	0.785	0.789
D2	18.85 REF		0.7421	
E	17.05	17.35	0.671	0.683
E1	13.95	14.05	0.549	0.553
E2	12.35 REF		0.4862	
K1	0.70	0.90	0.028	0.035
K3	1.60 REF		0.0630	
R1	0.23	---	0.009	---
R2	0.15	0.25	0.006	0.010
a	0.65 REF		0.0256	
b	0.30 REF		0.0118	
h	--	0.50	--	0.020
J	0.1524 REF		0.0060	

Ref. GP00-D234-5/92 (091393)

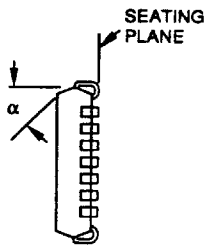
Note: * Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors

PD-PQFP-100

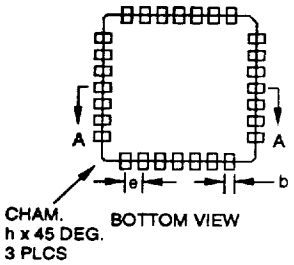
Figure 10a. 100-Pin PQFP Dimensions



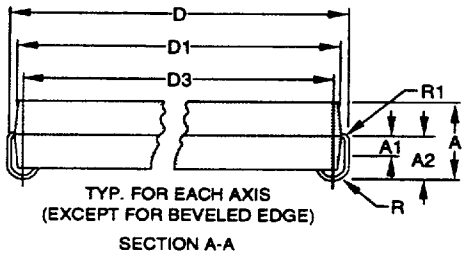
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SECTION A-A

Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	12.37	12.52	0.487	0.493
D1	11.38	11.48	0.448	0.452
D2	7.62 REF		0.300 REF	
D3	10.67 REF		0.420 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
Ref: GP00-D169				

PD-PLCC-28

Figure 10b. 28-Pin PLCC Dimensions