CY101E484
CY10E484
CY100E484

ADVANCED INFORMATION

CYPRESS SEMICONDUCTOR

4096 x 4 ECL Static RAM

Features

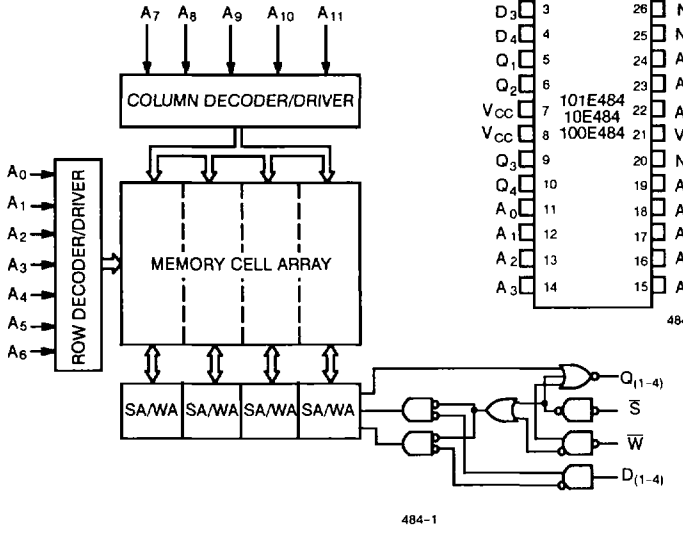
- **4096 x 4-bit organization**
- **Ultra high speed/standard power**
  - t_{AA} = 7 ns
  - I_{EE} = TBD mA
- **Low-power version**
  - t_{AA} = 7, 10 ns
  - I_{EE} = 200 mA
- **Both 10KH/10K- and 100K-compatible I/O versions**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

The Cypress CY101E484, CY10E484, and CY100E484 are 4K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These parts are fully decoded random access memories organized as 4096 words by 4 bits. The CY10E484 is 10KH/10K compatible. The CY100E484 is 100K compatible, and the CY101E484 is 100K compatible with a -5.2V supply.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, $\overline{W}$ is held HIGH while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory. The devices are packaged in 28-pin cerDIPs, PLCCs, and rectangular cerpacks in the high-performance center power-ground version pin configurations.

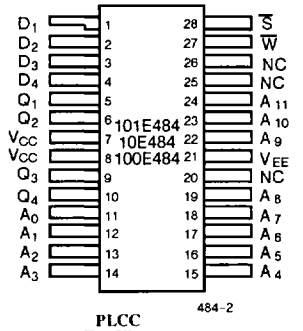
Logic Block Diagram



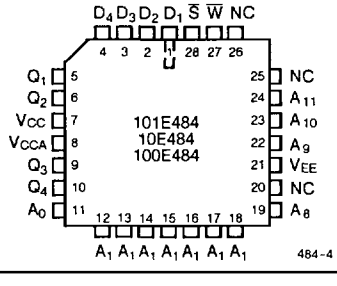
Pin Configurations

CerDIP
Top View

Rectangular Cerpak
Top View



PLCC
Top View



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Selection Guide

		101E484-7 10E484-7 100E484-7	101E484-10 10E484-10 100E484-10
Maximum Access Time (ns)		7	10
I_{EE} Max. (mA)	Commercial	TBD	
	L	200	200

Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write H
L	L	L	L	Write L
L	H	X	D_{OUT}	Read

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