1, 2, 4, 8M x 32
5 V, FPM, Unbuffered

DRAM Single-In-Line Memory Module (SIMM)
4, 8, 16, and 32 Megabyte

- JEDEC–Standard 72–Lead Single–In–Line Memory Module (SIMM)
- Single 5 V Power Supply, TTL–Compatible Inputs and Outputs
- Fast Page Mode (FPM)
- $\overline{RAS}$–Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
- 4MB/8MB: 1024 Cycle Refresh: 16 ms
- 16MB/32MB: 2048 Cycle Refresh: 32 ms

PART NUMBERS (See Page 19 for Definitions and 1997 Replacements)

Organization	60	70
1M x 32	MCM32B116S60 MCM32B116SG60 MCM32BT116SH60 MCM32BT116SHG60	MCM32B116S70 MCM32B116SG70 MCM32BT116SH70 MCM32BT116SHG70
2M x 32	MCM32B216S60 MCM32B216SG60 MCM32BT216SH60 MCM32BT216SHG60	MCM32B216S70 MCM32B216SG70 MCM32BT216SH70 MCM32BT216SHG70
4M x 32	MCM32C400ASH60 MCM32C400ASHG60 MCM32CT400ASH60 MCM32CT400ASHG60	MCM32C400ASH70 MCM32C400ASHG70 MCM32CT400ASH70 MCM32CT400ASHG70
8M x 32	MCM32C800ASH60 MCM32C800ASHG60 MCM32CT800ASH60 MCM32CT800ASHG60	MCM32C800ASH70 MCM32C800ASHG70 MCM32CT800ASH70 MCM32CT800ASHG70

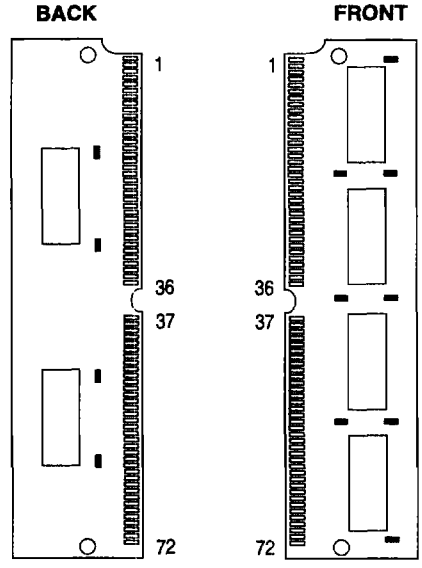
KEY TIMING PARAMETERS

Speed	t_{RC} (ns)	t_{RAC} (ns)	t_{CAC} (ns)	t_{AA} (ns)	t_{PC} (ns)
60	110	60	15	30	40
70	130	70	20	35	45

ADDITIONAL PARAMETERS

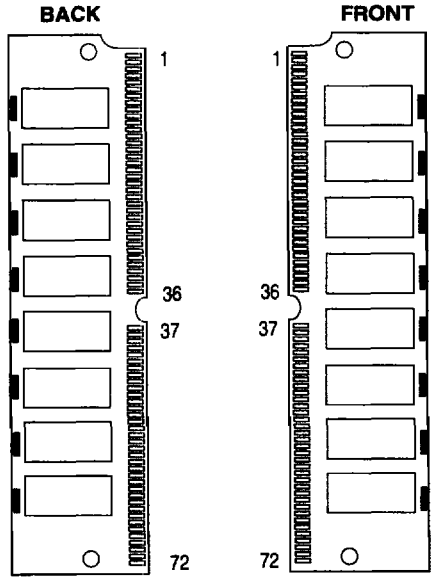
Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation (mW) (Max)	
			TTL	CMOS
4MB	60	2,035	22	11
	70	1,705		
8MB	60	2,057	44	22
	70	1,727		
16MB	60	4,840	88	44
	70	4,180		
32MB	60	4,928	176	88
	70	4,268		

1M x 32 (4MB), 2M x 32 (8MB)
72–LEAD LOW HEIGHT SIMM



Organization	Comp. Pkg.	Case	Components	
			Front	Back
1M x 32 (4MB)	TSOP	866H–01	2	0
	SOJ	866A–02	2	0
2M x 32 (8MB)	TSOP	866H–01	4	0
	SOJ	866A–02	2	2

4M x 32 (16MB), 8M x 32 (32MB)
72–LEAD LOW HEIGHT SIMM
CASE 866–02 (SOJ),
CASE 866H–01 (TSOP)



BACK NOT POPULATED ON 4M x 32 (16MB)

MOTOROLA

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	A10*	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{RAS3}$*	45	$\overline{RAS1}$*	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

* A10 is NC on the 4MB and 8MB. $\overline{RAS1}$ and $\overline{RAS3}$ are NC on the 4MB and 16MB.

PIN NAMES

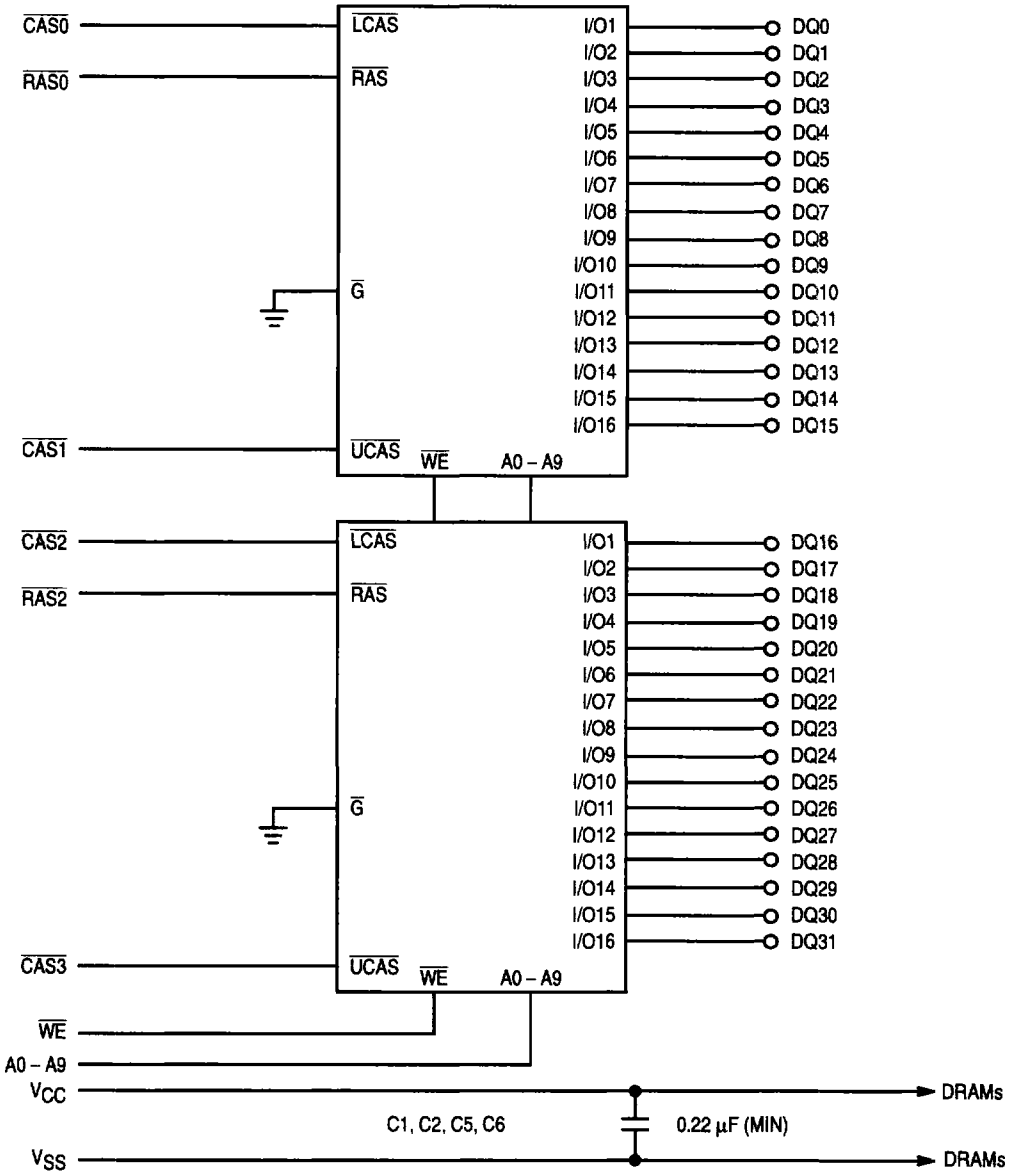
A0 – A10 ..... Address Inputs	DQ0 – DQ31 ..... Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$ .. Column Address Strobe	PD1 – PD4 ..... Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$ ..... Row Address Strobe	$\overline{W}$ ..... Write Enable
V_{CC} ..... Power	V_{SS} ..... Ground
NC ..... No Connection	

All power supply and ground pins must be connected for proper operation of the device.

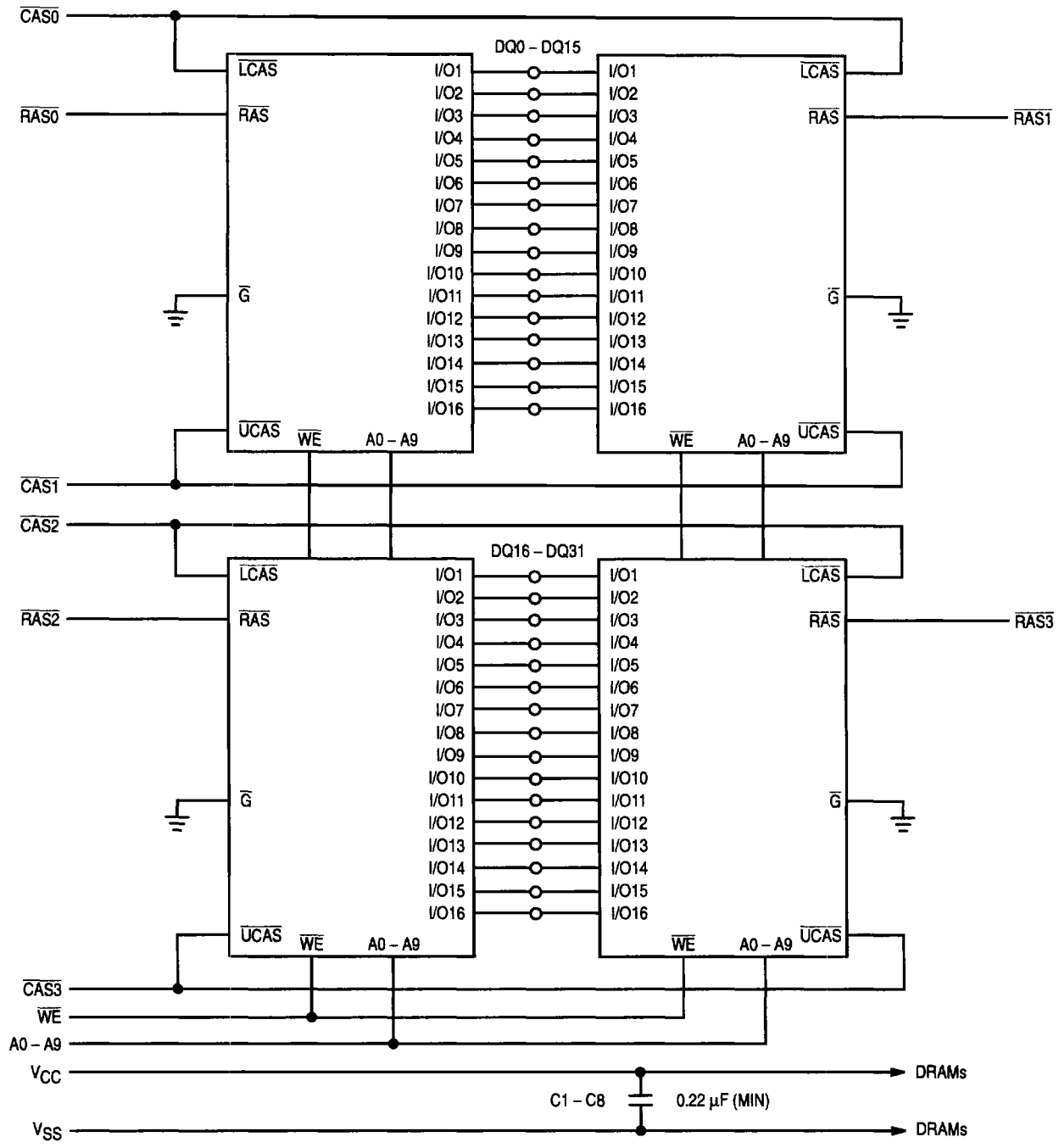
PRESENCE DETECT

Pin Names	Speed	4MB	8MB	16MB	32MB
PD1		V_{SS}	NC	V_{SS}	NC
PD2		V_{SS}	NC	NC	V_{SS}
PD3	60	NC	NC	NC	NC
	70	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD4	60	NC	NC	NC	NC
	70	NC	NC	NC	NC

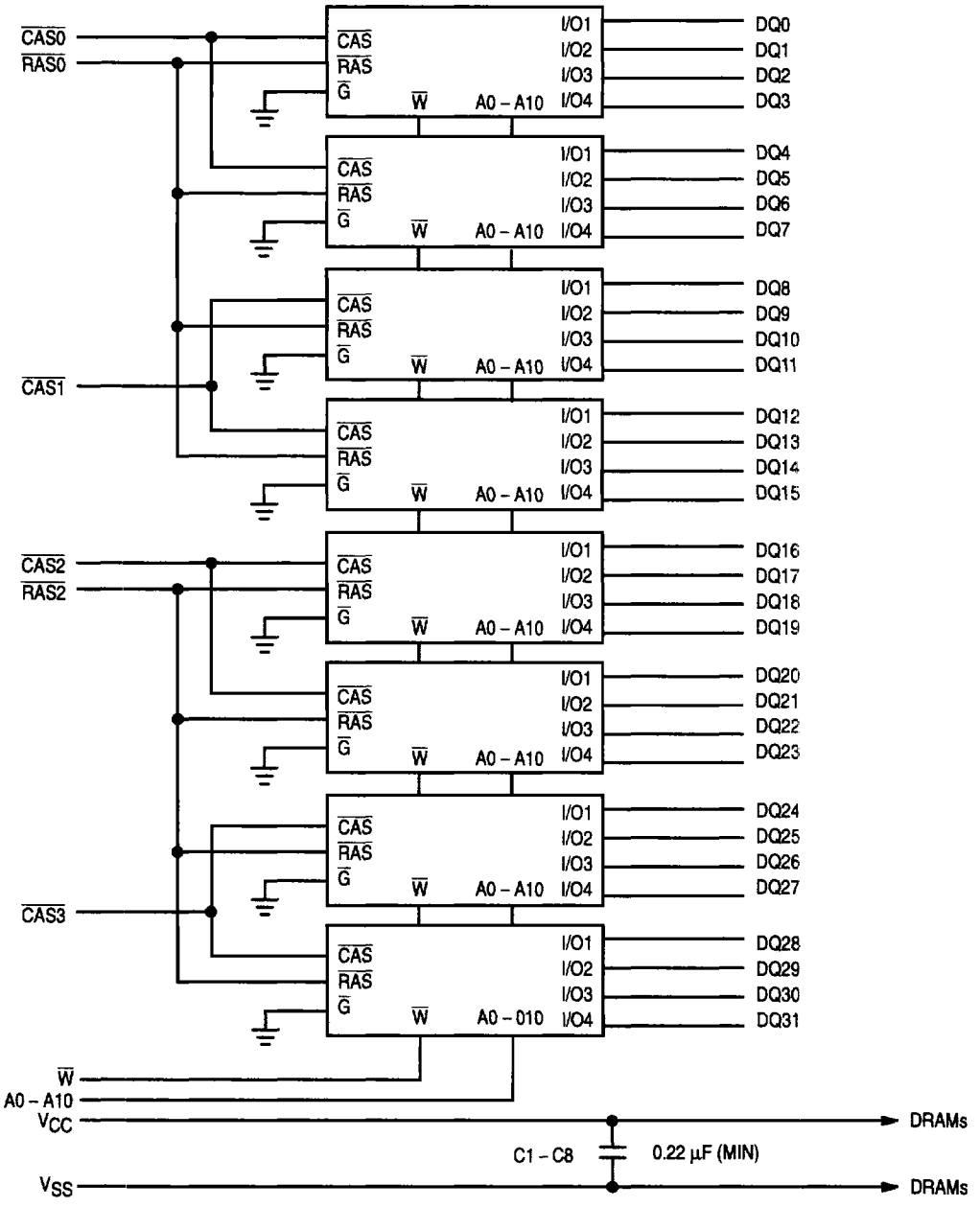
4MB BLOCK DIAGRAM



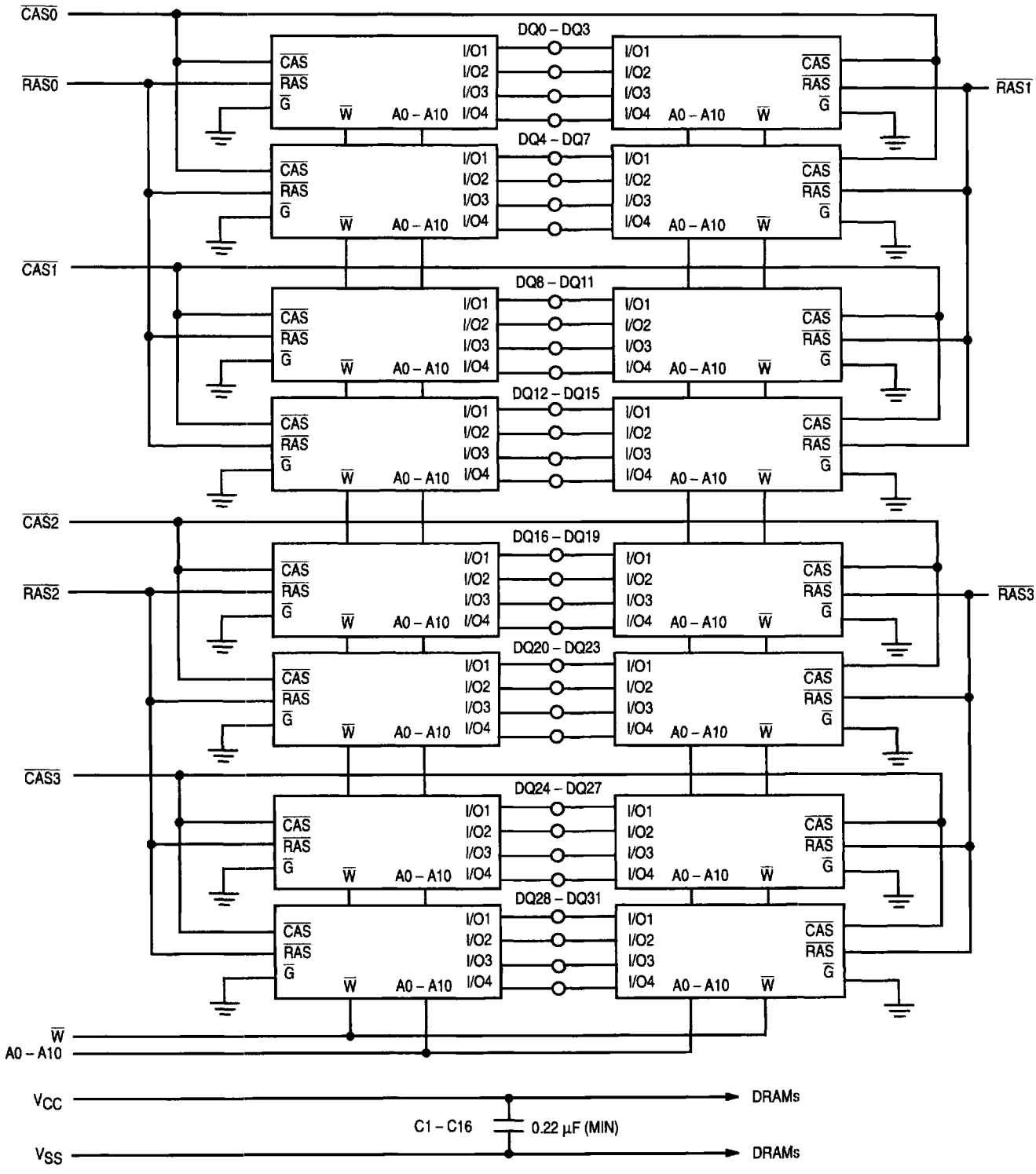
8MB BLOCK DIAGRAM



16MB BLOCK DIAGRAM



32MB BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} (for Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC}+ 0.5	V
Data Output Current per DQ pin	I_{out}	50	mA
Power Dissipation 4MB/8MB 16MB/32MB	P_D	2.6/5.2 7.2/14.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(i)}$	–160	—	+ 160	µA
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(o)}$	–20	—	+ 20	µA
Output High Voltage (I_{OH} = –2 mA)	V_{OH}	2.4	—	—	V
Output High Voltage (I_{OL} = 2 mA)	V_{OL}	—	—	0.4	V

* – 2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages Referenced to V_{SS})

Characteristic		Symbol	4MB		8MB		16MB		32MB		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	60	I_{CC1}	—	370	—	374	—	880	—	896	mA	1, 2
	70		—	310	—	314	—	760	—	776		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	4	—	8	—	16	—	32	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles (t_{RC} = t_{RC} Min)	60	I_{CC3}	—	370	—	374	—	880	—	896	mA	1, 2
	70		—	310	—	314	—	760	—	776		
V_{CC} Power Supply Current During FPM Cycle (t_{PC} = t_{PC} Min)	60	I_{CC4}	—	180	—	184	—	560	—	576	mA	1, 2
	70		—	160	—	164	—	480	—	496		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	2	—	4	—	8	—	16	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = t_{RC} Min)	60	I_{CC6}	—	370	—	374	—	880	—	896	mA	1
	70		—	310	—	314	—	760	—	776		

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	4MB Max	8MB Max	16MB Max	32MB Max	Unit
Addresses	C_{in}	20	30	50	90	pF
$\overline{WE}$	C_{in}	24	38	66	122	pF
$\overline{RAS}$	C_{in}	17	17	38	38	pF
$\overline{CAS}$	C_{in}	17	24	24	38	pF
DQ	C_{out}	17	24	17	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

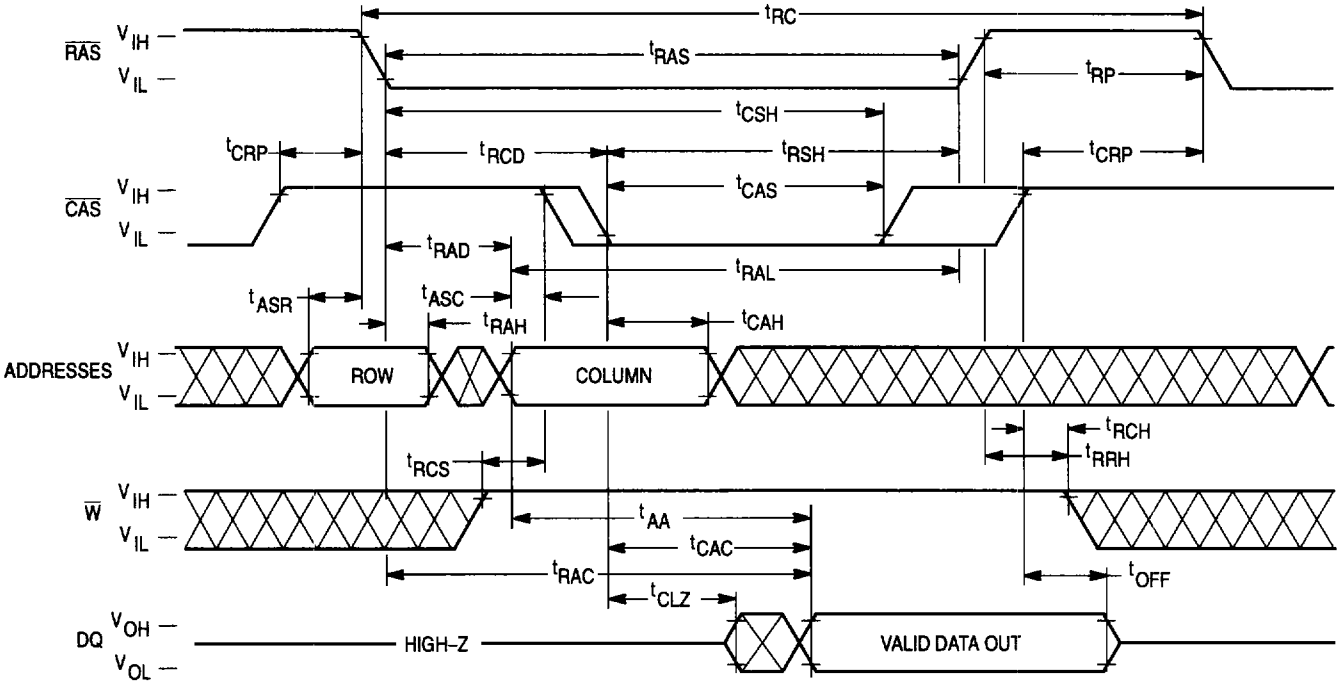
READ AND WRITE CYCLES (continued)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	14
Refresh Period 4MB/8MB 16MB/32MB	t_{RVRV}	t_{RFSH}	—	16 32	—	16 32	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	

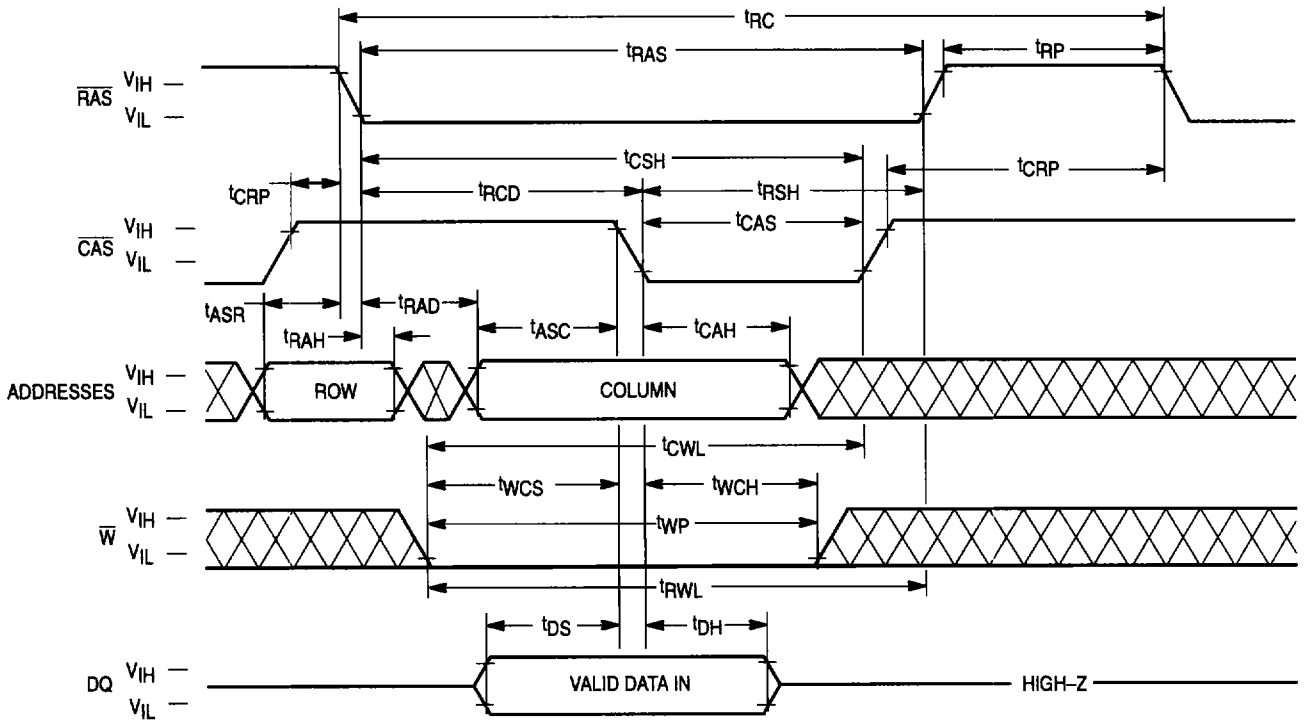
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

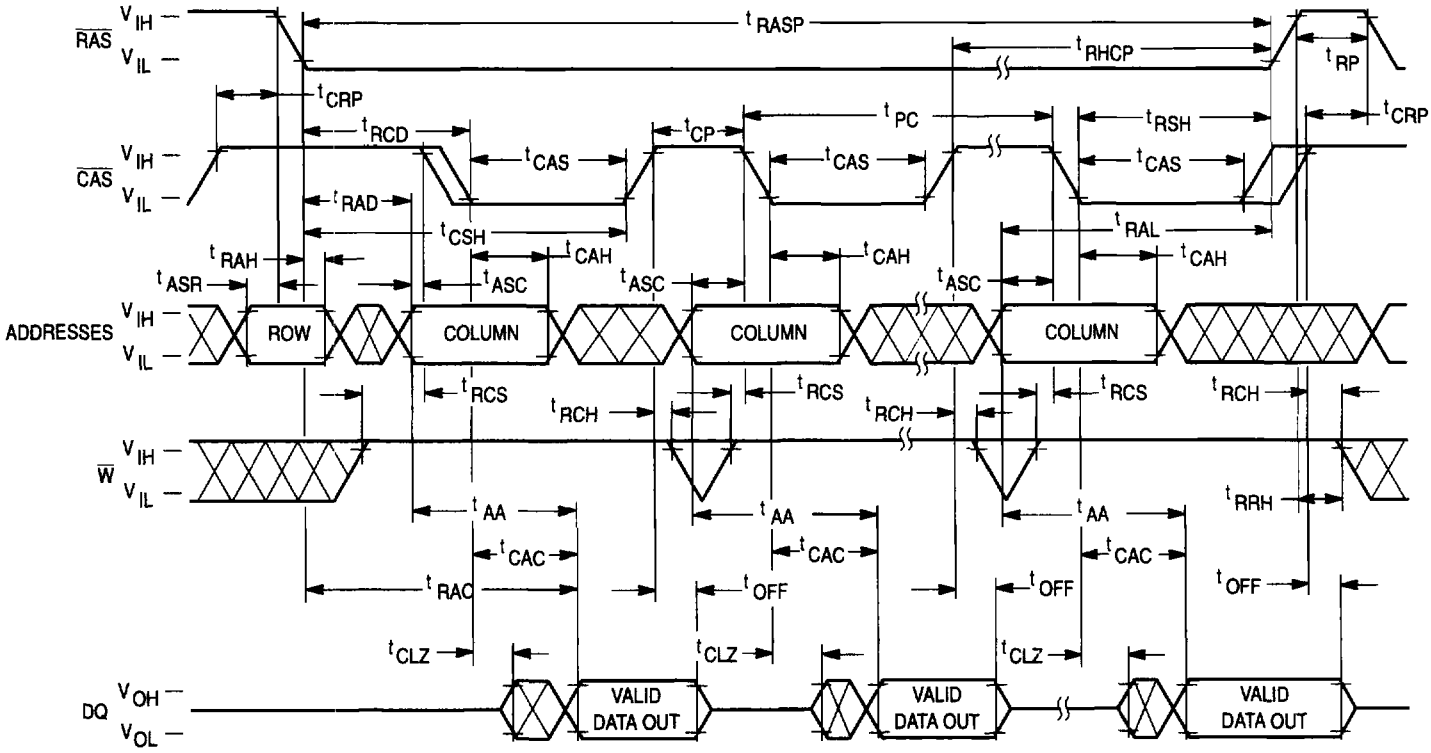
READ CYCLE



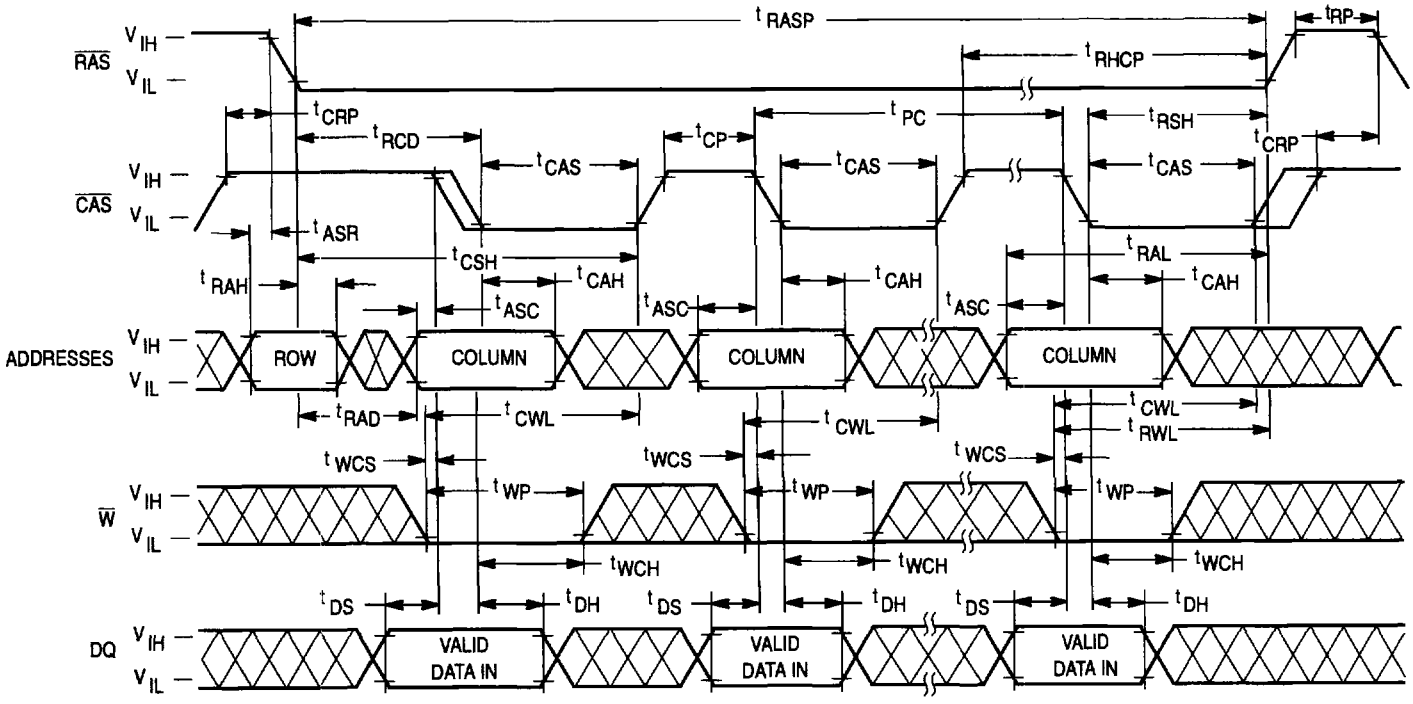
WRITE CYCLE



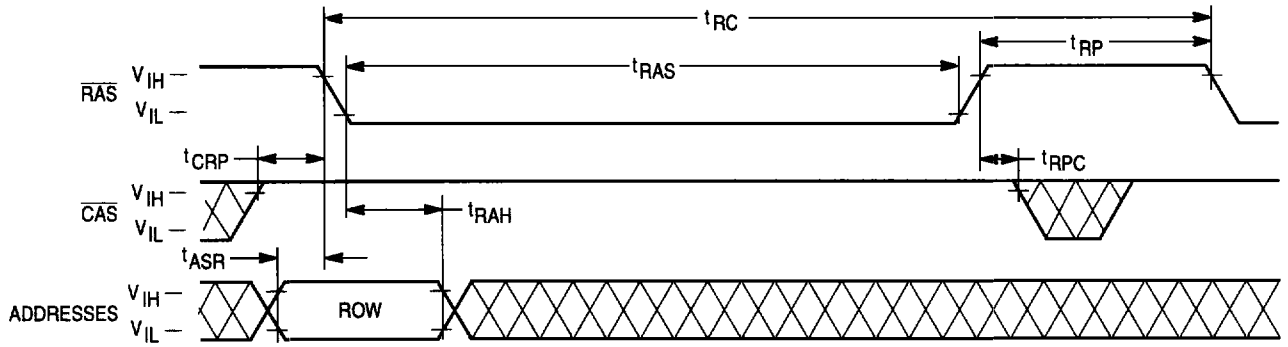
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE

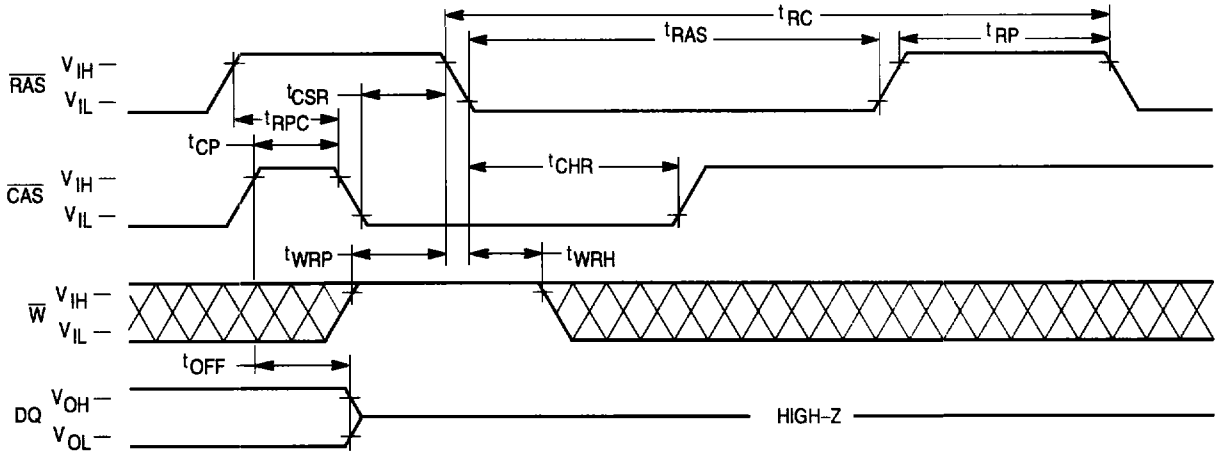


$\overline{RAS}$–ONLY REFRESH CYCLE



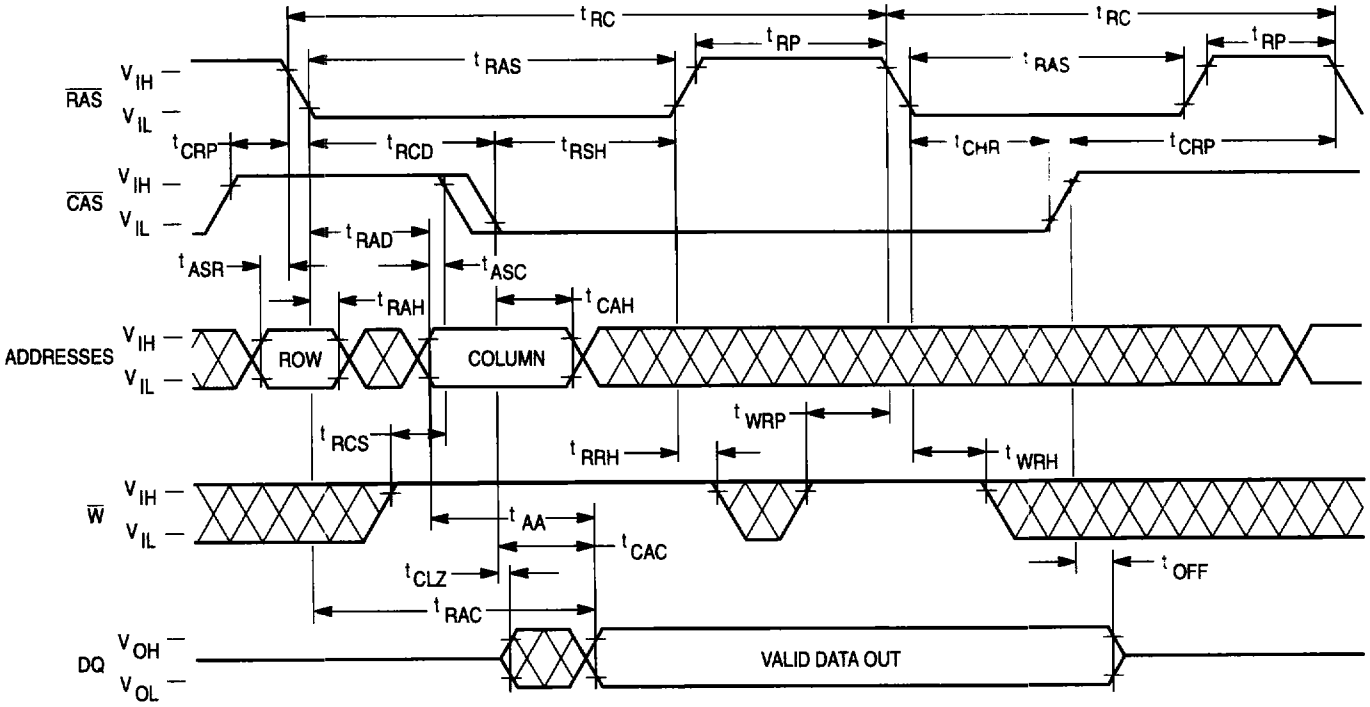
NOTE: $\overline{W}$ = H or L
DQ = Open

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

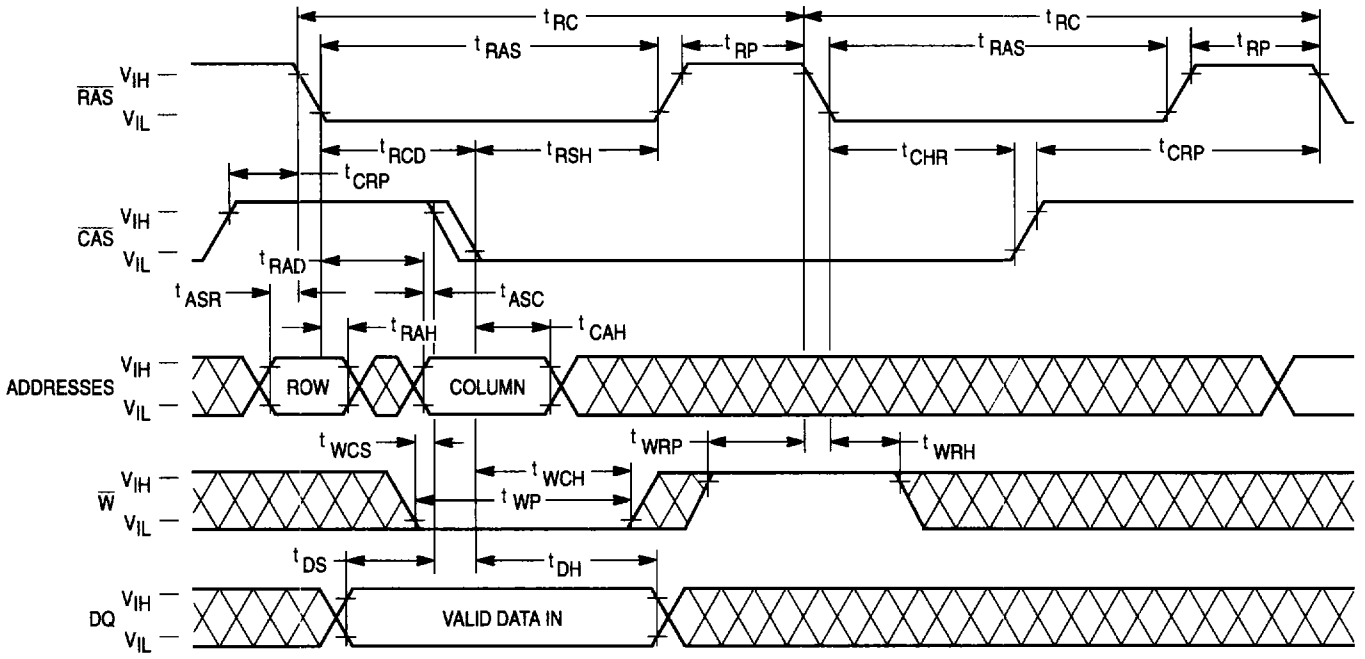


NOTE: Addresses = H or L
4MB, 8MB: $\overline{W}$ = H or L
16MB, 32MB: $\overline{W}$ must be as shown to avoid switching into component test mode

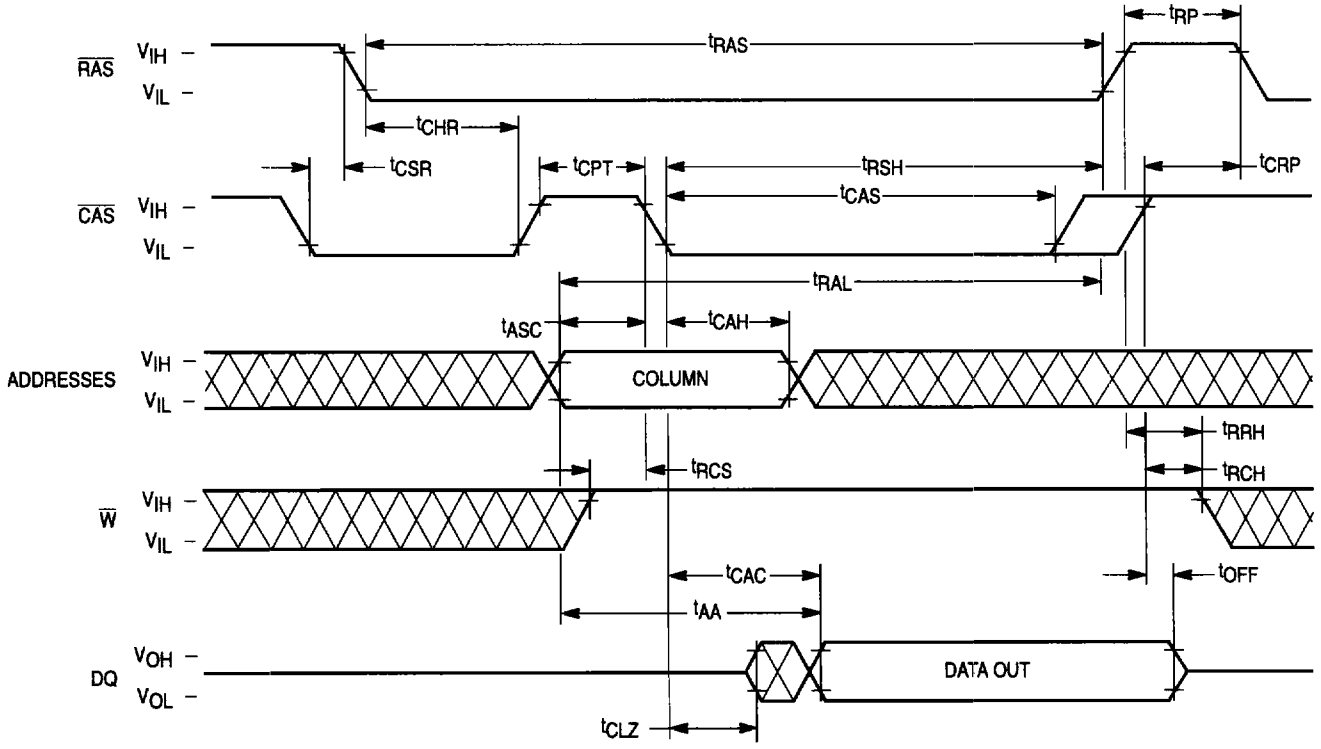
HIDDEN REFRESH CYCLE (READ)



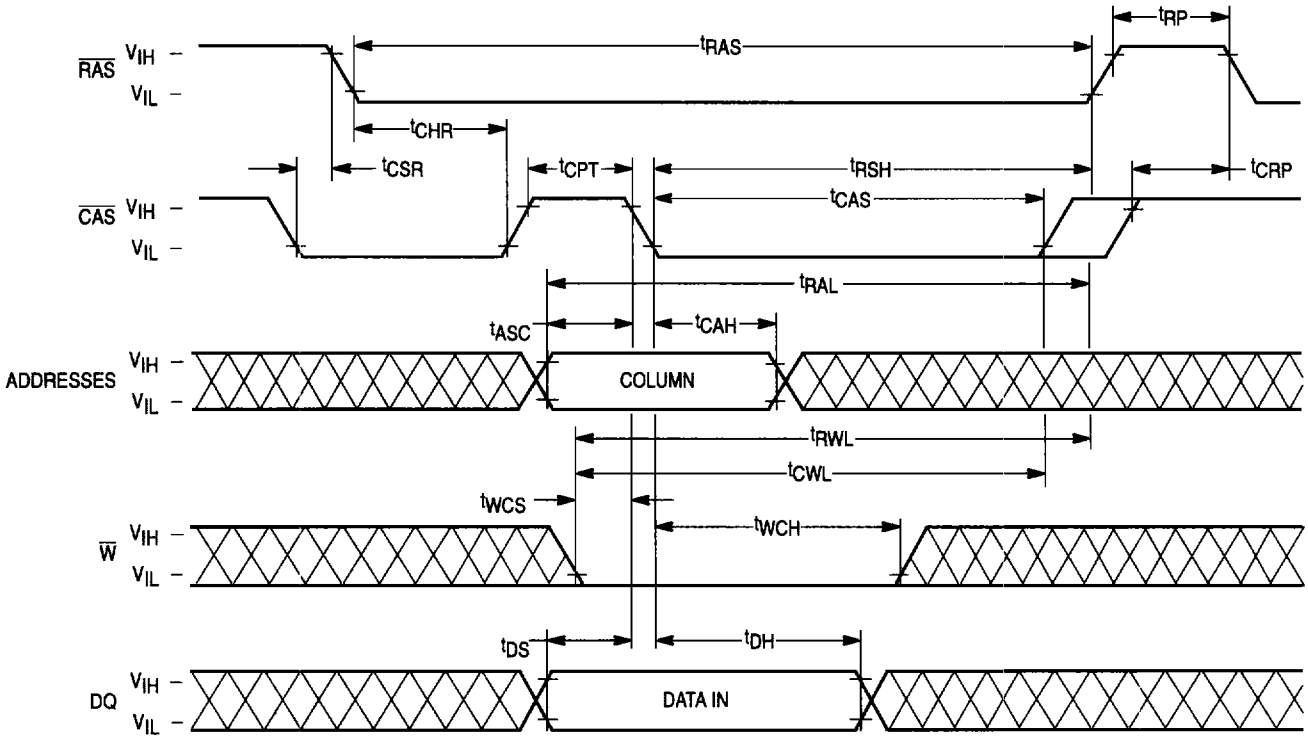
HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 µs is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 ms for the 4MB and 8MB, 32 ms for the 16MB and 32MB), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate address fields. For the 4MB and 8MB, a total of 20 address bits, 10 rows and 10 columns, will decode one of the word locations in the device. For the 16MB and 32MB, a total of 22 address bits, 11 rows and 11 columns, will decode one of the word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: $\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with two different cycles: "normal" random read cycle and fast page mode read cycle. The normal read cycle is outlined here, while the fast page mode cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

$\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

WRITE CYCLE

The user can write to the DRAM with any of two cycles: early write or fast page mode early write. Early write mode is discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data–out buffers disabled.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations on a selected row. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the module require refresh every t_{RFSH}.

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds. Burst refresh, a refresh of all rows consecutively, must be performed every t_{RFSH}.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$–only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$–Only Refresh

$\overline{RAS}$–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after completing one test cycle for every column as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation for every column.
3. Select a column address, and write 1 into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation for every column.
4. Read 1s (normal read mode), which were written at step three.
5. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read and write cycles**. Repeat this operation for every column.
6. Read 0s which were written in step five in normal read mode.
7. Repeat steps one to six using complement data.

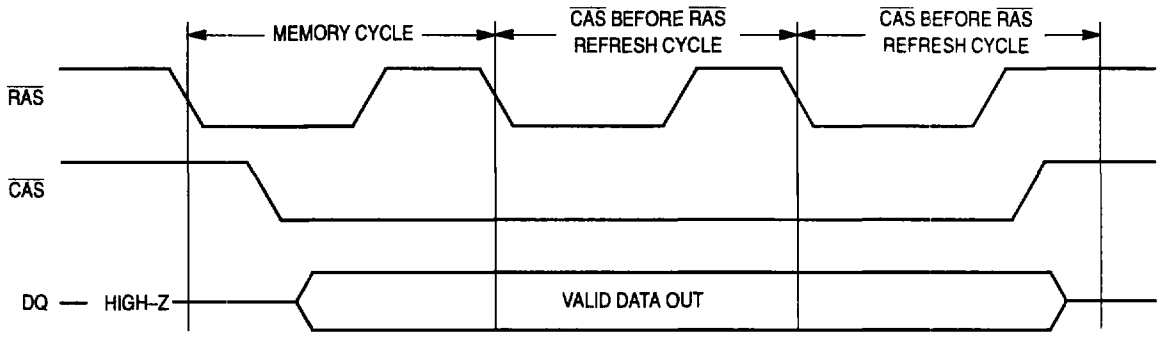
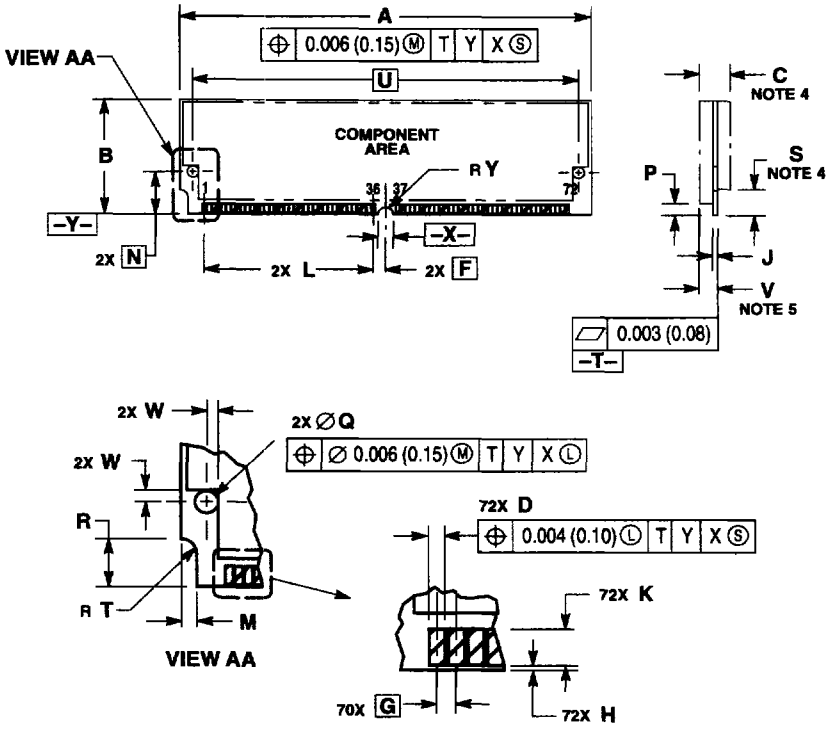


Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSIONS

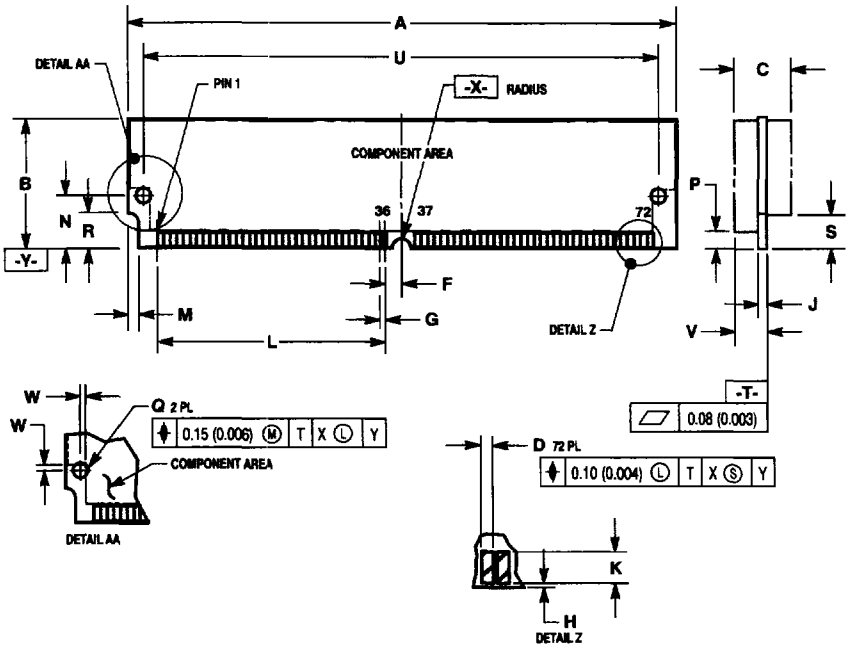
72–LEAD SIMM
CASE 866A–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE–SIDED MODULE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.245	4.255	107.82	108.08
B	1.245	1.255	31.62	31.88
C	—	0.360	—	9.14
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	1.19	—
L	1.750 REF		44.45 REF	
M	0.075	0.085	1.90	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC		101.19 BSC	
V	—	0.208	—	5.28
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

72–LEAD SIMM
CASE 866–02



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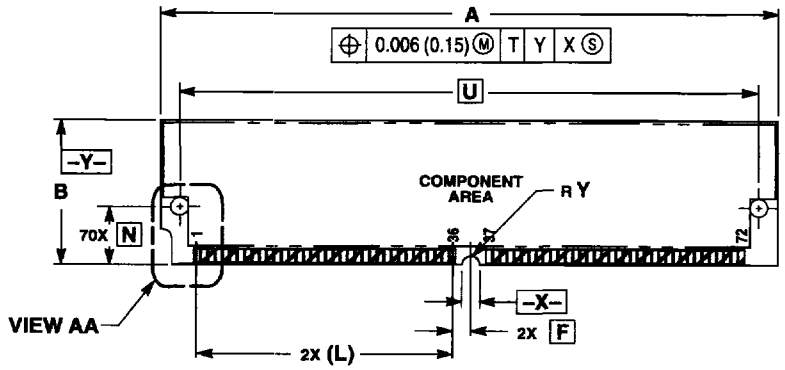
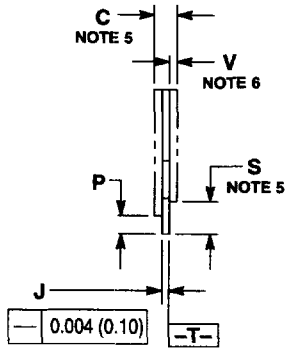
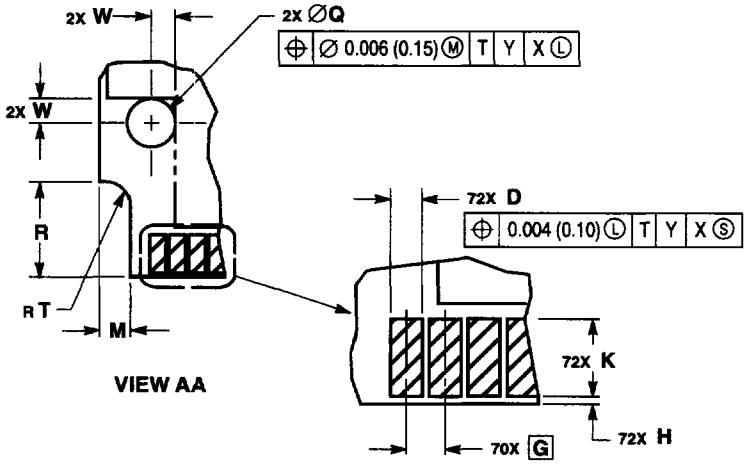
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

72–LEAD SIMM
CASE 866H–01







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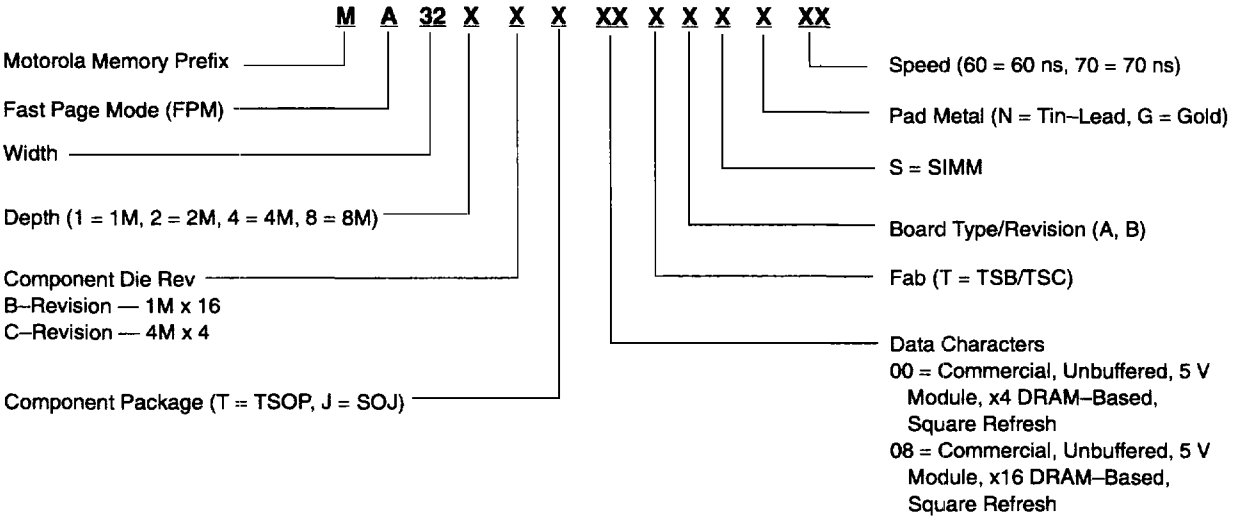
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.245	4.255	107.82	108.08
B	0.995	1.005	25.27	25.53
C	—	0.157	—	4.00
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	2.54	—
L	1.750 REF		44.45 REF	
M	0.075	0.085	1.91	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC		101.19 BSC	
V	—	0.106	—	2.70
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

ORDERING INFORMATION
(Order by Full Part Number)



REPLACEMENT PART NUMBERS FOR 1997

Organization	Old Number	New 60	New 70
1M x 32	MCM32B116S MCM32B116SG MCM32BT116SH MCM32BT116SHG	MA321CJ08TASN60 MA321CJ08TASG60 MA321CT08TASN60 MA321CT08TASG60	MA321CJ08TASN70 MA321CJ08TASG70 MA321CT08TASN70 MA321CT08TASG70
2M x 32	MCM32B216S MCM32B216SG MCM32BT216SH MCM32BT216SHG	MA322CJ08TASN60 MA322CJ08TASG60 MA322CT08TASN60 MA322CT08TASG60	MA322CJ08TASN70 MA322CJ08TASG70 MA322CT08TASN70 MA322CT08TASG70
4M x 32	MCM32C400ASH MCM32C400ASHG MCM32CT400ASH MCM32CT400ASHG	MA324DJ00TBSN60 MA324DJ00TBSG60 MA324DT00TBSN60 MA324DT00TBSG60	MA324DJ00TBSN70 MA324DJ00TBSG70 MA324DT00TBSN70 MA324DT00TBSG70
8M x 32	MCM32C800ASH MCM32C800ASHG MCM32CT800ASH MCM32CT800ASHG	MA328DJ00TBSN60 MA328DJ00TBSG60 MA328DT00TBSN60 MA328DT00TBSG60	MA328DJ00TBSN70 MA328DJ00TBSG70 MA328DT00TBSN70 MA328DT00TBSG70

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