

SMALL-OUTLINE SDRAM MODULE

MT8LSDT1664(L)H
For the latest data sheet, please refer to the Micron Web site: www.micron.com/mtlmspl/html/datasheet.html

FEATURES

- JEDEC-standard, PC66 and PC100 rev 1.0 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 100 MHz, 125 MHz and 133 MHz SDRAM components
- Unbuffered
- 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS

- Self Refresh Current
 - Standard
 - Low power
- Package
 - 144-pin SODIMM (gold)
- Frequency/CAS Latency
 - 133 MHz/CL=2 (7.5ns, 133 MHz SDRAMs) -13E
 - 133 MHz/CL=3 (7.5ns, 133 MHz SDRAMs) -133
 - 100 MHz/CL=2 (8ns, 125 MHz SDRAMs) -10E
 - 66 MHz/CL=2 (10ns, 100 MHz SDRAMs) -662

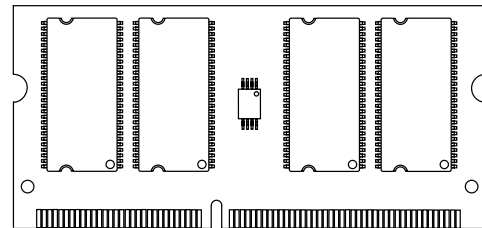
MARKING

None
L
G

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-13E	-7E	2	5.4ns	1.5ns	0.8ns
-133	-75	3	5.4ns	1.5ns	0.8ns
-10E	-8E	2	6ns	2ns	1ns
-662	-10	2	9ns	2ns	1ns

PIN ASSIGNMENT (Front View, 100 MHz) 144-Pin Small-Outline DIMM



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	Vss	2	Vss	73	DNU	74	CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	Vss	140	Vss
69	SO#	70	RFU (A12)	141	SDA	142	SCL
71	S1#	72	RFU (A13)	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	VERSION
MT8LSDT1664HG-13E__	16 Meg x 64	133 MHz, CL = 2
MT8LSDT1664HG-133__	16 Meg x 64	133 MHz, CL = 3
MT8LSDT1664HG-10E__	16 Meg x 64	100 MHz, CL = 2
MT8LSDT1664HG-662__	16 Meg x 64	66 MHz, CL = 2
MT8LSDT1664LHG-13E__	16 Meg x 64*	133 MHz, CL = 2
MT8LSDT1664LHG-133__	16 Meg x 64*	133 MHz, CL = 3
MT8LSDT1664LHG-10E__	16 Meg x 64*	100 MHz, CL = 2
MT8LSDT1664LHG-662__	16 Meg x 64*	66 MHz, CL = 2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT1664HG-10EB1.

*Low power option.

GENERAL DESCRIPTION

The Micron® MT8LSDT1664(L)H is a high-speed CMOS, dynamic random-access, 128MB memory organized in a x64 configuration. This module uses SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK1). Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

This module provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. This module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

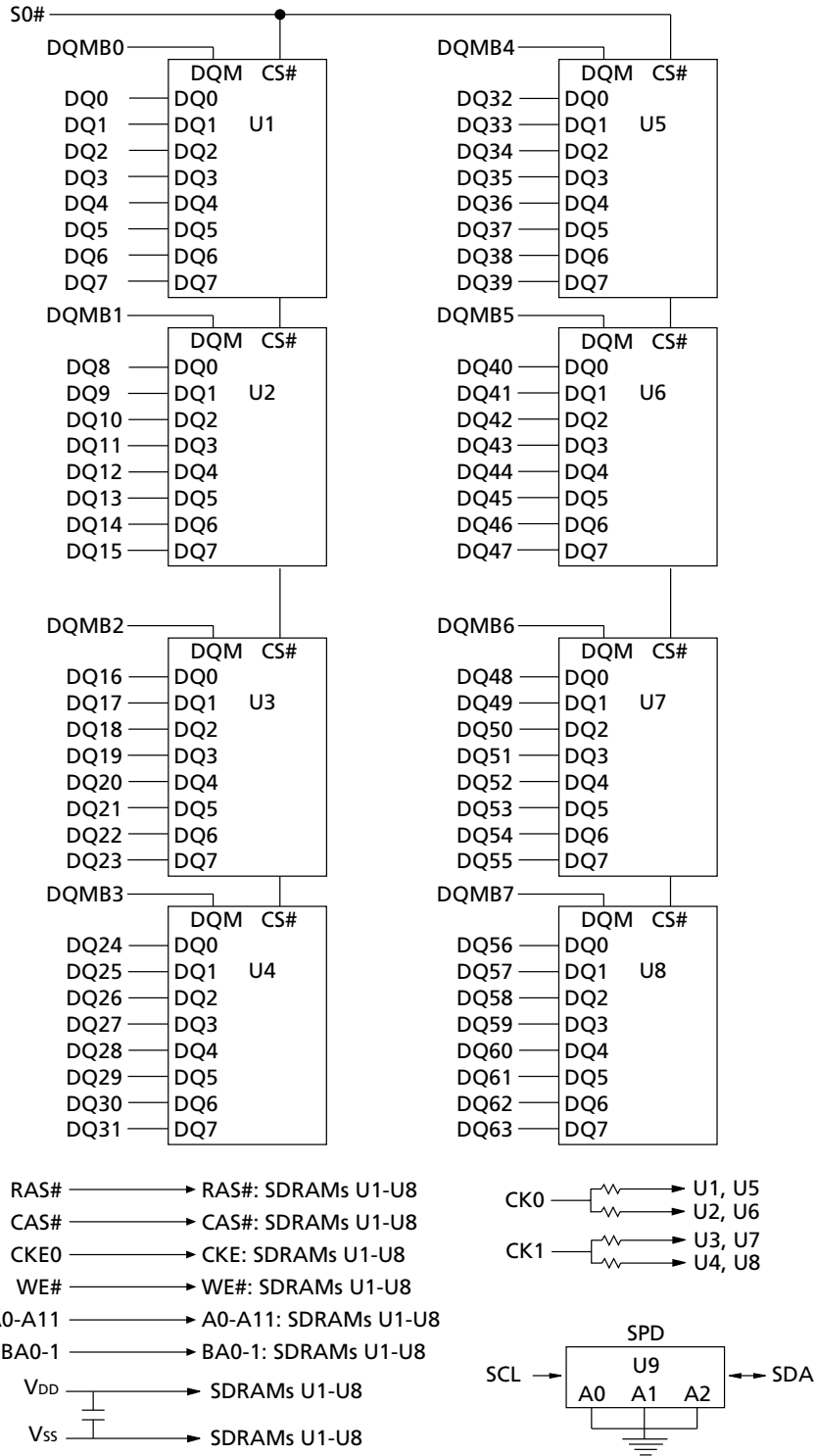
This module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

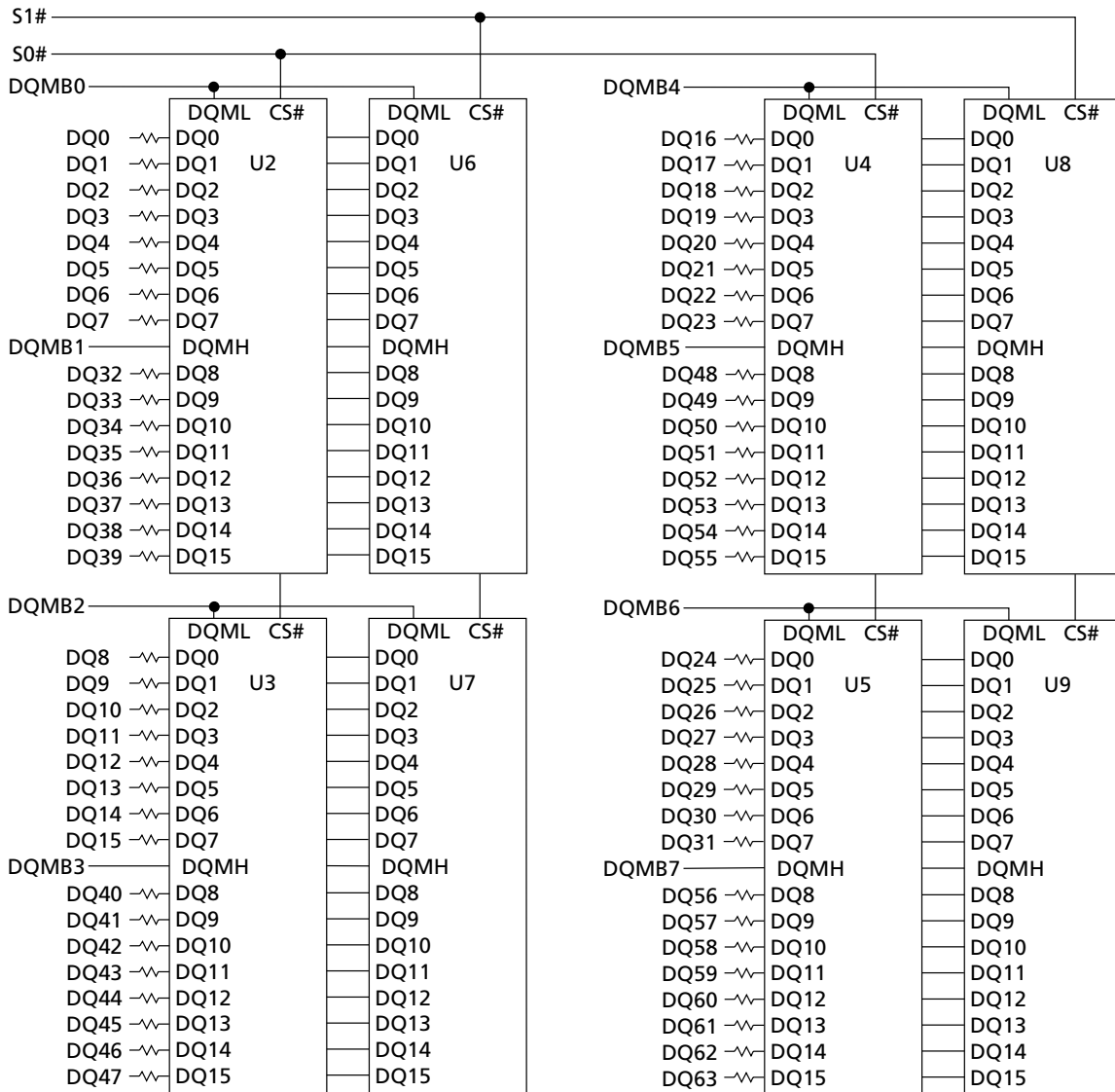
**FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1664(L)H (128MB, 66 MHz)**



NOTE: All resistor values are 10 ohms.

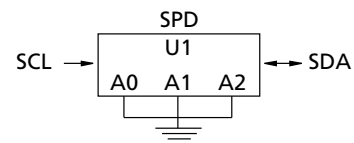
U1-U8 = MT48LC16M8A2TG SDRAMs

**FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1664(L)H (128MB, 133/100 MHz)**



- RAS# → RAS#: SDRAMs U2-U9
- CAS# → CAS#: SDRAMs U2-U9
- CKE0 → CKE: SDRAMs U2-U5
- CKE1 → CKE: SDRAMs U6-U9
- WE# → WE#: SDRAMs U2-U9
- A0-A11 → A0-A11: SDRAMs U2-U9
- BA0-1 → BA0-1: SDRAMs U2-U9
- V_{DD} → SDRAMs U2-U9
- V_{SS} → SDRAMs U2-U9

- CK0 → U2-U5
- CK1 → U6-U9



NOTE: All resistor values are 10 ohms.

U2-U9 = MT48LC8M16A2TG SDRAMs

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
65-67	RAS#, CAS#, WE#	Input	Command Inputs RAS#, CAS# and WE# (along with S0#) define the command being entered.
61, 74	CK0, CK1	Input	Clock: CK0 and CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
62, 68	CKE0, CKE1	Input	Clock Enable: CKE0 and CKE1 activates (HIGH) and deactivates (LOW) the CK0-CK1 signals. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 and CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0 and CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK1, are disabled during power-down and self refresh modes, providing low standby power.
69, 71	S0#, S1#	Input	Chip Select: S0# and S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# and S1# are registered HIGH. S0# and S1# are considered part of the command code.
23-26, 115-118	DQMB0-DQMB7	Input	Input Mask: DQMB is an input mask signal for write accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
106, 110	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the Mode Register.
29-34, 103-105, 109, 111, 112	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A8/A9, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
142	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
3-10, 13-20, 37-44, 47-54, 83-90, 93-100, 121-128, 131-138	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
141	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	V _{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107, 108, 119, 120, 139, 140	V _{SS}	Supply	Ground.
70, 72	RFU	–	Reserved for Future Use: These pins should be left unconnected.
73	DNU	–	Do Not Use: This pin is not connected on these modules but is an assigned pin on the compatible DRAM version.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

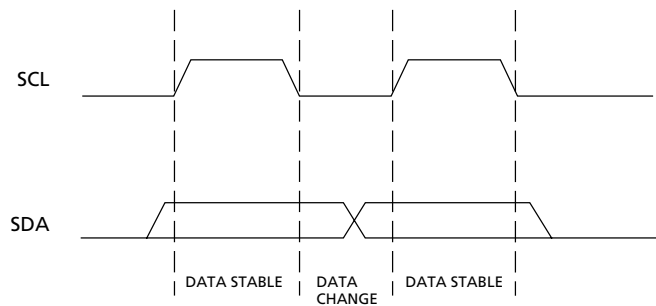
SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

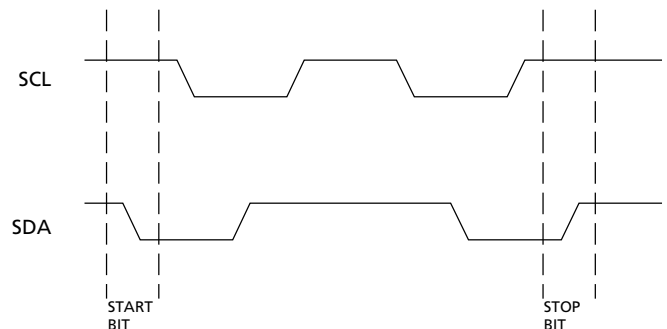
SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

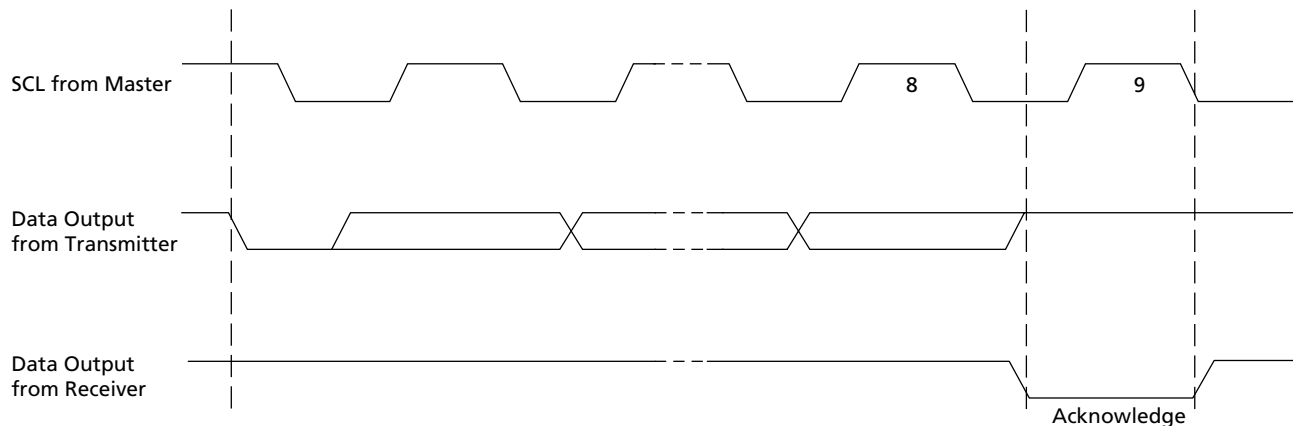
The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.



**Figure 1
Data Validity**



**Figure 2
Definition of Start and Stop**



**Figure 3
Acknowledge Response From Receiver**

SERIAL PRESENCE-DETECT MATRIX (Notes: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSDT1664(L)H(Hex)
0	NUMBER OF BYTES USED BY MICRON	128	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08
2	MEMORY TYPE	SDRAM	04
3	NUMBER OF ROW ADDRESSES	12	0C
4	NUMBER OF COLUMN ADDRESSES	9 (-13E/-133/-10E) 10 (-662)	09 0A
5	NUMBER OF BANKS	2 (-13E/-133/-10E) 1 (-662)	02 01
6	MODULE DATA WIDTH	64	40
7	MODULE DATA WIDTH (continued)	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTTL	01
9	SDRAM CYCLE TIME, t_{CK} (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E) 10 (-662)	70 75 80 A0
10	SDRAM ACCESS FROM CLOCK, t_{AC} (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E) 7.5 (-662)	54 60 75
11	MODULE CONFIGURATION TYPE	NONPARITY	00
12	REFRESH RATE/TYPE	15.6 μ s/SELF	80
13	SDRAM WIDTH (PRIMARY SDRAM)	16 (-13E/-133/-10E) 8 (-662)	10 08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE	00
15	MINIMUM CLOCK DELAY, t_{CCD}	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04
18	CAS LATENCIES SUPPORTED	2, 3	06
19	CS LATENCY	0	01
20	WE LATENCY	0	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E
23	SDRAM CYCLE TIME, t_{CK} (CAS LATENCY = 2)	7.5 (-13E) 10 (-133/-10E) 15 (-662)	75 A0 F0
24	SDRAM ACCESS FROM CLK, t_{AC} (CAS LATENCY = 2)	5.4 (-13E) 6 (-133/-10E) 9 (-662)	54 60 90
25	SDRAM CYCLE TIME, t_{CK} (CAS LATENCY = 1)	—	00
26	SDRAM ACCESS FROM CLK, t_{AC} (CAS LATENCY = 1)	—	00
27	MINIMUM ROW PRECHARGE TIME, t_{RP}	15 (-13E) 20 (-133/-10E) 30 (-662)	0F 14 1E
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, t_{RRD}	14 (-13E) 15 (-133) 20 (-10E/-662)	0E 0F 14

NOTE: "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued) (Notes: 1,2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSDT1664(L)H(Hex)
29	MINIMUM RAS# TO CAS# DELAY, ^t RCD	15 (-13E)	0F
		20 (-133/-10E)	14
		30 (-662)	1E
30	MINIMUM RAS# PULSE WIDTH, ^t RAS	37 (-13E)	25
		44 (-133)	2C
		50 (-10E)	32
		60 (-662)	3C
31	MODULE BANK DENSITY	64MB (-13E/-133/-10E)	10
		128MB (-662)	20
32	COMMAND AND ADDRESS SETUP TIME	1.5 (-13E/-133)	15
		2 (-10E)	20
		0 (-662)	00
33	COMMAND AND ADDRESS HOLD TIME	0.8 (-13E/-133)	08
		1 (-10E)	10
		0 (-662)	00
34	DATA SIGNAL INPUT SETUP TIME	1.5 (-13E/-133)	15
		2 (-10E)	20
		0 (-662)	00
35	DATA SIGNAL INPUT HOLD TIME	0.8 (-13E/-133)	08
		1 (-10E)	10
		0 (-662)	00
36-61	RESERVED		00
62	SPD REVISION	1.2 (-13E/-133/-10E)	12
		1.0 (-662)	01
63	CHECKSUM FOR BYTES 0-62	-13E	58
		-133	A6
		-10E	EE
		-662	58
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C
65-71	MANUFACTURER'S JEDEC ID CODE (continued)		FF
72	MANUFACTURING LOCATION		01
			02
			03
			04
			05
			06
			07
			08
73-90	MODULE PART NUMBER (ASCII)		x
91	PCB IDENTIFICATION CODE	1	01
		2	02
		3	03
		4	04
		5	05
		6	06
		7	07
		8	08
		9	09

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

SERIAL PRESENCE-DETECT MATRIX (continued) (Notes: 1,2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8LSDT1664(L)H(Hex)
92	IDENTIFICATION CODE (continued)	0	00
93	YEAR OF MANUFACTURE IN BCD		x
94	WEEK OF MANUFACTURE IN BCD		x
95-98	MODULE SERIAL NUMBER		x
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		-
126	SYSTEM FREQUENCY	133/100 (-13E/-133/-10E)	64
		66 (-662)	66
127	SDRAM COMPONENT AND CLOCK DETAIL	-13E/-133/-10E	CF
		-662	06

- NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
 2. x = Variable Data.

COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description of

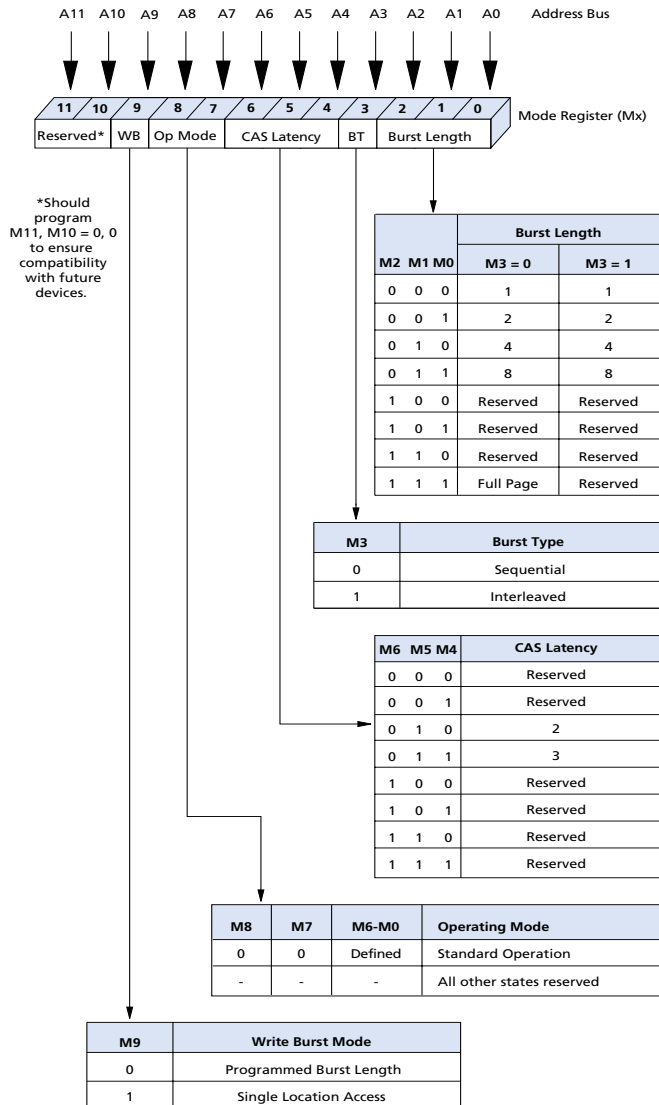
commands and operations, refer to the 128Mb x4, x8, x16 SDRAM data sheet.

TRUTH TABLE 1 – Commands and DQMB Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H ⁸	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H ⁸	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
 2. A0-A11 define the op-code written to the Mode Register.
 3. A0-A11 provide row address and BA0, BA1 determine which bank is made active.
 4. A0-A8/A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
 5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care."
 6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
 7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
 8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).



**Figure 4
Mode Register Definition**

**Table 1
Burst Definition**

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
Full Page (Y)	n = A0-A8/A9 (location 0-Y)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

- NOTE:**
1. For full-page accesses: y = 512 (133 MHz/100 MHz), y = 1,024 (66 MHz).
 2. For a burst length of two, A1-A8/A9 select the block-of-two burst; A0 selects the starting column within the block.
 3. For a burst length of four, A2-A8/A9 select the block-of-four burst; A0-A1 select the starting column within the block.
 4. For a burst length of eight, A3-A8/A9 select the block-of-eight burst; A0-A2 select the starting column within the block.
 5. For a full-page burst, the full row is selected, and A0-A8/A9 select the starting column.
 6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
 7. For a burst length of one, A0-A8/A9 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} -1V to +4.6V
 Voltage on Inputs, NC or I/O Pins
 Relative to V_{SS} -1V to +4.6V
 Operating Temperature, T_A (ambient) ... 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 8W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

 (Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
SUPPLY VOLTAGE	V _{DD}	3	3.6	V		
INPUT HIGH VOLTAGE: Logic 1; All inputs	V _{IH}	2	V _{DD} +0.3	V	2	
INPUT LOW VOLTAGE: Logic 0; All inputs	V _{IL}	-0.5	0.8	V	2	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} (All other pins not under test = 0V)	CK0, CK1, S0#, S1#, CKE0, CKE1	I _{I1}	-20	20	μA	3
	RAS#, CAS#, WE#, BA0, BA1, A0-A11	I _{I2}	-40	40	μA	
	DQMB0-DQMB7	I _{I3}	-10	10	μA	4
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DD}	DQ0-DQ63	I _{OZ}	-10	10	μA	4
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -4mA) Output Low Voltage (I _{OUT} = 4mA)	V _{OH}	2.4	-	V		
	V _{OL}	-	0.4	V		

- NOTE:**
1. All voltages referenced to V_{SS}.
 2. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
 3. 133 MHz/100 MHz module values for S0# and CDED will be twice those shown.
 4. 66 MHz module values will be half of those shown.

I_{DD} SPECIFICATIONS AND CONDITIONS

 (Notes: 1, 2, 3, 4) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX				UNITS	NOTES	
		-13E	-133	-10E	-662			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^t RC = ^t RC (MIN); CAS latency = 3	I _{DD1}	840	800	720	1,040	mA	5, 6, 7, 8	
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I _{DD2}	16	16	16	16	mA	8	
STANDBY CURRENT: Active Mode; S0#, S1# = HIGH; CKE = HIGH; All banks active after ^t RCD met; No accesses in progress	I _{DD3}	400	400	320	400	mA	5, 7, 8, 9	
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3	I _{DD4}	860	800	720	1,120	mA	5, 6, 7, 8	
AUTO REFRESH CURRENT: CKE = HIGH; S0# = HIGH	^t RC = ^t RC (MIN); CL = 3	I _{DD5}	1,520	1,440	1,240	1,600	mA	5, 6, 7, 8, 10, 12
	^t RC = 15.625µs; CL = 3	I _{DD6}	24	24	24	24	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I _{DD7}	16	16	16	16	mA	11
	Low power (L)	I _{DD7}	8	8	8	8	mA	

- NOTE:**
- All voltages referenced to V_{SS}.
 - An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
 - AC timing tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to the 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crossover point.
 - I_{DD} specifications are tested after the device is properly initialized.
 - I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
 - The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
 - Address transitions average one transition every two clocks.
 - ^tCK = 7.5ns for -13E/-133; ^tCK = 10ns for -10E.
 - Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
 - CKE is HIGH during refresh command period (^tRFC [MIN]) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.
 - Enables on-chip refresh and address counters.
 - Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.

CAPACITANCE

PARAMETER	SYMBOL	-13X/-10E		-662		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#	C11	22	32	22	32	pF	1
Input Capacitance: S0#, S1#, CKE0, CKE1	C12	12	18	22	32	pF	1
Input Capacitance: CK0, CK1	C12	12	18	12	18	pF	1
Input Capacitance: DQMB0#-DQMB7#	C13	7	10	4	6	pF	1
Input Capacitance: SCL, SDA	C101	–	10	–	10	pF	1
Input/Output Capacitance: DQ0-DQ63	C102	10	14	6	8	pF	1

NOTE: 1. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1 \text{ MHz}$.

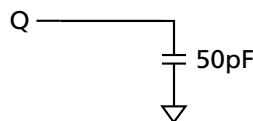
SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 1, 2, 3, 4, 5, 6)

AC CHARACTERISTICS			-13E		-133		-10E		-662			
PARAMETER		SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	t_{AC}		5.4		5.4		6		7.5	ns	
	CL = 2	t_{AC}		5.4		6		6		9	ns	
Address hold time		t_{AH}	0.8		0.8		1		1		ns	
Address setup time		t_{AS}	1.5		1.5		2		2		ns	
CLK high-level width		t_{CH}	2.5		2.5		3		3		ns	
CLK low-level width		t_{CL}	2.5		2.5		3		3		ns	
Clock cycle time	CL = 3	t_{CK}	7		7.5		8		10		ns	7
	CL = 2	t_{CK}	7.5		10		10		15		ns	7
CKE hold time		t_{CKH}	0.8		0.8		1		1		ns	
CKE setup time		t_{CKS}	1.5		1.5		2		2		ns	
CS#,RAS#,CAS#,WE#,DQM hold time		t_{CMH}	0.8		0.8		1		1		ns	
CS#,RAS#,CAS#,WE#,DQM setup time		t_{CMS}	1.5		1.5		2		2		ns	
Data-in hold time		t_{DH}	0.8		0.8		1		1		ns	
Data-in setup time		t_{DS}	1.5		1.5		2		2		ns	
Data-out high-impedance time	CL = 3	t_{HZ}		5.4		5.4		6		8	ns	8
	CL = 2	t_{HZ}		5.4		6		7		10	ns	8
Data-out low-impedance time		t_{LZ}	1		1		1		2		ns	
Data-out hold time (load)		t_{OH}	2.7		2.7		3		3		ns	
Data-out hold time (no load)		t_{OH_N}	1.8		1.8		1.8		n/a		ns	9
ACTIVE to PRECHARGE command		t_{RAS}	37	120,000	44	120,000	50	120,000	60	120,000	ns	
ACTIVE to ACTIVE command period		t_{RC}	60		66		70		90		ns	
ACTIVE to READ or WRITE delay		t_{RCD}	15		20		20		30		ns	
Refresh period (4,096 rows)		t_{REF}		64		64		64		64	ms	
AUTO REFRESH period		t_{RFC}	66		66		70		90		ns	
PRECHARGE command period		t_{RP}	15		20		20		30		ns	10
ACTIVE bank A to ACTIVE bank B command		t_{RRD}	14		15		20		20		ns	
Transition time		t_T	0.3	1.2	0.3	1.2	0.3	1.2	1	1.2	ns	11
WRITE recovery time		t_{WR}	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		1 CLK + 7ns		-	12
			14		15		15		15		ns	13
Exit SELF REFRESH to ACTIVE command		t_{XSR}	67		75		80		90		ns	14

*Specifications for the SDRAM components used on the module.

- NOTE:**
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) is ensured.
 - An initial pause of 100 μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
 - AC characteristics assume $t_T = 1\text{ns}$.
 - In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
 - Outputs measured at 1.5V with equivalent load:



- AC timing tests have $V_{IL} = 0\text{V}$ and $V_{IH} = 3\text{V}$, with timing referenced to the 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at $V_{IL}(\text{MAX})$ and $V_{IL}(\text{MIN})$ and no longer at the 1.5V crossover point.

NOTES (continued)

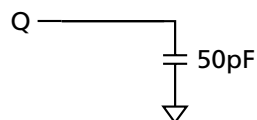
7. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including 'WR , and PRECHARGE commands). CKE may be used to reduce the data rate.
8. 'HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} . The last valid data element will meet 'OH before going High-Z.
9. Parameter guaranteed by design.
10. Based on $\text{'CK} = 133 \text{ MHz (-13E/-133)}$, 100 MHz (-10E) , or 66 MHz (-662) .
11. AC characteristics assume $\text{'T} = 1 \text{ ns}$.
12. Auto precharge mode only. The precharge timing budget ('RP) begins $7.5 \text{ ns}/7 \text{ ns}$ after the first clock delay, after the last WRITE is executed.
13. Precharge mode only.
14. CLK must be toggled a minimum of two times during this period.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 1, 2, 3, 4, 5, 6)

PARAMETER	SYMBOL	-13E	-133	-10E/-662	UNITS	NOTES
READ/WRITE command to READ/WRITE command	t_{CCD}	1	1	1	t_{CK}	7
CKE to clock disable or power-down entry mode	t_{CKED}	1	1	1	t_{CK}	8
CKE to clock enable or power-down exit setup mode	t_{PED}	1	1	1	t_{CK}	8
DQM to input data delay	t_{DQD}	0	0	0	t_{CK}	7
DQM to data mask during WRITES	t_{DQM}	0	0	0	t_{CK}	7
DQM to data high-impedance during READs	t_{DQZ}	2	2	2	t_{CK}	7
WRITE command to input data delay	t_{DWD}	0	0	0	t_{CK}	7
Data-in to ACTIVE command	t_{DAL}	4	5	4	t_{CK}	9, 10
Data-in to PRECHARGE command	t_{DPL}	2	2	2	t_{CK}	10, 11
Last data-in to burst STOP command	t_{BDL}	1	1	1	t_{CK}	7
Last data-in to new READ/WRITE command	t_{CDL}	1	1	1	t_{CK}	7
Last data-in to PRECHARGE command	t_{RDL}	2	2	2	t_{CK}	10, 11
LOAD MODE REGISTER command to ACTIVE or REFRESH command	t_{MRD}	2	2	2	t_{CK}	12
Data-out to high-impedance from PRECHARGE command	CL = 3	t_{ROH}	3	3	t_{CK}	7
	CL = 2	t_{ROH}	2	2	t_{CK}	7

- NOTE:**
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) is ensured.
 - An initial pause of 100 μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
 - AC characteristics assume $t_T = 1\text{ns}$.
 - In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
 - Outputs measured at 1.5V with equivalent load:



- AC timing tests have $V_{IL} = 0\text{V}$ and $V_{IH} = 3\text{V}$, with timing referenced to the 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at $V_{IL}(\text{MAX})$ and $V_{IL}(\text{MIN})$ and no longer at the 1.5V crossover point.
- Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
- Timing actually specified by t_{CKS} ; clock(s) specified as a reference only at minimum cycle rate.
- Timing actually specified by t_{WR} plus t_{RP} ; clock(s) specified as a reference only at minimum cycle rate.
- Based on $t_{CK} = 133\text{MHz}$ (-13E/-133), 100 MHz (-10E), or 66 MHz (-662).
- Timing actually specified by t_{WR} .
- JEDEC and PC100 specify three clocks.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	V_{OL}	-	0.4	V	
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to V_{DD}	I_{LI}	-	10	μA	
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to V_{DD}	I_{LO}	-	10	μA	
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$; All other inputs = GND or $3.3V + 10\%$	I_{SB}	-	30	μA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	-	2	mA	

NOTE: 1. All voltages referenced to V_{SS} .

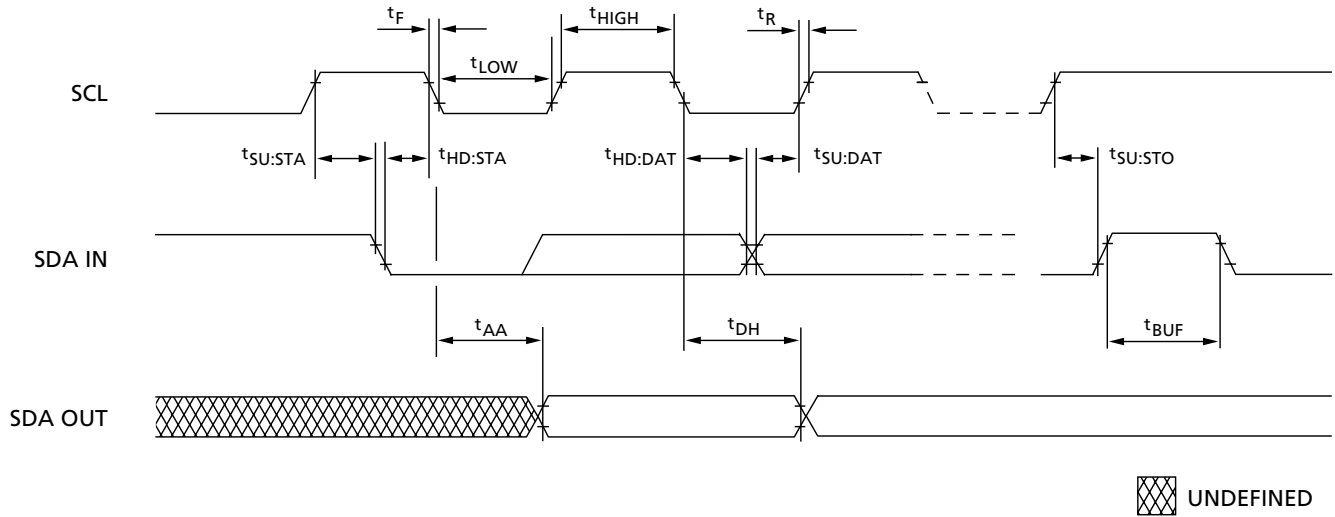
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	t_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WRC}		10	ms	2

NOTE: 1. All voltages referenced to V_{SS} .
2. Timing actually specified by t_{WR} .

SPD EEPROM

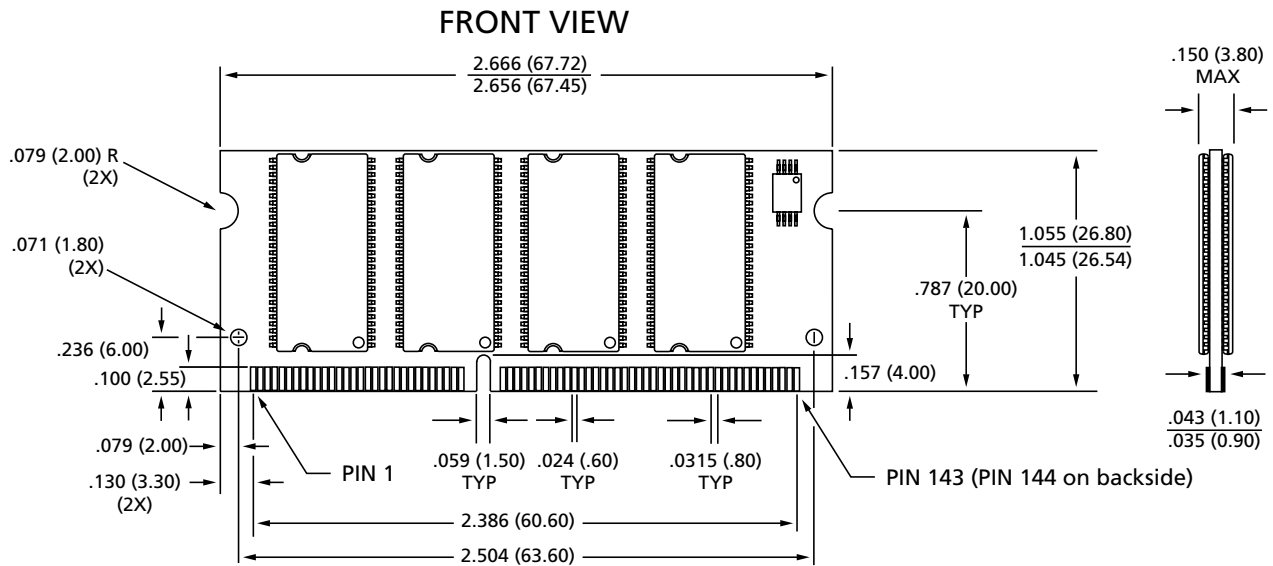


**SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS**

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μs
t_{BUF}	4.7		μs
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μs
$t_{HD:STA}$	4		μs

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		μs
t_{LOW}	4.7		μs
t_R		1	μs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μs
$t_{SU:STO}$	4.7		μs

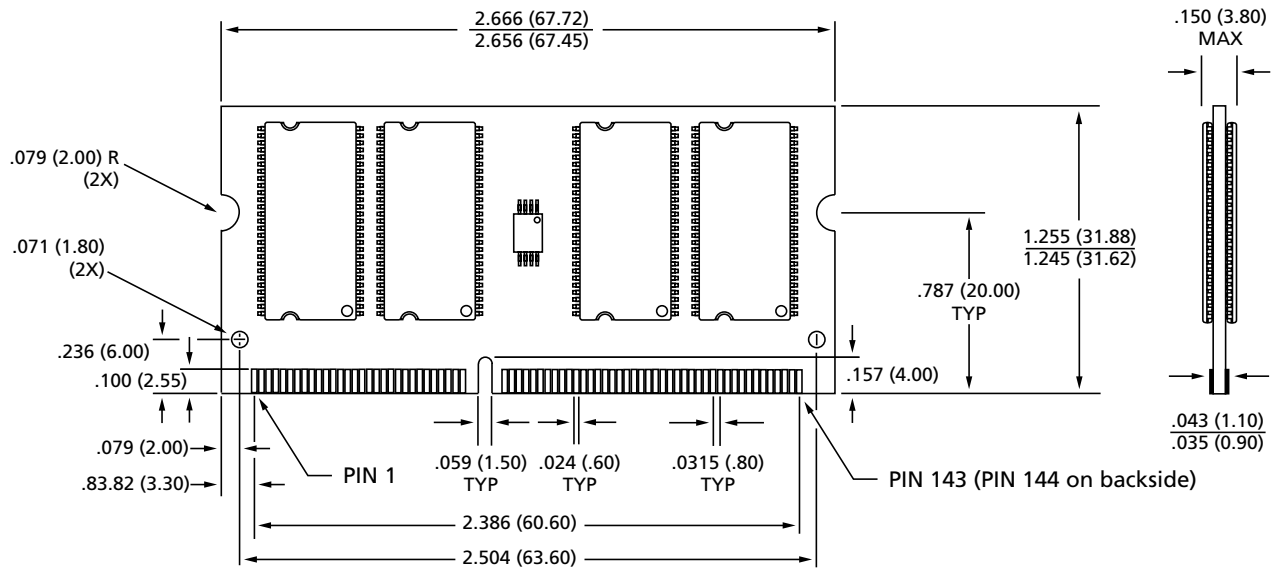
**144-PIN SODIMM
(128MB, 66 MHz)**



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

**144-PIN SODIMM
(128MB, 133 MHz/100 MHz)**

FRONT VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



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