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S1R72V18
Data Sheet

SEIKO EPSON CORPORATION

Rev.1.00

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Scope

This document applies to the S1R72V18 USB 2.0 device/host controller LSI.

Contents

1. Overview

The S1R72V18 is a USB host/device controller LSI that supports the USB 2.0 high-speed mode. It features two host ports to function as a USB root hub. One of the ports can be used as a USB device port after setting a switch to the appropriate setting.

2. Features

<<USB 2.0 host functions>>

- 2-port root hub
- Supports HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) transfer
- Built-in pull-down resistor for downstream ports (no external circuit required)
- Built-in HS termination (no external circuit required)
- Supports control, bulk, interrupt, and isochronous transfers

  Proven channel system designed specifically for embedded host

  One control transfer channel for each port

  One bulk transfer channel for each port

  Four bulk, interrupt, and isochronous transfer channels for each port
- USB power switching interface

<<USB 2.0 device functions>>

- Supports HS (480 Mbps) and FS (12 Mbps) transfer
- Built-in FS/HS termination (no external circuit required)
- VBUS 5V I/F (requires external protective circuit)
- Supports control, bulk, interrupt, and isochronous transfers
- Supports five bulk, interrupt, and isochronous transfers and Endpoint 0

<<MCU I/F>>

- Supports 16-bit width standard CPU bus I/F
- Includes DMA 1ch for each port (multi-word sequence)
- Big Endian (Includes bus-swapping function to support Little Endian CPUs)
- I/F variable voltage (3.3 V to 1.8 V)

<<Miscellaneous>>

- Clock input: Supports 12 MHz/24 MHz crystal oscillator. (built-in oscillator circuit and 1 MΩ feedback resistor)
- Power supply voltage: 3-voltage system including 3.3 V, 1.8 V, and CPU I/F power supply (3.3 V to 1.8 V)
- Package type QFP14-80, PFBGA10UX121
- Guaranteed operating temperature range: -40°C to 85°C

3. Block Diagram

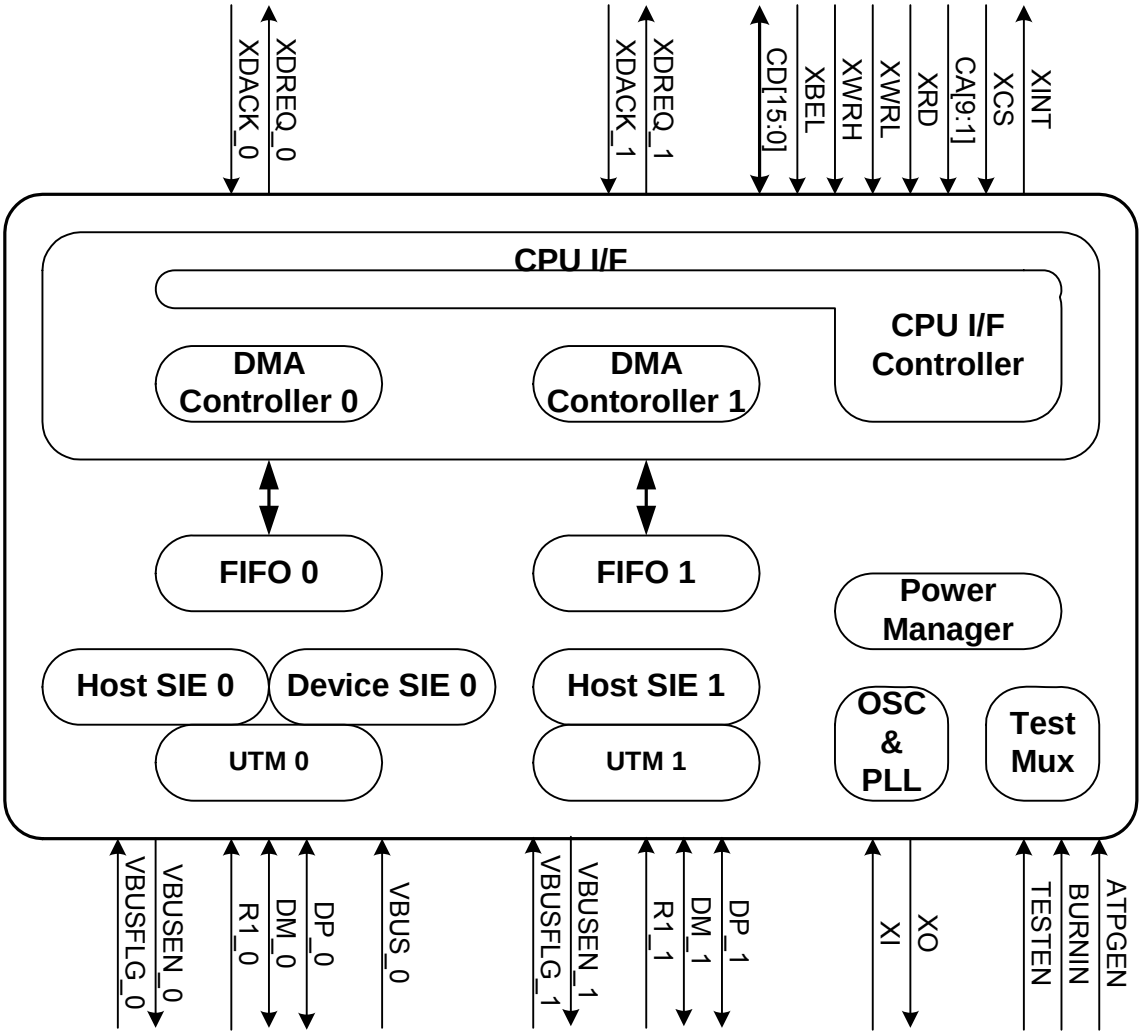


Figure 3-1 Overall block diagram

4. Explanation of Functions

For details of the register names used in the following discussion, refer to the Technical Manual for this LSI. Apart from USB device functions, some of the registers in this LSI have the same functions for each port. Note that this is indicated only when explaining the functions for individual ports.

4.1 Power Supply

This LSI has three power supply systems and a common GND. The power supply systems consist of HVDD (3.3 V) for the USB I/O power supply, CVDD (3.3 V to 1.8 V) for the CPU I/F power supply, and LVDD (1.8 V) for internal circuits and TEST I/O. (See Figure 4-1.)

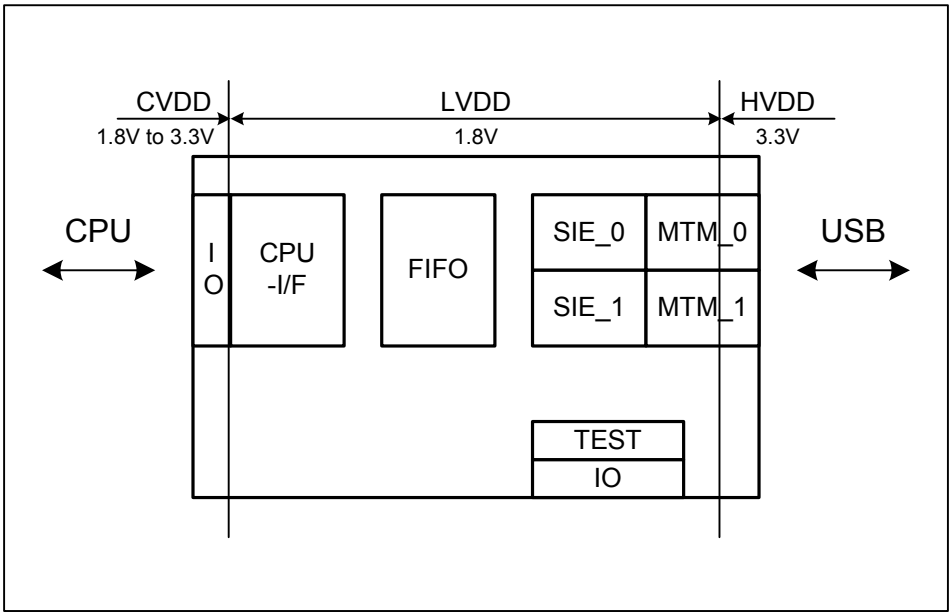


Figure 4-1 S1R72V18 power supply circuit diagram

The sequence of steps for turning the power supplies on and off are described below.

This LSI does not allow individual power supply circuits to be held in a continuous on or off state. Also, the following restrictions apply to the sequence for turning the CVDD/HVDD I/O power supplies and LVDD internal power supply on or off. There are no restrictions on the sequence for turning the CVDD and HVDD power supplies on or off.

- In the power on sequence, the LVDD must be turned on before turning on the CVDD and HVDD.
- In the powering off sequence, the CVDD and HVDD must be turned off before turning off the LVDD.

If power supply circuit characteristics or the power supply load make this sequence impossible to follow, the CVDD or HVDD must not be on for more than 1 second while the LVDD is off.

4.2 Reset

This LSI includes a hard reset function using the external XRESET terminal and a soft reset function using register settings.

4.2.1 Hard Reset

Start up from reset status when power is turned on, then cancel the reset after confirming power on.

4.2.2 Soft Reset

The USB circuits can be reset, or internal USB analog macros can be reset individually, via software. The ChipReset.AllReset bit initializes all circuits except the CPUIF_MODE register, or the ChipReset.ResetMTM bit for each port is used to reset individual port USB analog macros. Note that the USB analog macro should be reset only when in the sleep state.

4.3 Clock

This LSI incorporates an internal oscillator and feedback resistor (1 MΩ) and supports clock generation with an external oscillator. The oscillator frequency can be set to 12 MHz or 24 MHz via register settings.

Figure 4-2 shows a typical connection configuration for an oscillation circuit. Cd, Cg, and Rd in the oscillator circuit shown must be matched for the specific oscillator. Contact the oscillator manufacturer to obtain circuit constants.

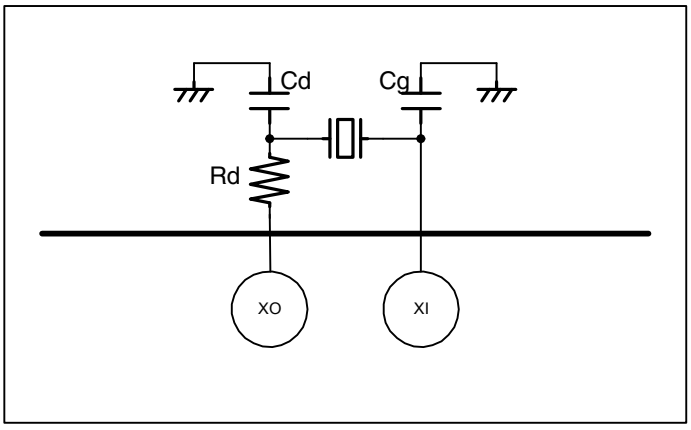


Figure 4-2 Clock generation using the internal oscillator and external oscillator

4.4 Power Management

This LSI includes a power management function featuring two power management states for each port, SLEEP and ACTIVE, together with the CPU_Cut power management state common for the chip. (See Figure 4-3.)

All function blocks are active in the ACTIVE state, whereas only the bare minimum circuits necessary for restarting from standby mode are active in SLEEP state. CPU_Cut mode minimizes power consumption attributable to the CPU-I/F input buffer.

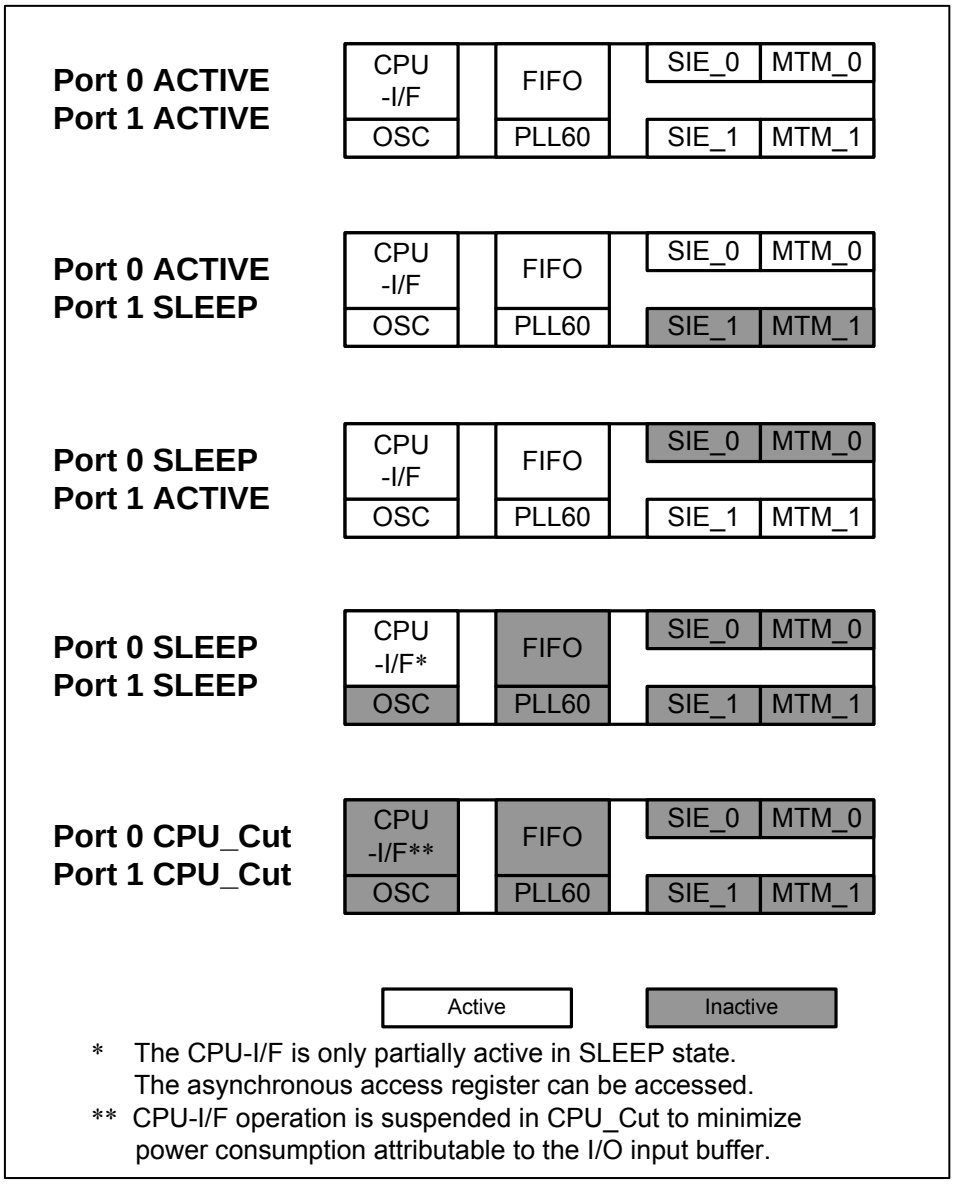


Figure 4-3 Power management states

4.5 CPU-I/F

This LSI is connected to the CPU via a 16-bit interface. Endian settings can be set as Big Endian or Little Endian in 16-bit steps. For Big Endian, registers with even addresses can be accessed above the bus (CD[15:8]), while registers with odd addresses can be accessed below the bus (CD[7:0]). For Little Endian, registers with even addresses can be accessed below the bus (CD[7:0]), while registers with odd addresses can be accessed above the bus (CD[15:8]).

The bus mode can be set to either Strobe mode for access using high/low strobe (XWRH/XWRL) or Byte Enable mode for access using high/low byte enable (XBEH/XBEL) for writing the first or last 8 bits. Endian and bus mode is set by the CPUIF_MODE register immediately after reset cancelling.

The CPU-I/F on this LSI includes 1-ch DMA (slave) for each port (2-ch in total).

The registers that can be accessed will depend on the power management state. For details, refer to the LSI Technical Manual.

4.6 USB Device I/F

This LSI supports High-Speed specification USB device functions complying with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.6.1 Speed Mode and Transfer Type

This LSI's USB device function supports HS (480 Mbps) and FS (12 Mbps) speed modes. The speed mode is set automatically by the speed negotiation performed when resetting the bus. For example, HS transfer mode is selected automatically by speed negotiation if connected to a USB host that supports HS speed mode. In addition, the register can be set so that FS speed mode is always selected in speed negotiations.

All transfer types stipulated under the USB 2.0 standard are supported, including control transfers (endpoint 0), bulk transfers, interrupt transfers, and isochronous transfers.

4.6.2 Resources

4.6.2.1 Endpoint

This LSI's USB device function includes endpoint 0 and five standard endpoints. Endpoint 0 supports control transfers. The standard endpoints support bulk transfers, interrupt transfers, and isochronous transfers. The standard endpoint numbers, maximum packet size, and transfer direction (in/out) can be set as desired.

4.6.2.2 FIFO

The LSI ports include 4.5 kB of FIFO for use with USB data transfers. This forms the data transfer route with USB. The FIFO capacity of each endpoint can be assigned as desired by the software. For example, performance can be improved by assigning a sufficient size FIFO area to the endpoints for bulk transfers.

4.6.3 Data Flow

Endpoints are assigned to USB FIFO areas on a one-to-one basis, and responses are returned to USB transactions automatically, depending on effective USB FIFO free capacity (for OUT transfers) or effective data quantity (for IN transfers). This means the software does not need to be directly involved in individual transactions, allowing USB data transfers to be controlled as data flows at the USB FIFO.

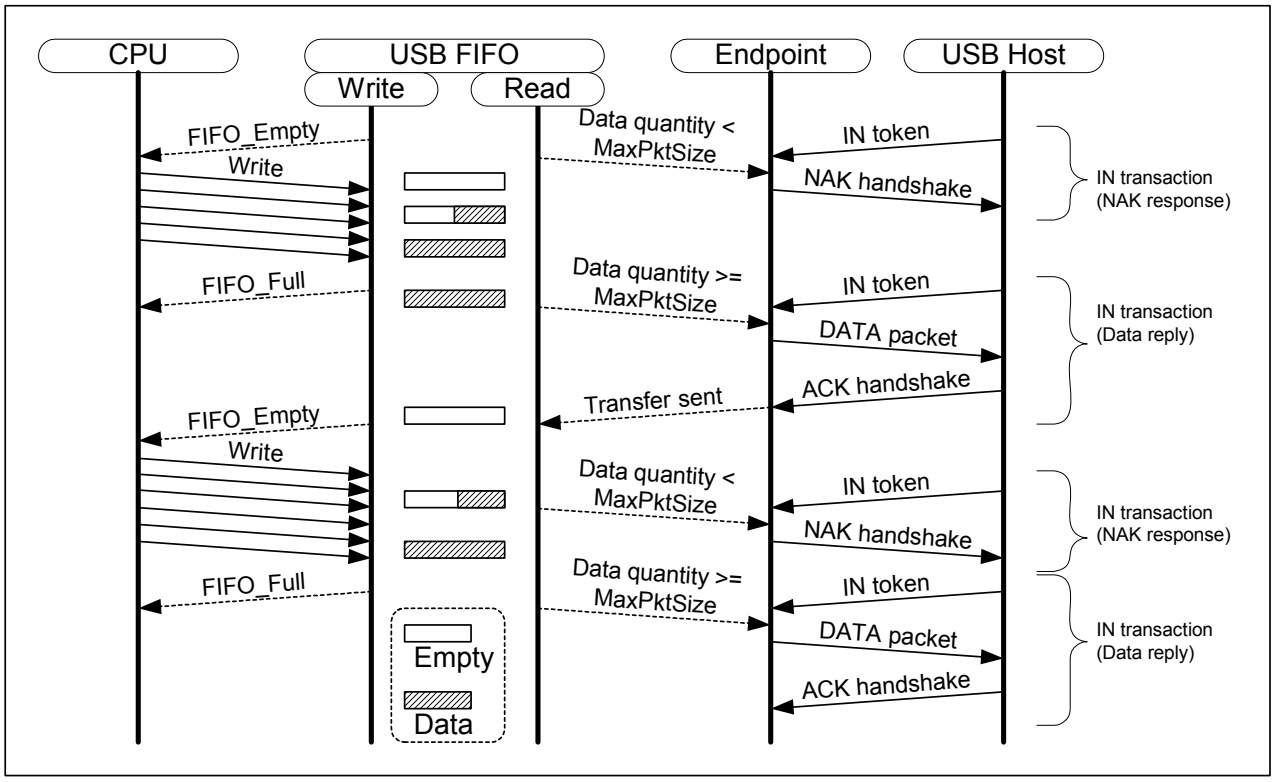


Figure 4-4 Typical data flow (with FIFO assigned for MaxPktSize and IN transfer)

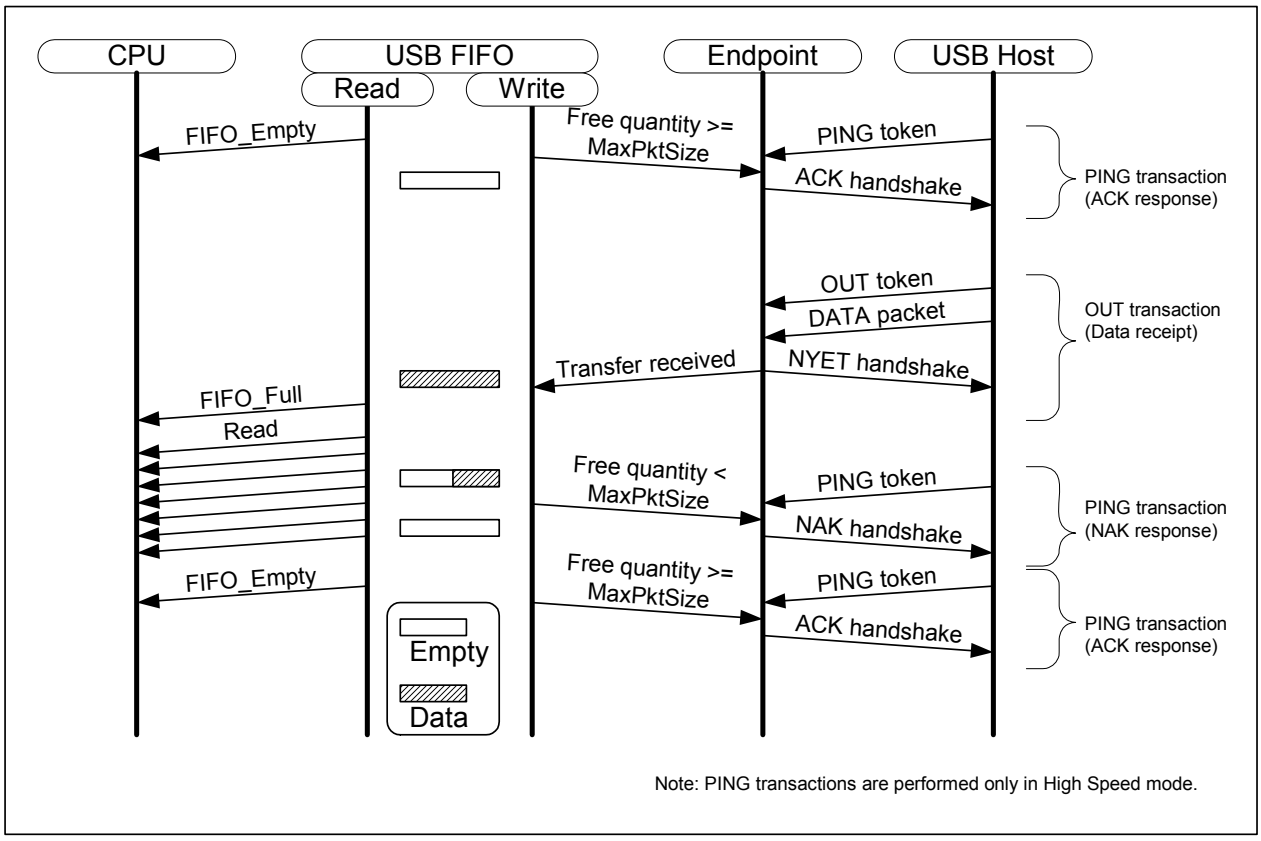


Figure 4-5 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfer)

4.6.4 USB Device Port External Circuits

The LSI USB Port 0 has internal FS and HS device termination resistors, eliminating the need for the components normally used to adjust impedance. This allows a DP/DM line to be connected directly between the LSI terminal and the connector. Note that the appropriate components must be used to ensure static electricity protection and to implement EMI precautions.

The VBUS terminal uses a 5 V input and does not require external voltage conversion. A protection circuit is recommended, since certain commercially-available USB host and hub products may apply surge voltages exceeding VBUS ratings.

Refer to the separately provided PCB Design Guidelines for S1R72V Series USB 2.0 Hi-Speed.

4.7 USB Host I/F

The LSI USB Port 0 and Port 1 support high-speed specification USB host functions complying with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.7.1 Speed Mode and Transfer Type

This LSI's USB host function supports HS (480 Mbps), FS (12 Mbps) and LS (1.5 Mbps) speed modes. The speed mode is automatically set by speed negotiations performed on resetting the bus.

All transfer types stipulated in the USB 2.0 standard are supported, including control transfers, bulk transfers, interrupt transfers, and isochronous transfers.

4.7.2 Resources

4.7.2.1 Channels

In the LSI USB host functions, sets of register settings for transfers with end points on a one-to-one basis are called channels. The LSI USB host function features one dedicated channel for control transfers, one dedicated channel for bulk transfers, and four general channels that support bulk transfers, interrupt transfers, and isochronous transfers. The endpoint number, maximum packet size, and transfer direction (IN/OUT) can be set as desired for all channels. Transfers are also possible for a number of endpoints exceeding the channel number using software-based time-multiplexing for the channels.

4.7.2.2 FIFO

Each port on the LSI includes 4.5 kB of FIFO for use with USB data transfers. This forms the data transfer route with USB. The FIFO capacity for each channel can be assigned as desired by the software. For example, to improve performance, assign a FIFO area of adequate size to the endpoints for bulk transfers.

4.7.3 Data Flow

The channels are assigned to FIFO areas on a one-to-one basis. Transactions are sent automatically to USB, depending on the FIFO effective free capacity (for IN transfers) or effective data quantity (for OUT transfers). The software does not need to be directly involved in individual transactions, allowing USB data transfers to be controlled as data flow at the FIFO.

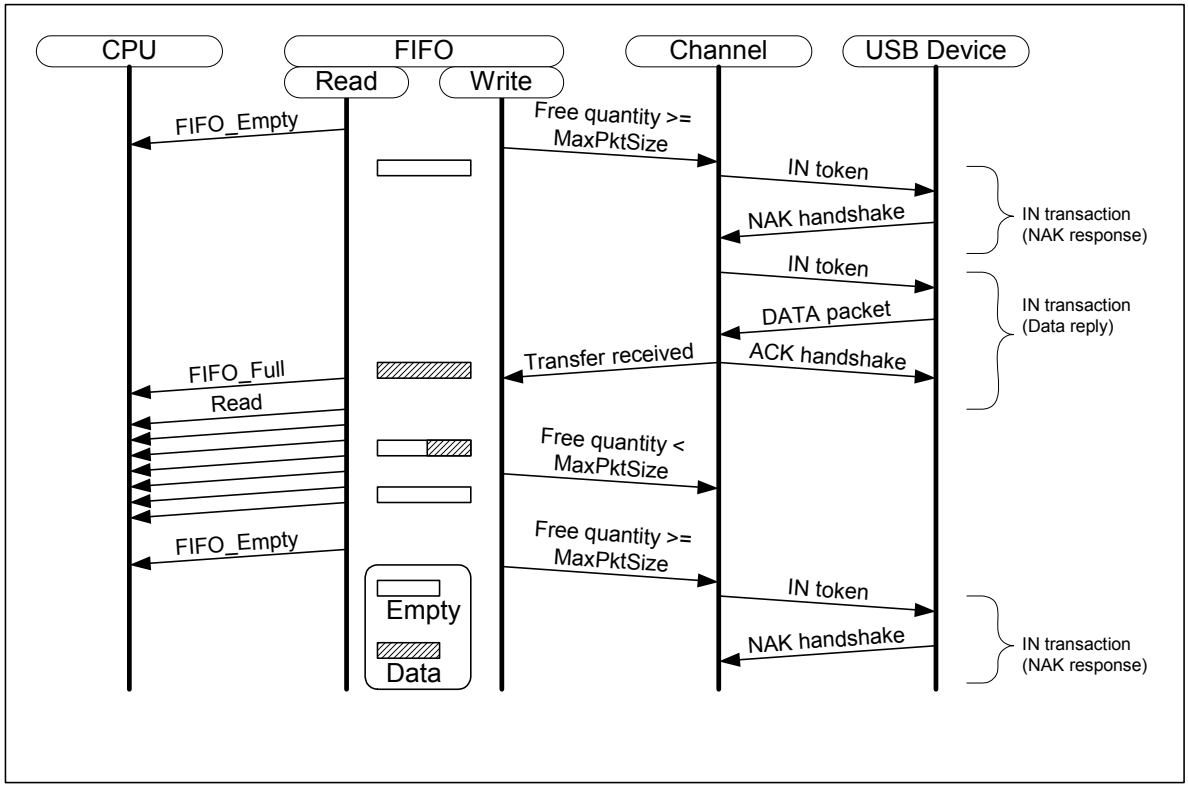


Figure 4-6 Typical data flow (with FIFO assigned for MaxPktSize and IN transfer)

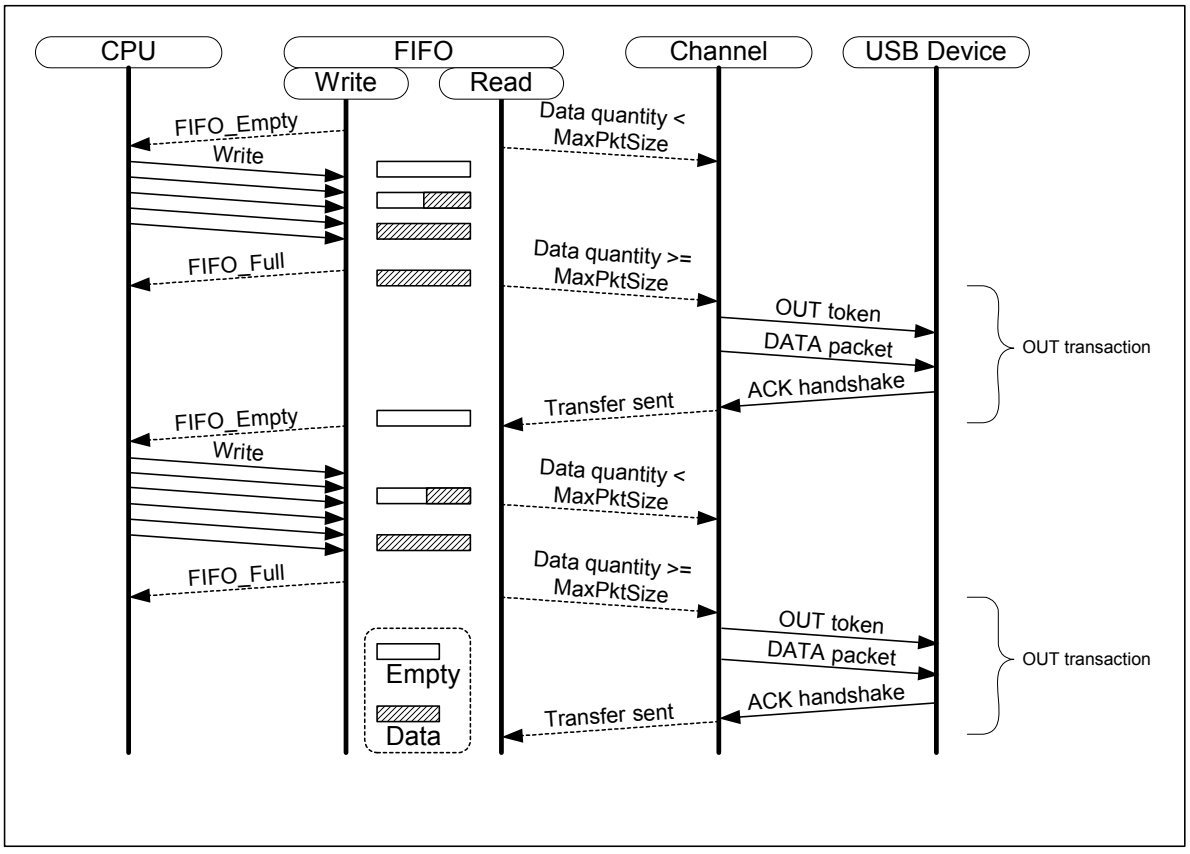


Figure 4-7 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfer)

4.7.4 USB Host Port External Circuits

The LSI ports have internal USB host termination resistors, including an HS termination resistor, eliminating the need for the external components normally used to adjust impedance. This allows a DP/DM line to be connected between the LSI terminal and the connector. Note that the appropriate components must be used to ensure static electricity protection and to implement EMI precautions.

An external VBUS control component is required for the VBUS.

4.8 FIFO

Each port on the LSI includes 4.5 kB of USB FIFO for use with USB data transfers. The USB FIFO capacity for each endpoint or channel can be assigned as desired using the register settings.

Transfers are possible between the USB-I/F and CPU-I/F via the USB FIFO.

5. Terminal Layout Diagrams

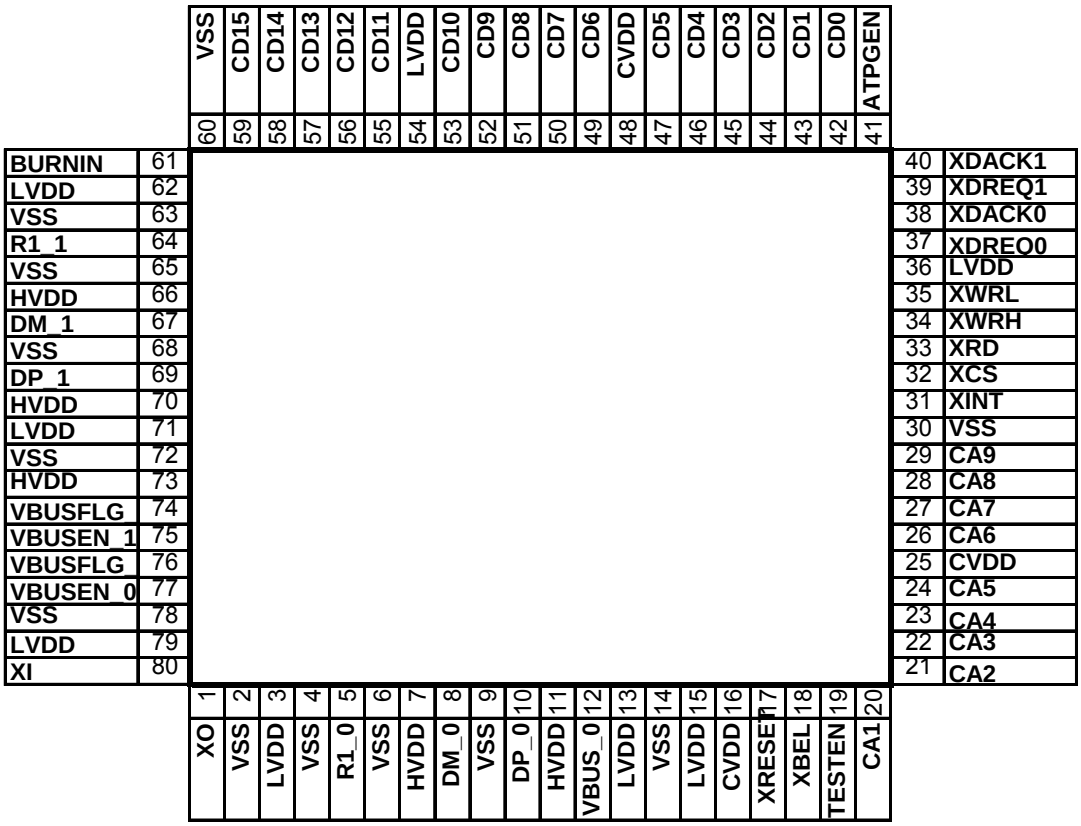


Figure 5-1 QFP package terminal layout diagram

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	XI	VSS	HVDD	LVDD	DP_1	DM_1	R1_1	LVDD	VSS	NC	A
B	XO	LVDD	VBUSFLG_0	VBUSFLG_1	VSS	HVDD	VSS	VSS	BURNIN	CD15	VSS	B
C	LVDD	VSS	VBUSEN_0	VBUSEN_1	VSS	VSS	VSS	VSS	VSS	CD14	CD13	C
D	R1_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CD12	CD11	D
E	DM_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CD9	CD10	LVDD	E
F	DP_0	HVDD	VBUS_0	VSS	VSS	VSS	VSS	VSS	CD6	CD7	CD8	F
G	LVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CD4	CD5	CVDD	G
H	VSS	LVDD	VSS	VSS	VSS	VSS	VSS	VSS	ATPGEN	CD2	CD3	H
J	CVDD	XRESET	TESTEN	CA5	CA9	XCS	XWRL	VSS	VSS	CD1	CD0	J
K	XBEL	CA1	CA3	CA6	CA7	XINT	XWRH	XDREQ0	XDREQ1	VSS	VSS	K
L	NC	CA2	CA4	CVDD	CA8	VSS	XRD	LVDD	XDACK0	XDACK1	NC	L
	1	2	3	4	5	6	7	8	9	10	11	

Top View

Figure 5-2 BGA package terminal layout diagram

6. Terminal Functions

OSC

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
80	A2	XI	IN	-	Analog	Internal oscillator circuit input (12 MHz, 24 MHz)
1	B1	XO	OUT	-	Analog	Internal oscillator circuit output

TEST

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
19	J3	TESTEN	IN	-	-	Test terminal (Set to Low)
41	H9	ATPGEN	IN	-	-	Test terminal (Set to Low)
61	B9	BURNIN	IN	-	-	Test terminal (Set to Low)

USB Port 0

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
5	D1	R1_0	IN	-	Analog	Internal operation reference current setting terminal (Connect 6.2 kΩ ±1% resistor between VSS)
10	F1	DP_0	BI	Hi-Z	Analog	USB port 0, data line (Data +)
8	E1	DM_0	BI	Hi-Z	Analog	USB port 0, data line (Data -)
76	B3	VBUSFLG_0	IN	(PU)	Schmitt (PU)	USB power switch fault detection signal (1: Normal, 0: Error)
77	C3	VBUSEN_0	OUT	Lo	2mA	USB power switch control signal
12	F3	VBUS_0	IN	(PD)	(PD)	USB device bus detection signal

PD: Pull Down

PU: Pull Up

USB Port 1

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
64	A8	R1_1	IN	-	Analog	Internal operation reference current setting terminal (Connect 6.2 kΩ ±1% resistor between VSS)
69	A6	DP_1	BI	Hi-Z	Analog	USB port 1, data line (Data +)
67	A7	DM_1	BI	Hi-Z	Analog	USB port 1, data line (Data -)
74	B4	VBUSFLG_1	IN	(PU)	Schmitt (PU)	USB power switch fault detection signal (1: Normal, 0: Error)
75	C4	VBUSEN_1	OUT	Lo	2mA	USB power switch control signal

PD: Pull Down

PU: Pull Up

CPU I/F

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description	
					Bus Mode ⇒	16bit Strobe mode	16bit BE mode
17	J2	XRESET	IN	-	-	Reset signal	
33	L7	XRD	IN	-	-	Read/strobe	
35	J7	XWRL (XWR)	IN	-	-	Write/strobe (lower)	Write/strobe
34	K7	XWRH (XBEH)	IN	-	-	Write/strobe (upper)	High-byte enable
32	J6	XCS	IN	-	-	Chip select signal	
31	K6	XINT	OUT	High	2mA (Tri-state)	Interrupt output signal	
37	K8	XDREQ0	OUT	High	2mA	Port 0 DMA request	
38	L9	XDACK0	IN	-	-	Port 0 DMA acknowledge	
39	K9	XDREQ1	OUT	High	2mA	Port 1 DMA request	
40	L10	XDACK1	IN	-	-	Port 1 DMA acknowledge	
18	K1	XBEL	IN	-	-	Set to High or Low	Low-byte enable
20	K2	CA1	IN	-	-	CPU bus address	
21	L2	CA2	IN	-	-		
22	K3	CA3	IN	-	-		
23	L3	CA4	IN	-	-		
24	J4	CA5	IN	-	-		
26	K4	CA6	IN	-	-		
27	K5	CA7	IN	-	-		
28	L5	CA8	IN	-	-		
29	J5	CA9	IN	-	-		
42	J11	CD0	BI	Hi-Z	2mA	CPU data bus	
43	J10	CD1	BI	Hi-Z	2mA		
44	H10	CD2	BI	Hi-Z	2mA		
45	H11	CD3	BI	Hi-Z	2mA		
46	G9	CD4	BI	Hi-Z	2mA		
47	G10	CD5	BI	Hi-Z	2mA		
49	F9	CD6	BI	Hi-Z	2mA		
50	F10	CD7	BI	Hi-Z	2mA		
51	F11	CD8	BI	Hi-Z	2mA		
52	E9	CD9	BI	Hi-Z	2mA		
53	E10	CD10	BI	Hi-Z	2mA		
55	D11	CD11	BI	Hi-Z	2mA		
56	D10	CD12	BI	Hi-Z	2mA		
57	C11	CD13	BI	Hi-Z	2mA		
58	C10	CD14	BI	Hi-Z	2mA		
59	B10	CD15	BI	Hi-Z	2mA		

The XINT terminal can be set to 1/0 or Hi-Z/0 mode, depending on register settings.

PD: Pull Down

PU: Pull Up

6. Terminal Functions

POWER

Pin	Ball	Name	Voltage	Terminal description
7, 11, 66, 70, 73	F2, B6, A4	HVDD	3.3V	USB I/O power supply
16, 25, 48	J1, L4, G11	CVDD	1.8 to 3.3 v	CPU I/F I/O power supply
3, 13, 15, 36, 54, 62, 71, 79	C1, G1, H2, L8, E11, A9, A5, B2	LVDD	1.8V	OSC I/O, TEST I/O, and internal power supply
2, 4, 6, 9, 14, 30, 60, 63, 65, 68, 72, 78	A3, A10, B5, B7, B8, B11, C2, C5, C6, C7, C8, C9, D2, D3, D4, D5, D6, D7, D8, D9, E2, E3, E4, E5, E6, E7, E8, F4, F5, F6, F7, F8, G2, G3, G4, G5, G6, G7, G8, H1, H3, H4, H5, H6, H7, H8, J8, J9, K10, K11, L6	VSS	0V	GND
-	A1, A11, L1, L11	N.C.	0V	NC terminal (connect to GND)

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	HVDD	VSS – 0.3 to 4.0	V
	CVDD	VSS – 0.3 to 4.0	V
	LVDD	VSS – 0.3 to 2.5	V
Input voltage	HVI	VSS – 0.3 to HVDD + 0.5	V
	CVI*1	VSS – 0.3 to CVDD + 0.5	V
	VVI*2	VSS – 0.3 to 6.0	V
	LVI*3	VSS – 0.3 to LVDD + 0.5	V
Output voltage	HVO	VSS – 0.3 to HVDD + 0.5	V
	CVO*1	VSS – 0.3 to CVDD + 0.5	V
Output current/terminal	IOUT	±10	mA
Storage temperature	Tstg	-65 to 150	°C

*1 CPU-IF

*2 VBUS_0

*3 XI, TESTEN, ATPGEN, BURNIN

7.2 Recommended Operating Conditions

Item	Symbol	MIN	TYP	MAX	Units
Power supply voltage	HVDD	3.00	3.30	3.60	V
	CVDD	1.65	-	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage	HVI	-0.3	-	HVDD+0.3	V
	CVI*1	-0.3	-	CVDD+0.3	V
	VVI*2	-0.3	-	6.0	V
	LVI*3	-0.3	-	LVDD+0.3	V
Ambient temperature	Ta	-40	25	85	°C

*1 CPU-I/F

*2 VBUS_0

*3 XI, TESTEN, ATPGEN, BURNIN

Turn on power to the IC in the sequence shown below.

LVDD (internal) → HVDD, CVDD (IO section)

Likewise, turn off power to the IC in the sequence shown below.

HVDD, CVDD (IO section) → LVDD (internal)

Note:
Avoid leaving the HVDD or CVDD on continuously (for more than 1 second) when the LVDD is off, as doing so may affect chip reliability.

7.3 DC Characteristics

7.3.1 Current Consumption

Item	Symbol	Condition	MIN	TYP	MAX	Units
Power supply feed current	*1					
Power supply current	IDDH	HVDD = 3.3V(typ), HVDD = 3.6V(max)	-	17.3	26.0	mA
	IDDCH	CVDD = 3.3V(typ), CVDD = 3.6V(max)	-	2.0	6.0	mA
	IDDCL	CVDD = 1.8V(typ), CVDD = 1.95V(max)	-	0.8	2.3	mA
	IDDL	LVDD = 1.8V(typ), LVDD = 1.95V(max)	-	60.9	92.0	mA
Stationary current	*2					
Power supply current	IDDS	VIN = HVDD,CVDD,LVDD or VSS HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V	-	-	40	μA
Input leakage						
Input leakage current	IL	HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V HVIH = HVDD CVIH = CVDD LVIH = LVDD VIL = VSS	-5	-	5	μA

*1: The “typ” values are measured when transferring data between two devices connected to each port of 72V18 working as USB Host.

*2: Stationary current with Ta = 25°C and both terminals in input mode.

Current consumption measurements for individual power management states using Seiko Epson operating conditions (Ta = 25°C)

Item	Condition	MIN	TYP	MAX	Units
CPU_Cut	CPU bus operation *1 *2				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	-	17	-	μW
SLEEP	CPU bus operation *1 *2				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	-	212	-	μW
ACTIVE/SLEEP (USB ⇔ CPU-I/F)	*3				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	-	101	-	mW
ACTIVE/ACTIVE (USB ⇔ CPU-I/F)	*4				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	-	172	-	mW

*1: When the CPU is accessing memory (e.g., SRAM or ROM) connected to the CPU bus.

*2: Excluding current consumption attributable to DP pull-up resistor inside S1R72V18 (approx. 200 μA).

*3: When transferring data connected to a PC as a USB device.

*4: With both ports transferring data between a memory connected to the CPU bus and USB-HDD with USB-HDD connected with the LSI as the USB host .

7.3.2 Input Characteristics

Item	Symbol	Condition	MIN	TYP	MAX	Units
Input characteristics (LVCMOS)	Terminal names: CA[8:1], CD[15:0], XCS, XRD, XWRL, XWRH, XBEL, XDACK_0, XDACK_1, XRESET					
H level input voltage	VIH2	CVDD = 3.6V	2.2	-	-	V
L level input voltage	VIL2	CVDD = 3.0V	-	-	0.8	V
H level input voltage	VIH3	CVDD = 1.95V	1.27	-	-	V
L level input voltage	VIL3	CVDD = 1.65V	-	-	0.57	V
Schmitt input characteristics	Terminal names: VBUSFLG_0, VBUSFLG_1					
H level trigger voltage	VT+	HVDD = 3.6V	1.4	-	2.7	V
L level trigger voltage	VT-	HVDD = 3.0V	0.6	-	1.8	V
Hysteresis voltage	ΔV	HVDD = 3.0V	0.3	-	-	V
Schmitt input characteristics (USB FS)	Terminal names: DP_0, DM_0, DP_1, DM_1					
H level trigger voltage	VT+(USB)	HVDD = 3.6V	1.1	-	1.8	V
L level trigger voltage	VT-(USB)	HVDD = 3.0V	1.0	-	1.5	V
Hysteresis voltage	ΔV(USB)	HVDD = 3.0V	0.1	-	-	V
Input characteristics (USB FS differential)	Terminal names: DP_0 + DM_0 pair, DP_1 + DM_1 pair					
Differential input sensitivity	VDS(USB)	HVDD = 3.0V Differential input voltage = 0.8 V to 2.5 V	-	-	0.2V	V
Input characteristics (VBUS)	Terminal name: VBUS_0					
H level trigger voltage	VT+(VBUS)	HVDD = 3.6V	1.86	-	2.85	V
L level trigger voltage	VT-(VBUS)	HVDD = 3.0V	1.48	-	2.23	V
Hysteresis voltage	ΔV(VBUS)	HVDD = 3.0V	0.31	-	0.64	V
Input characteristics	Terminal name: VBUS_0					
Pull-down resistor	RPLDV	VIH = 5.0V	110	125	150	kΩ

7.3.3 Output Characteristics

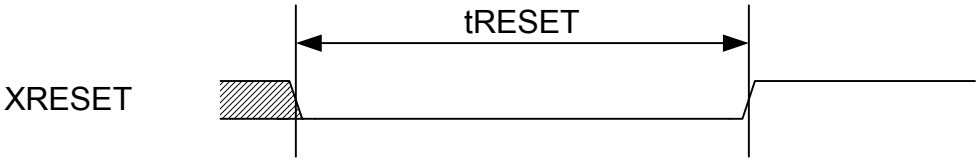
Item	Symbol	Condition	MIN	TYP	MAX	Units
Output characteristics	Terminal names: CD[15:0], XDREQ_0, XDREQ_1, XINT					
H level output voltage	VOH1	CVDD = 3.0V IOH = -2mA	CVDD-0.4	-	-	V
L level output voltage	VOL1	CVDD = 3.0V IOL = 2mA	-	-	VSS+0.4	V
H level output voltage	VOH2	CVDD = 1.65V IOH = -1mA	CVDD-0.4	-	-	V
L level output voltage	VOL2	CVDD = 1.65V IOL = 1mA	-	-	VSS+0.4	V
Output characteristics	Terminal names:VBUSEN_0, VBUSEN_1					
H level output voltage	VOH4	HVDD = 3.0V IOH = -2mA	HVDD-0.4	-	-	V
L level output voltage	VOL4	HVDD = 3.0V IOL = 2mA	-	-	VSS+0.4	V
Output characteristics (USB FS)	Terminal names: DP_0, DM_0, DP_1, DM_1					
H level output voltage	VOH(USB)	HVDD=3.0V	2.8	-	-	V
L level output voltage	VOL(USB)	HVDD=3.6V	-	-	0.3	V
Output characteristics (USB HS)	Terminal names: DP_0, DM_0, DP_1, DM_1					
H level output voltage	VHSOH (USB)	HVDD = 3.0V	360	-	-	mV
L level output voltage	VHSOL (USB)	HVDD = 3.6V	-	-	10.0	mV
Output characteristics	Terminal names: CD[15:0], XINT					
OFF-STATE leakage current	IOZ	CVDD = 3.6V CVOH = CVDD VOL = VSS	-5	-	5	μA

7.3.4 Terminal Capacitance

Item	Symbol	Condition	MIN	TYP	MAX	Units
Terminal capacitance	Terminal name: All input terminals					
Input terminal capacitance	CI	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8pF	pF
Terminal capacitance	Terminal name: All output terminals					
Output terminal capacitance	CO	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8pF	pF
Terminal capacitance	Terminal name: All input/output terminals (except DP_0, DM_0, DP_1, DM_1)					
Input/output terminal capacitance 1	CIO1	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8pF	pF
Terminal capacitance	Terminal names: DP_0, DM_0, DP_1, DM_1					
Input/output terminal capacitance 2	CIO2	f = 10MHz HVDD = CVDD = LVDD = VSS	-	-	8pF	pF

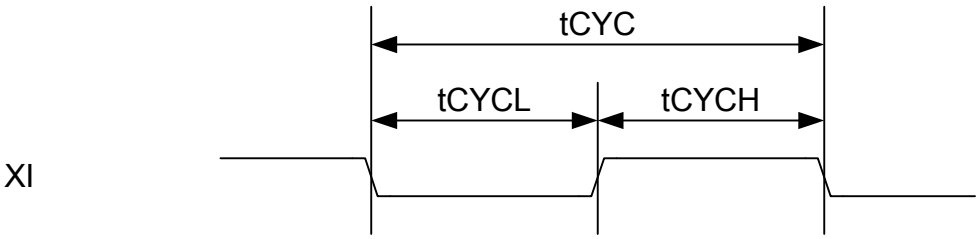
7.4 AC Characteristics

7.4.1 Reset Timing



Code	Description	min	typ	max	Units
tRESET	Reset pulse width	40	-	-	ns

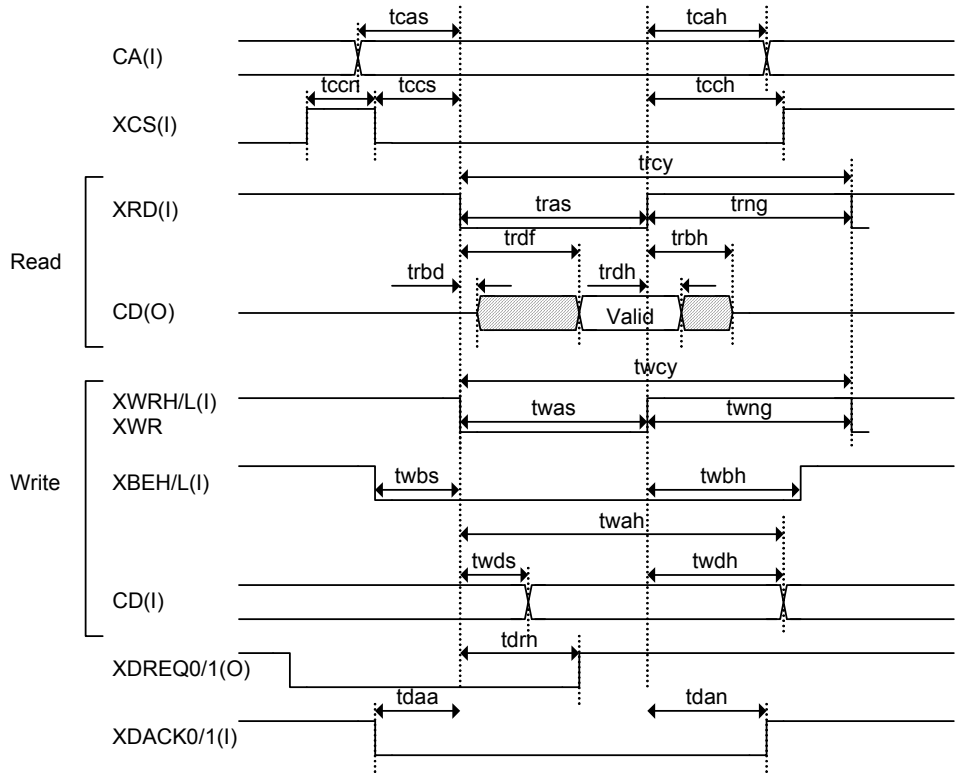
7.4.2 Clock Timing



Code	Description	min	typ	max	Units
tCYC	Clock cycle (ClkSelect=0)	11.999	12	12.001	MHz
tCYC	Clock cycle (ClkSelect=1)	23.998	24	24.002	MHz
tCYCH tCYCL	Clock duty	45	-	55	%

7.4.3 CPU/DMA I/F Access Timing

7.4.3.1 Specifications for CVDD = 1.65 V to 3.6 V

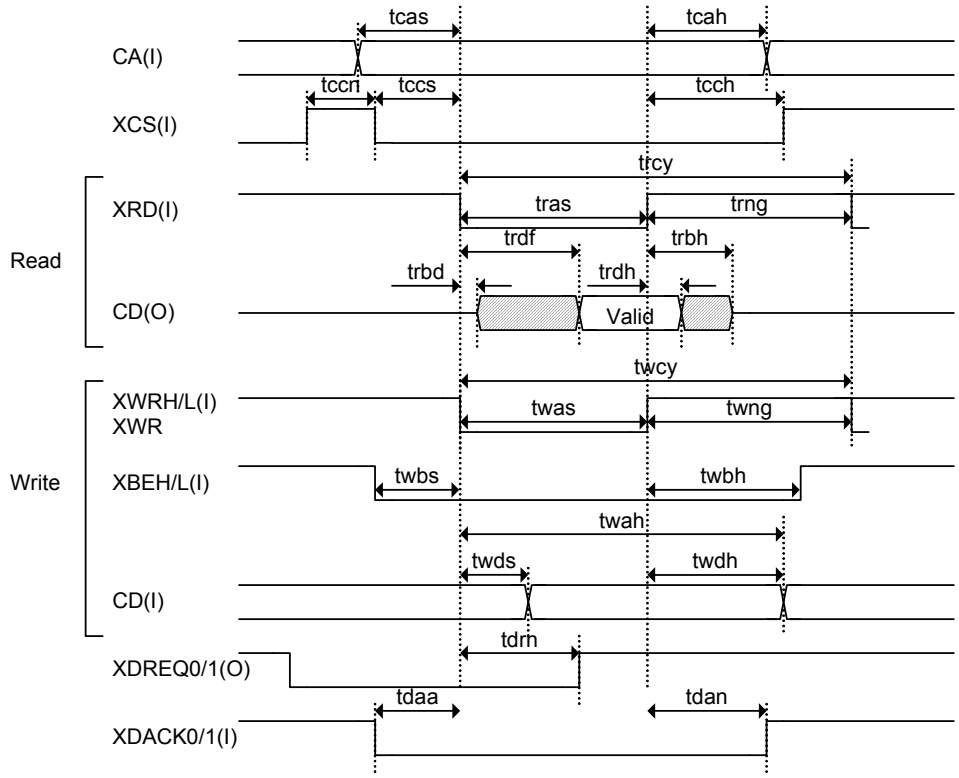


(C_L=30pF)

Code	Item	min	typ	max	unit
tcas	Address setup time	6	-	-	ns
tcah	Address hold time	6	-	-	ns
tccs	XCS setup time	6	-	-	ns
tcch	XCS hold time	6	-	-	ns
tccn	XCS negate time (for CPUIF mode only*)	15	-	-	ns
trcy	Read cycle	80	-	-	ns
tras	Read strobe assert time	45	-	-	ns
trng	Read strobe negate time	25	-	-	ns
trbd	Read data output start time	1	-	-	ns
trdf	Read data confirmation time	-	-	40	ns
trdh	Read data hold time	2	-	-	ns
trbh	Read data output delay time	-	-	10	ns
twcy	Write cycle	80	-	-	ns
twas	Write strobe assert time	45	-	-	ns
twng	Write strobe negate time	25	-	-	ns
twbs	Write byte enable setup time	6	-	-	ns
twbh	Write byte enable hold time	6	-	-	ns
twds	Write data delay acknowledge time	-	-	10	ns
twdh	Write data hold time (after strobe negation)	6	-	-	ns
twah	Write data hold time (after strobe assertion)	50	-	-	ns
tdrn	XDREQ0/1 negate delay time	-	-	35	ns
tdaa	XDACK0/1 setup time	6	-	-	ns
tdan	XDACK0/1 hold time	6	-	-	ns

* Refer to “Technical Manual” for details of CPUIF mode settings.

7.4.3.2 Specifications when limited to CVDD = 3.0 V to 3.6 V (relaxed specifications)



(C_L=30pF)

Code	Item	min	typ	max	unit
tcas	Address setup time	6	-	-	ns
tcah	Address hold time	6	-	-	ns
tccs	XCS setup time	6	-	-	ns
tcch	XCS hold time	6	-	-	ns
tccn	XCS negate time (for CPUIF mode only*)	15	-	-	ns
trcy	Read cycle	75	-	-	ns
tras	Read strobe assert time	40	-	-	ns
trng	Read strobe negate time	25	-	-	ns
trbd	Read data output start time	1	-	-	ns
trdf	Read data confirmation time	-	-	35	ns
trdh	Read data hold time	2	-	-	ns
trbh	Read data output delay time	-	-	10	ns
twcy	Write cycle	75	-	-	ns
twas	Write strobe assert time	40	-	-	ns
twng	Write strobe negate time	25	-	-	ns
twbs	Write byte enable setup time	6	-	-	ns
twbh	Write byte enable hold time	6	-	-	ns
twds	Write data delay acknowledge time	-	-	10	ns
twdh	Write data hold time (after strobe negation)	6	-	-	ns
twah	Write data hold time (after strobe assertion)	50	-	-	ns
tdrn	XDREQ0/1 negate delay time	-	-	30	ns
tdaa	XDACK0/1 setup time	6	-	-	ns
tdan	XDACK0/1 hold time	6	-	-	ns

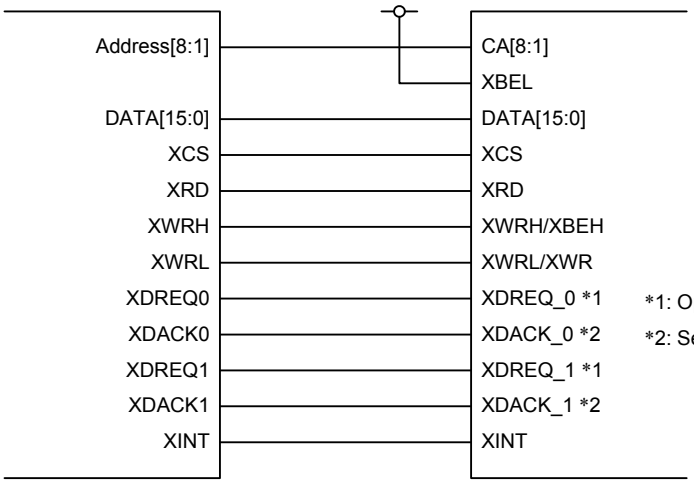
* Refer to “Technical Manual” for details of CPUIF mode settings.

7.4.4 USB I/F Timing

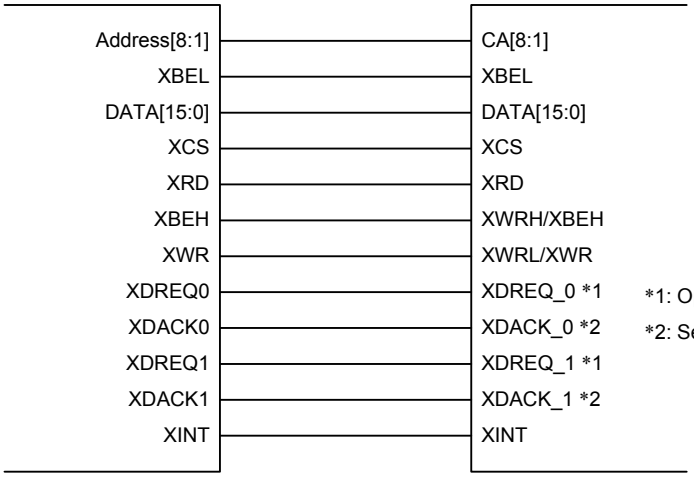
Complies with the USB 2.0 standard (Universal Serial Bus Specification Revision 2.0 Released on April 27, 2000).

8. Connection Examples

8.1 CPU I/F Connection Example



16-bit CPU (XWRH/XWRL) connection example



16-bit CPU (XBEH/XBEL) connection example

8.2 USB I/F Connection Example

Refer to the separately provided S1R72V Series USB 2.0 Hi-Speed PCB Design Guidelines.

9. Product Codes

Table 9-1 Product codes

Product code	Product type
S1R72V18B10****	PFBGA10UX121 package
S1R72V18F14****	QFP14-80 package

10. External Dimension Diagrams

Refer to the PFBGA10UX121 and QFP14-80 package drawings at the end of this document.

Revision History

Date	Revision details			
	Rev.	Page (old issue)	Type	Details
07/10/12	0.79	All pages	New	New issue
08/04/01	0.90	5	Revision	“The ChipReset.AllReset bit for each port is used to reset the LSI,” → “Correction)The ChipReset.AllReset bit initializes all circuits except the CPUIF_MODE register,”
		24	Revision	Added the rated value in cells previously commented as “T.B.D”
08/11/21	1.00	18,19	Revision	Added the rated value in cells previously commented as “T.B.D”
		18	Revision	“typ values are measured with the USB-HDD connected as the USB host and when transferring data between the IDE-HDD and USB-HDD” → “The “typ” values are measured when transferring data between two devices connected to each port of 72V18 working as USB Host”
		19	Revision	“With one port transferring data between a memory connected to the CPU bus and USB-HDD with USB-HDD connected with the LSI as the USB host” → “When transferring data connected to a PC as a USB device”
				Blank below this line

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