STA680

HD Radio™ baseband receiver

Preliminary data

Features

General

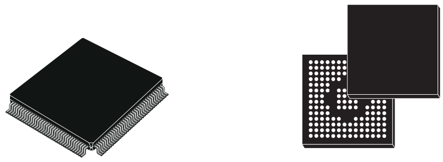
- HD Radio signal decoding for AM and FM digital audio
- Tensilica™ signal/audio processing core architecture running up to 166 MHz
- Hardware support for conditional access (one-time programmable 640-bit memory)
- 2 internal PLLs: processor cores and peripheral bus
- 1 Internal clock oscillator and external clock input
- 250 mW with core voltage of 1.2 V and IO voltage of 3.3 V
- Temperature range: -40 to +85 °C

Memories

- Internal boot ROM
- SDRAM controller addressing up to 512 Mbit of SDRAM in x16 configuration
- Serial Flash memory interface for application code loading

Turner interface

- Support of RF-IF peripheral processor (RIPP) and other front ends such as STA3004 and STA7506
- Input from RF front-end via programmable serial interface supporting 650 kS/s, 675 kS/s, 744.1875 kS/s, 882 kS/s, 912 kS/s sample rates
- Secondary RF front-end interface for dual tuner applications



LQFP144 (20x20x1.4 mm) **LFBGA 168 balls (12x12x1.4 mm)**

Other interfaces

- One stereo audio sample rate converter (44.1 kS/s, 45.6 kS/s, 48 kS/s)
- One input and three stereo channels audio output (by IIS serial audio interface)
- 2 IIC and 3 SPI serial interfaces
- 1 UART interface
- 1 GPIO interface (8 lines)
- SD/MMC interface via SPI
- JTAG interface

Supported HD Radio system capabilities

- Multicasting
- Program service data
- Real-time traffic
- Audio time shifting
- iTunes Tagging™
- Surround sound

Applications

- Car radio
- Personal navigation device (PND)
- Portable battery operated systems

Table 1. Device summary

Order code	Package(1)	Packing
STA680	LFBGA 168 balls (12x12x1.4 mm)	Tray
STA680Q	LQFP144 (20x20mm)	Tray

1. ECOPACK® compliant.

Contents

List of tables

List of figures

1 Description

The STA680 from STMicroelectronics is a system on a chip designed for demodulating and decoding of HD Radio[a] signals. The STA680 is compliant with the iBiquity specification and extends the possibility to implement new and optional features and to manage additional services.

The device combines it all into a single IC consisting of several hardware blocks and a programmable core to guarantee the proper level of flexibility, low current consumption and an optimized die size.

The STA680 implements the entire signal processing chain of an HD Radio receiver.

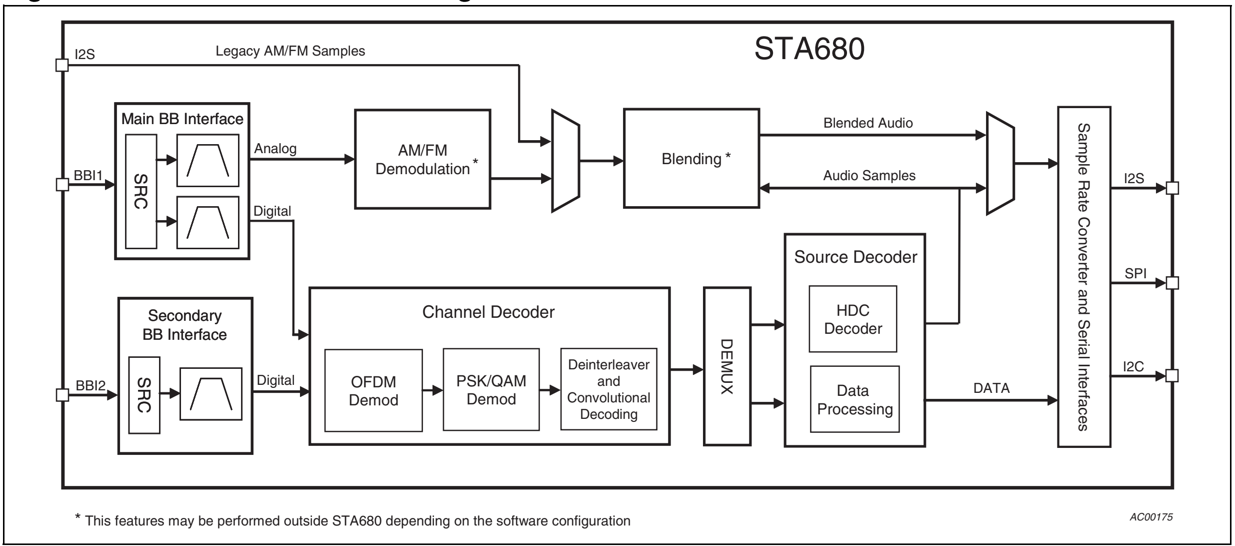
- The digital channel demodulation and decoding, including OFDM demodulation and error correction.
- Source decoding, consisting of audio and data decoding of the digital channel.
- The analog demodulator extracting the audio signal from the legacy analog AM/FM signal (can be implemented as an optional feature)
- The blending of the analog and digital audio signals

Figure 1 presents a functional diagram describing the data flow inside STA680 for HD Radio demodulating and decoding.

The architecture consists of an effective and balanced hardware/software implementation, to pursue the best combination in terms of current consumption, system flexibility and device cost.

Functional blocks which are standard, and computation intensive, are implemented using custom logic. Software implementation is more efficient for functional blocks where flexibility is needed. Such flexibility enables the STA680 to be ready for future evolution, and allows the implementation of specific and optional features.

Figure 1. Functional data flow diagram



a. HD Radio™ technology manufactured under license from iBiquity Digital Corp. U.S. and Foreign Patents. HD Radio™ and the HD Radio logo are proprietary trademarks of iBiquity Digital Corp.

2 HD Radio™ system

The HD Radio™ system, compliant with National Radio System Committee NSRC-5 standard, was developed by iBiquity Digital Corporation.

This system is designed to permit a smooth evolution from current (legacy) analog AM/FM radio to a fully digital in-band on-channel (IBOC) system. The HD Radio system delivers digital audio and data services to mobile, portable, and fixed receivers from terrestrial trasmitters in the existing medium frequency (MF) and very high frequency (VHF) radio bands. Broadcaster may continue to transmit analog AM and FM simultaneusly with the new, higher quality and more robust digital signal, allowing themselves and their listener to convert from legacy analog to digital radio while maintaining their current frequencies allocations.

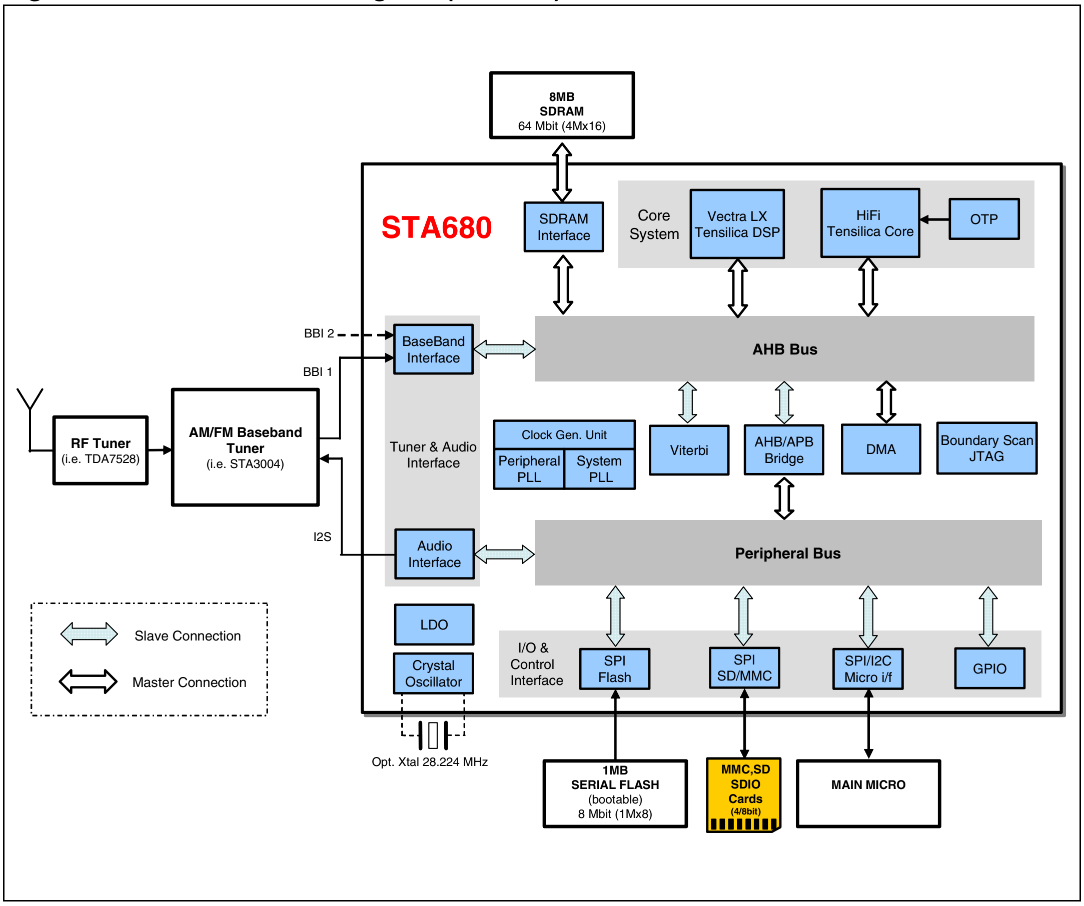
The HD Radio system is identified by the logo reported hereafter:

Figure 2. HD Radio™ system logo

3 Receiver system overview

Figure 3 shows the partitioning of the HD Radio receiver system, composed by an AM/FM RF front-end, IF channel signal processor and the HD Radio decoder (STA680).

Figure 3. STA680 block diagram (detailed)



The analog IF signal from the tuner front-end is digitized by a high-resolution sigma-delta A/D converter. A digital down-converter block, embedded into the IF channel signal processor, transforms the IF into a complex baseband signal. Its Bandwidth and sample rate have been adapted by filtering and decimation to match the specification of the HD Radio system. The complex baseband signal feed the HD Radio decoder (STA680) where the HD Radio stream is demodulated and decoded. The STA680 receives a digital baseband signal from the IF channel signal processor and returns the recovered audio and data services.

STA680 can be configured to work with digital IF baseband inputs based on standard front-ends. Front-ends must conform to HD Radio standards for filter bandwidth and linearity.

The STA680 requires external serial Flash memory to boot but can also be configured to boot from a host controller on IIC or SPI interfaces. The FLASH memory Is issued for program code and configuration data storage. STA680 needs SDRAM for bulk data storage required during the IBOC signal processing.

3.1 HD Radio processing

The STA680 HD Radio decoder does the processing of the IBOC signal. It receives a complex digital signal from an AM/FM IF channel signal processor. The native sample rate is 744.1875 kS/s for FM and 46.51171875 kS/s for AM. However, other input sample rates are acceptable because of the sample rate converter in the baseband Interface (BBI). These include: 650 kS/s, 675 kS/s, 882 kS/s and 912 kS/s. If a baseband signal is provided that is not at the native sample frequency of 744.1875 kHz it must be sample rate converted to this rate. Sample rate conversion hardware is provided on-chip to support this. This feature allows the STA680 to operate with various AM/FM front-ends.

The STA680is then responsible for detection, acquisition, and demodulation of the IBOC signal. Such function is primarily implemented by the Vectra DSP core. The demodulated signal is then passes to the Hi-Fi processor, for decoding, audio blending and handling of data services. A digital 44.1 kHz decompressed audio is output via the Digital Audio Interface.

The STA680 uses sophisticated algorithms to recover IBOC data even in the presence of signal impairments including fading and a variety of other interferences.

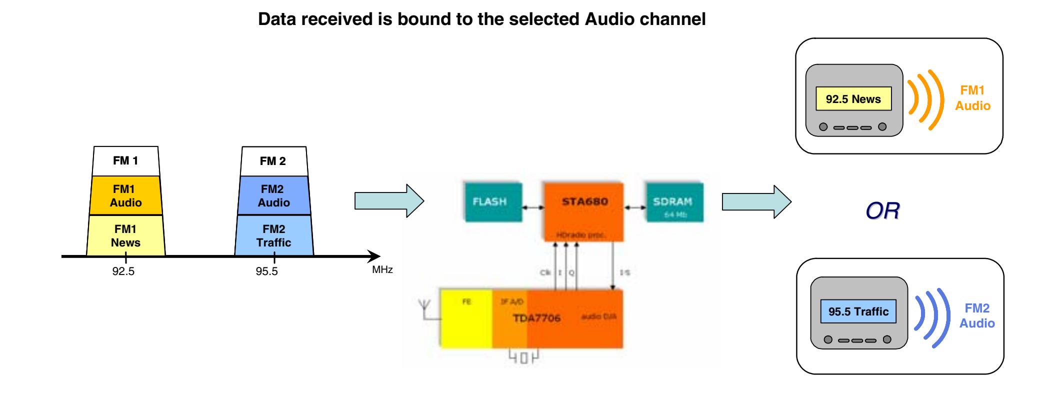
To process the HD Radio stream STA680 requires a 4M x16 external SDRAM (with up to 32M x16 supported) for data storage.

3.2 Dual stream HD Radio processing

STA680 is capable to simultaneously demodulate two different HD Radio streams. This unique feature enables the device to decode an HD Radio audio stream, in parallel with any data service broadcasted by a different radio channel. The implementation of the dual stream HD Radio processing requires that two AM/FM RF tuners are connected to the STA680.

In a single channel implementation a single RF tuner is used. In such configuration STA680 is able to demodulate at the same time both the audio and the data associated with the radio channel (i.e. 92.5 MHz or 102.5 MHz). This means that if the user sets the tuner 102.5 MHz, he or she can listed to FM2 audio and receive traffic information broadcasted on that channel. At the same time if the user tunes to another frequency (FM1), current traffic information will be lost.

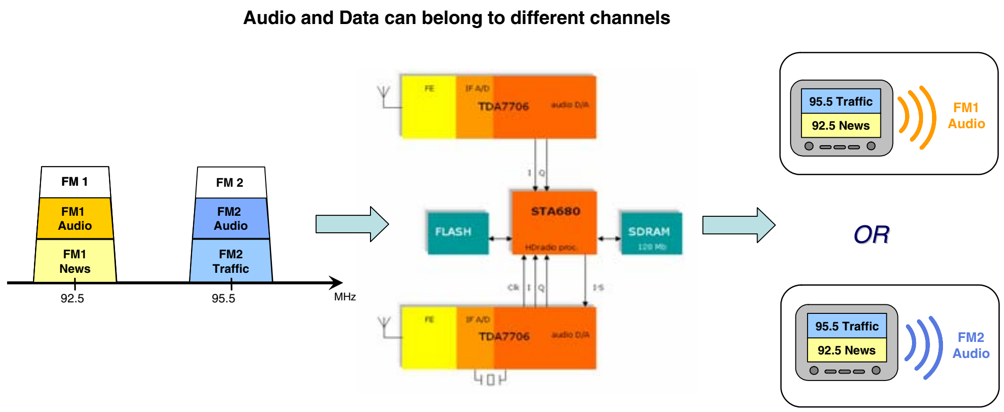
Figure 4. Single channel application



STA680 is able to demodulate both audio and data associated with a single radio channel. Example: While receiver is tuned to 99.5MHz, it is possible to simultaneously listen to audio content and receive traffic information associated with this channel.

In a dual channels implementation STA680 can simultaneously demodulate audio and data associated to different radio channels. This means that in the example above it would be still possible to receive traffic information broadcasted on FM2 (102.5 MHz) while listening FM1 audio program broadcasted on 92.5 MHz

Figure 5. Dual channel application



In this configuration, the system is able to simultaneously demodulate audio and data from the first radio channel ***plus*** *data from a second one. As a result STA680 can provide 1 audio and 2 data channels.*
Alternatively it is possible to receive audio content from one channel while pulling traffic or weather data from another at the same time.

3.3 Additional processing

The HD Radio stream demodulation and decoding take up only part of the computation power and memories resources available on STA680. This makes it possible to use the spare resources to implement additional features.

Depending on memory and computation power required by the additional features, it is possible to run them in parallel with the HD Radio stream decoding or in alternative, having all the hardware resources available for the additional features.

3.3.1 AM/FM processing

It is possible to implement legacy AM/FM processing in parallel with the HD Radio stream demodulation and decoding. Such solution is particularly suitable and appealing when the STA680 processor works jointly with an AM/FM RF front-end not incorporating the AM/FM demodulation.

3.3.2 Audio codec

STA680 can be used as a media processor to decode MP3/WMA audio stream. Thanks to the availability of the MMC and SD interface it is possible to reproduce an MP3 stream stored into any MMC or SD cards

3.3.3 Other

The spare computation power and memories are suitable to implement other specific algorithms or custom software application. For example sophisticated sound and audio processing could be implemented on the HD Radio decompressed audio. Audio output can be provided either in IIS master clock mode or in slave mode with the on-chip audio sample rate converter. Up to six audio channels may be provided in a standard configuration.

Another possibility is to implement on the STA680 the handling of data services.

3.4 Overview of main functional blocks

3.4.1 Adjacent channel filter

This module performs time domain filtering specifically for IBOC system. It receives a complex baseband IBOC signal input from SRC module and pre-conditions the signal for subsequent modem processing. The module is a front-end device.

3.4.2 HiFi2 core

The HiFi2 is a signal processing engine specifically designed to provide high quality 24-bit audio processing. The HiFi2 is also useful for advanced data applications such as storage and playback of received audio and conditional access processing. The HiFi2 leverages the Tensilica Xtensa LX engine with additional useful hardware capabilities such as:

- Specialized instructions for 24-bit Audio MAC & stream coding
- Dual MAC (each supports 24 x 24 and 32 x 16 bit format)
- Huffman Encode / Decode and truncate functions
- Two way SIMD arithmetic and Boolean operations

3.4.3 Vectra core

The Vectra LX is a powerful, configurable 32-bit RISC engine optimized for DSP with VLIW capabilities. The Vectra LX on board the STA680 includes eight MAC units, sixteen 160-bit vector operation registers, and a number of SIMD arithmetic instructions. Custom instructions in the Vectra are targeted for DSP applications such as filters and FFTs. The Vectra processor has been further configured with specific instructions for efficient performance on the HD Radio application.

3.4.4 DMA

A ten-channel DMA controller is attached to the AHB bus to allow the Vectra and HiFi2 processor cores to move large blocks of data efficiently. Certain channels are dedicated for use with certain hardware blocks because of hardware handshaking signals.

3.4.5 Hardware accelerator (VITERBI)

A complex convolutional Viterbi module is designed to fully comply with the HD Radio system. The module supports both K constant of 7 and 9, for IBOC digital FM and AM bands respectively.

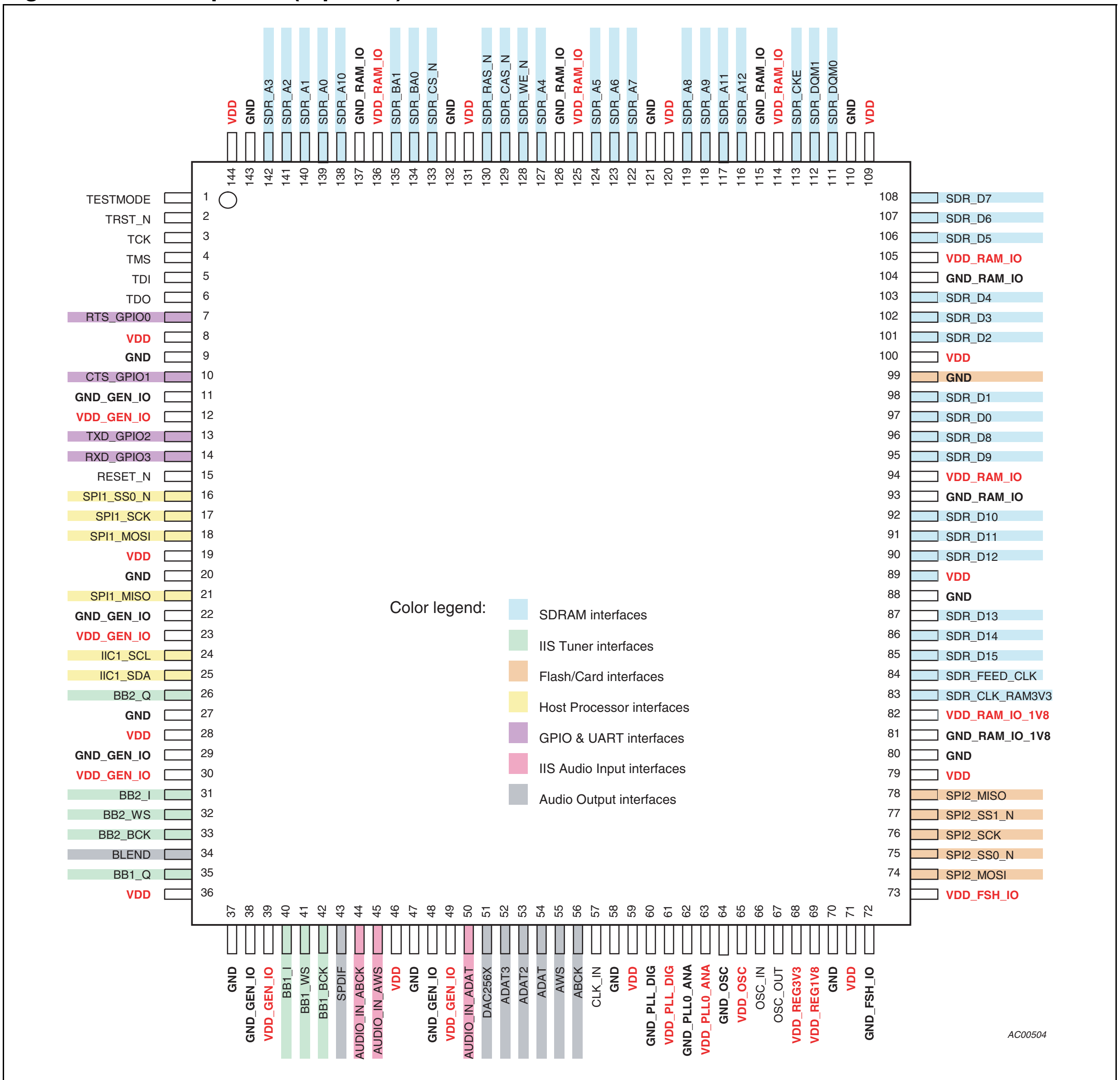
4 I/O description

The STA680 has two package options to suit different application needs. The first option is a 20x20mm LQFP package with 144 pins while the second one is a 12x12mm LFBGA with 169 balls and 0.8mm pitch.

4.1 LQFP description

Figure 6 presents the pinout of the STA680 for the LQFP package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 4.3*.

Figure 6. LQFP pinout (top view)



4.2 LFBGA description

Figure 7 presents the ballout of the STA680 for the LFBGA package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 4.3*.

Figure 7. LFBGA ballout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		GPIO6	BB2_BCK	BB2_I	GND_IO_GEN	IIC1_SDA	SPI1_MISO	SPI1_SCK	RESET_N	TXD_GPIO2	RTS_GPIO0	VDD_GEN_IO	TESTMODE	
B	GPIO5	BB1_Q	BLEND	BB2_WS	GND_IO_GEN	BB2_Q	IIC1_SCL	SPI1_MOSI	SPI1_SS0_N	RXD_GPIO3	CTS_GPIO1	VDD_GEN_IO	SDR_A3	TRST_N
C	BB1_WS	BB1_I	ADAT2	IIC2_SDA	GPIO7	IIC2_SCL	IIC1_DA	SPI3_MOSI	SPI3_MISO	SPI3_SCK	TDI	TCK	SDR_A1	SDR_A2
D	VDD_GEN_IO	VDD_GEN_IO	BB1_BCK	IIC2_DA	VDD	VDD			SPI3_SS_N	GPIO4	TDO	TMS	SDR_A10	SDR_A0
E	AUDIO_IN_ ABCK	SPDIF	ADAT3	VDD_PLL_DIG							VDD	MODEOP_FSH	SDR_BA0	SDR_BA1
F	AUDIO_IN_ ADAT	AUDIO_IN_ AWS	GND_PLL_ DIG	GND_PLL_ DIG		GND	GND	GND	GND		VDD	MODEOP_GEN	SDR_RAS_N	SDR_CS_N
G	AWS	ADAT	DAC256X			GND	GND	GND	GND			SDR_CAS_N	SDR_WE_N	VDD_RAM_IO
H	GND_IO_GEN	GND_IO_GEN	ABCK			GND	GND	GND	GND			SDR_A4	SDR_A5	GND_RAM_IO
J	VDD_OSC	GND_OSC	GND_PLL1_ ANA	GND_PLL0_ ANA		GND	GND	GND	GND		VDD	VDD	SDR_A7	SDR_A6
K	OSC_OUT	CLK_IN	VDD	VDD_REG3V3							VDD	VDD	SDR_A9	SDR_A8
L	OSC_IN	GND_OSC	VDD	VDD_REG3V3	VDD_FSH_IO	GND_FSH_IO			VDD_RAM_IO _1V8	GND_RAM_IO _1V8	GND_RAM_IO	GND_RAM_IO	SDR_A12	SDR_A11
M	VDD_PLL1_ ANA	VDD_PLL0_ ANA	SPI2_SS1_N	SPI2_SS2_N	SPI2_SS3_N	RFU	SDR_D13	SDR_D10	VDD_RAM_IO	VDD_RAM_IO	GND_RAM_IO	GND_RAM_IO	SDR_DQM1	SDR_CKE
N	VDD_REG1V8	VDD_REG1V8	SPI2_MOSI	SPI2_SCK	SDR_CLK_ RAM3V3	SDR_D15	SDR_D12	SDR_D9	SDR_D0	SDR_D2	SDR_D4	SDR_D6	SDR_DQM0	
P			SPI2_SS0_N	SPI2_MISO	SDR_FEED_ CLK	SDR_D14	SDR_D11	SDR_D8	SDR_D1	SDR_D3	SDR_D5	SDR_D7		

AC00707

Color legend:

Ball unused · Ball not present · SDRAM interfaces · IIS Tuner interfaces · Flash/Card interfaces · Host Processor interfaces · GPIO & UART interfaces · IIS Audio Input interfaces · Audio Output interfaces

4.3 Pin list

The *Table 2* briefly describes the main function and characteristics of the STA680 I/O signals in normal operation mode.

Table 2. Pins description

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Test							
1	A13	TESTMODE	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Factory test mode enable
Standard 1149.1 JTAG interface							
2	B14	TRST_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG active-low test reset
3	C12	TCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	JTAG test clock
4	D12	TMS	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG test mode state
5	C11	TDI	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	JTAG test data in
6	D11	TDO	O	-	1.8 V or 3.3 V	Generic IO supply	JTAG test data out
GPIO & UART interfaces							
7	A11	RTS_GPIO0	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART ready to send / GPIO bit 0
10	B11	CTS_GPIO1	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART clear to send / GPIO bit 1
13	A10	TXD_GPIO2	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART transmit data / GPIO bit 2
14	B10	RXD_GPIO3	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	UART receive data / GPIO bit 3
Not bonded	D10	GPIO4	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 4
Not bonded	B1	GPIO5	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 5
Not bonded	A2	GPIO6	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 6
Not bonded	C5	GPIO7	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	GPIO bit 7
Reset							
15	A9	RESET_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Device active-low reset

Table 2. **Pins description (continued)**

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Host processor interfaces							
16	B9	SPI1_SS0_N	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 active-low slave select
17	A8	SPI1_SCK	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial clock
18	B8	SPI1_MOSI	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial data master out/slave in
21	A7	SPI1_MISO	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 1 serial data master in/slave out
24	B7	IIC1_SCL	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 serial clock line
25	A6	IIC1_SDA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 serial data line
Not bonded	C7	IIC1_DA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 1 data acknowledged
Not bonded	C6	IIC2_SCL	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 2 serial clock line
Not bonded	C4	IIC2_SDA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 2 serial data line
Not bonded	D4	IIC2_DA	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	IIC interface 2 data acknowledged
IIS tuner interfaces							
40	C2	BB1_I	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface serial I data
35	B2	BB1_Q	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface serial Q data
41	C1	BB1_WS	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface word strobe
42	D3	BB1_BCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Primary baseband interface bit clock
31	A4	BB2_I	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface serial I data
26	B6	BB2_Q	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface serial Q data
32	B4	BB2_WS	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface word strobe
33	A3	BB2_BCK	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Secondary baseband interface bit clock

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
IIS audio input interface							
45	F2	AUDIO_IN_AWS	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio input word strobe
44	E1	AUDIO_IN_ABCK	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio input bit clock
50	F1	AUDIO_IN_ADAT	I	Pull-down	1.8 V or 3.3 V	Generic IO supply	Digital audio input serial data
Audio output interfaces							
55	G1	AWS	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio output word strobe
56	H3	ABCK	I/O	Pull-up	1.8 V or 3.3 V	Generic IO supply	Digital audio output clock
54	G2	ADAT	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output serial data
53	C3	ADAT2	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output serial data channel 2
52	E3	ADAT3	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output serial data channel 3
43	E2	SPDIF	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output in SPDIF format
34	B3	BLEND	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output blend output
51	G3	DAC256X	O	-	1.8 V or 3.3 V	Generic IO supply	Digital audio output oversampling clock
Clock & oscillator							
57	K2	CLK_IN	I	-	1.8 V or 3.3 V	Generic IO supply	Reference digital clock
66	L1	OSC_IN	ana	-	1.8 V	Osc supply	28,224MHz crystal in or digital clock input
67	L2	OSC_OUT	ana	-	1.8 V	Osc supply	Crystal output
SPI Flash interface							
78	P4	SPI2_MISO	I	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial data master in/slave out
74	N3	SPI2_MOSI	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial data master out/slave in
75	P3	SPI2_SS0_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 active-low slave select 0

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down[(1)]	Electrical	Supply group	Description
77	M3	SPI2_SS1_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 active-low slave select 1
Not bonded	M4	SPI2_SS2_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 active-low slave select 2
Not bonded	M5	SPI2_SS3_N	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 active-low slave select 3
76	N4	SPI2_SCK	O	Pull-up	1.8 V or 3.3 V	Flash IO supply	SPI interface 2 serial clock
SPI SD/MMC interface							
Not bonded	C9	SPI3_MISO	I	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 3 serial data master in/slave out
Not bonded	C8	SPI3_MOSI	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 3 serial data master out/slave in
Not bonded	D9	SPI3_SS_N	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 3 active-low slave select
Not bonded	C10	SPI3_SCK	O	Pull-up	1.8 V or 3.3 V	Generic IO supply	SPI interface 3 serial clock
SDRAM interface							
84	P5	SDR_FEED_CLK	I	-	3.3 V	SDRAM IO supply	Feedback clock from SDRAM interface
83	N5	SDR_CLK_RAM 3V3	O	-	3.3 V	SDRAM IO supply	Clock to SDRAM for 3.3 V interface
97	N9	SDR_D0	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 0
98	P9	SDR_D1	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 1
101	N10	SDR_D2	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 2
102	P10	SDR_D3	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 3
103	N11	SDR_D4	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 4
106	P11	SDR_D5	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 5
107	N12	SDR_D6	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 6
108	P12	SDR_D7	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 7
96	P8	SDR_D8	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 8

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
95	P9	SDR_D9	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 9
92	M8	SDR_D10	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 10
91	P7	SDR_D11	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 11
90	N7	SDR_D12	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 12
87	M7	SDR_D13	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 13
86	P6	SDR_D14	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 14
85	N6	SDR_D15	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 15
111	N13	SDR_DQM0	O	-	3.3 V	SDRAM IO supply	Low-byte data input/output mask
112	M13	SDR_DQM1	O	-	3.3 V	SDRAM IO supply	High-byte data input/output mask
128	G13	SDR_WE_N	O	-	3.3 V	SDRAM IO supply	Active-low write enable
129	G12	SDR_CAS_N	O	-	3.3 V	SDRAM IO supply	Active-low column address strobe
130	F13	SDR_RAS_N	O	-	3.3 V	SDRAM IO supply	Active-low row address strobe
113	M14	SDR_CKE	O	-	3.3 V	SDRAM IO supply	Clock enable
133	F14	SDR_CS_N	O	-	3.3 V	SDRAM IO supply	Active-low chip select
134	E13	SDR_BA0	O	-	3.3 V	SDRAM IO supply	Bank select address 0
135	E14	SDR_BA1	O	-	3.3 V	SDRAM IO supply	Bank select address 1
139	D14	SDR_A0	O	-	3.3 V	SDRAM IO supply	Address bit 0 to SDRAM
140	C13	SDR_A1	O	-	3.3 V	SDRAM IO supply	Address bit 1 to SDRAM
141	C14	SDR_A2	O	-	3.3 V	SDRAM IO supply	Address bit 2 to SDRAM
142	B13	SDR_A3	O	-	3.3 V	SDRAM IO supply	Address bit 3 to SDRAM

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
127	H12	SDR_A4	O	-	3.3 V	SDRAM IO supply	Address bit 4 to SDRAM
124	H13	SDR_A5	O	-	3.3 V	SDRAM IO supply	Address bit 5 to SDRAM
123	J14	SDR_A6	O	-	3.3 V	SDRAM IO supply	Address bit 6 to SDRAM
122	J13	SDR_A7	O	-	3.3 V	SDRAM IO supply	Address bit 7 to SDRAM
119	K14	SDR_A8	O	-	3.3 V	SDRAM IO supply	Address bit 8 to SDRAM
118	K13	SDR_A9	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
138	D13	SDR_A10	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
117	L14	SDR_A11	O	-	3.3 V	SDRAM IO supply	Address bit 11 to SDRAM
116	L13	SDR_A12	O	-	3.3 V	SDRAM IO supply	Address bit 12 to SDRAM
Supplies							
Not bonded	F12	MODEOP_GEN	I	Pull-up	3.3 V	SDRAM IO supply	Define the opereting voltage of the "Generic I/O" supply group. If tied low the I/Os work at 1.8V else they work at 3.3V. Default value is 3.3V.
Not bonded	E12	MODEOP_FSH	I	Pull-up	3.3 V	SDRAM IO supply	Define the opereting voltage of the "Flash I/O" supply group. If tied low the I/Os work at 1.8V else they work at 3.3V. Default value is 3.3V.
8, 19, 28, 36, 46, 59, 71, 79, 89, 100, 109, 120, 131, 144	D5, D6, E11, F11, J11, J12, K3, K11, K12, L3	VDD	n/a	-	1.2 V	Core supply	Power supply for core logic

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
9, 20, 27, 37, 47, 58, 70, 80, 88, 99, 110, 121, 132, 143	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	GND	n/a	-	-	Core supply	Ground for core logic
11, 22, 29, 38, 48	A5, B5, H1, H2	GND_GEN_IO	n/a	-	-	Generic IO supply	Generic I/Os ground
12, 23, 30, 39, 49	A12, B12, D1, D2	VDD_GEN_IO	n/a	-	1.8 V or 3.3 V	Generic IO supply	Generic I/Os power supply
72	L6	GND_FSH_IO	n/a	-	-	Flash IO supply	Ground for Flash Interface I/Os
73	L5	VDD_FSH_IO	n/a	-	1.8 V or 3.3 V	Flash IO supply	Power supply for Flash Inteface I/Os
93, 104, 115, 126, 137	H14, L11, L12, M11, M12	GND_RAM_IO	n/a	-	-	SDRAM IO supply	Ground for SDRAM Interface I/Os
94, 105, 114, 125, 136	G14, M9, M10	VDD_RAM_IO	n/a	-	3.3 V	SDRAM IO supply	Power supply for SDRAM Interface I/Os
60	F3, F4	GND_PLL_DIG	n/a	-	-	PLL digital supply	Ground for PLL digital part
61	E4	VDD_PLL_DIG	n/a	-	1.2 V	PLL digital supply	Power supply for PLL digital part
62	J4	GND_PLL0_ANA	n/a	-	-	PLL analog supply	Ground for PLL0 analog part (2)
62	J3	GND_PLL1_ANA	n/a	-	-	PLL analog supply	Ground for PLL1 analog part (2)

Table 2. Pins description (continued)

Pin #	Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
63	M2	VDD_PLL0_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL0 analog part(3)
63	M1	VDD_PLL1_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL1 analog part (3)
64	J2, L2	GND_OSC	n/a	-	-	Osc supply	Ground for oscillator core
65	J1	VDD_OSC	n/a	-	1.8 V	Osc supply	Power supply for oscillator core
68	K4, L4	VDD_REG3V3	n/a	-	3.3 V	LDO supply	Voltage regulator input power supply@3.3 Volt
69	N1, N2	VDD_REG1V8	n/a	-	1.8 V	LDO supply	Voltage regulator output power supply@1.8 Volt
82	L9	VDD_RAM_IO _1V8	n/a	-	1.8 V	n/a	Reserved - connect to 1.8 V supplyt
81	L10	GND_RAM_IO _1V8	n/a	-	-	n/a	Reserved - Connect to ground
Others							
Not bonded	M6	RFU	n/a	-	n/a	n/a	Reserved for future use - do not connect

1. Each input pin has a pull-up/down resistor to its default value. Unless otherwise specified, unused pins can be left unconnected after verifying that the impedance value of the pull-up/down resistor (see *Table 22*) is sufficient to guarantee noise immunity in user application environment.
2. In the LQFP package GND_PLL0_ANA and GND_PLL1_ANA are bonded together.
3. In the LQFP package VDD_PLL0_ANA and VDD_PLL1_ANA are bonded together.

4.4 I/Os supply groups

The STA680 I/O signals are arranged into three different supply groups: Generic IO supply, Flash IO supply and SDRAM IO supply group (see *Table 2*).

In the LQFP package option all three groups must be supplied with 3.3 V.

In the LFBGA package the three supply groups can independently operate at 3.3 V or 1.8 V.

- The SDRAM_IO supply group must always be supplied at 3.3 V.
- The MODEOP_GEN pin selects the operating voltage of the Generic_IO supply group. If it is shorted to ground then all the I/O signals belonging to the Generic_IO supply group will work at 1.8 V; if the MODEOP_GEN pin is left floating or it is tied high (3.3 V) all the group I/Os will operate at 3.3 V.
- The MODEOP_FSH pin selects the operating voltage of the Flash_IO supply group. If it is shorted to ground then all the I/O signals belonging to the Flash_IO supply group will work at 1.8 V; if the MODEOP_FSH pin is left floating or it is tied high (3.3 V) the Flash Interface I/Os will operate at 3.3 V.

5 Operation and general remarks

5.1 Clock schemes

The STA680 needs an external clock source to feed the internal Phase Locked Loops (PLLs) to generate all the frequency needed by its cores and peripherals. This reference clock may be supplied in several ways thus offering flexibility in the development of the final application:

- The reference clock may be supplied through the use of an external crystal or as a digital signal coming from an external IC.
- The reference clock may have different frequencies and can be fed to the STA680 through different input pins.

The selection of the clock input mode is performed during the power-on phase of the device by latching the value of the pins ADAT3, BLEND and DAC256X on the rising edge of the RESET_N signal (see *Chapter 5.2*); this value shall be selected according to *Table 3*.

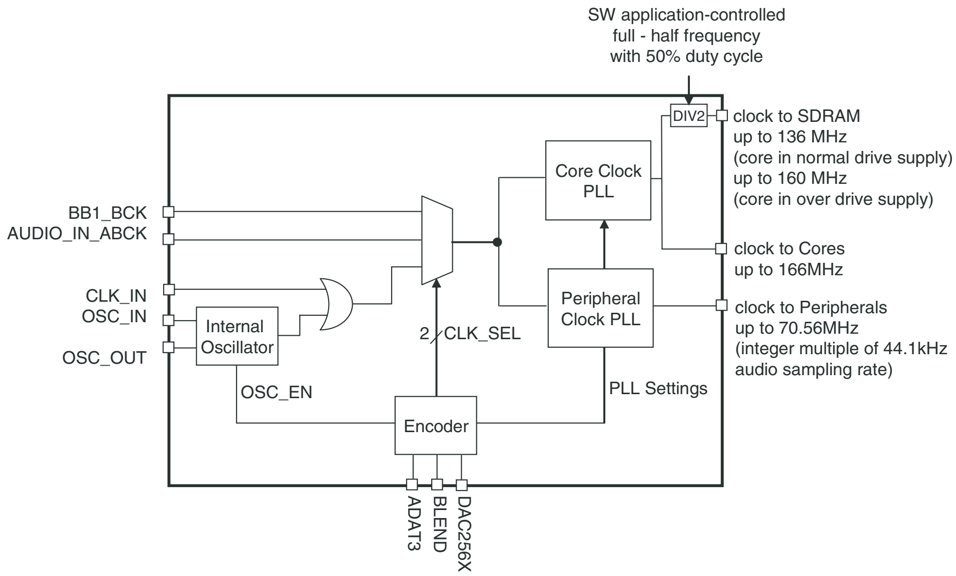
Table 3. Reference clock configuration

[ADAT3, BLEND, DAC256X]	Clock type	Input pin	Clock frequency (MHz)
[0,0,0] (1)	Crystal	OSC_IN	28.224
[0,0,1]	Digital	OSC_IN or CLK_IN (2)	23.3472
[0,1,0]	Digital	OSC_IN or CLK_IN (2)	36.48
[0,1,1]	Digital	OSC_IN or CLK_IN (2)	2.9184
[1,0,0]	Digital	BB1_BCK	10.4
[1,0,1]	Digital	BB1_BCK	10.8
[1,1,0]	Digital	BB1_BCK	14.112
[1,1,1]	Digital	AUDIO_IN_ABCK	2.9184

1. Default setting.
2. When using OSC_IN pin to input the reference clock the CLK_IN pin must be connected to ground and vice versa.

Figure 8 shows a simplified version of the internal clock generation unit.

Figure 8. Clock generation unit



Some remarks on the choice of the clock input pin must be done:

- OSC_IN is always a 1.8 V input pin.
- CLK_IN, BB1_BCK and AUDIO_IN_ABCK are 3.3 V pins when the LQFP package is selected while they can be configured as a 3.3 V or 1.8 V pins if the LFBGA is chosen (see *Chapter 4.4*)
- When the clock is fed through CLK_IN pin, the OSC_IN pin must be connected to ground. Similarly if the clock is fed using CLK_IN pin then the OSC_IN pin must be connected to ground.
- The BB1_BCK pin is the bit clock of the digital interface to the baseband Tuner, so to fed the reference clock through this pin the selected clock frequency must be chosen accordingly to the Primary baseband Interface settings (see *Chapter 6.2*):
  - 10.4 MHz = 16 * 2 * 650 kHz → BBI set to 650 Ksample/s
  - 10.8 MHz = 16 * 2 * 675 kHz → BBI set to 675 Ksample/s
  - 14.112 MHz = 16 * 2 * 882 kHz → BBI set to 882 Ksample/s
- The AUDIO_IN_ABCK is the bit clock of the digital audio input interface to the Tuner. When this pin is selected as clock source the STA680 Input Serial Audio Interface (see *Chapter 6.3.2*) must be set according to following specification:
  - Slave mode
  - Input sample rate = 45.6 kHz
  - Word length = 32 bit

With this settings the reference clock frequency is 2.9184 MHz = 32 * 2 * 45.6 kHz.

5.2 Power on

This chapter describes the power-on procedure for the cold start (cold start means that the device is completely disconnected from the power supply before being turned on). *Figure 9* and *Table 4* show the timing for the power up sequence of the cold start.

Figure 9. Power on timing

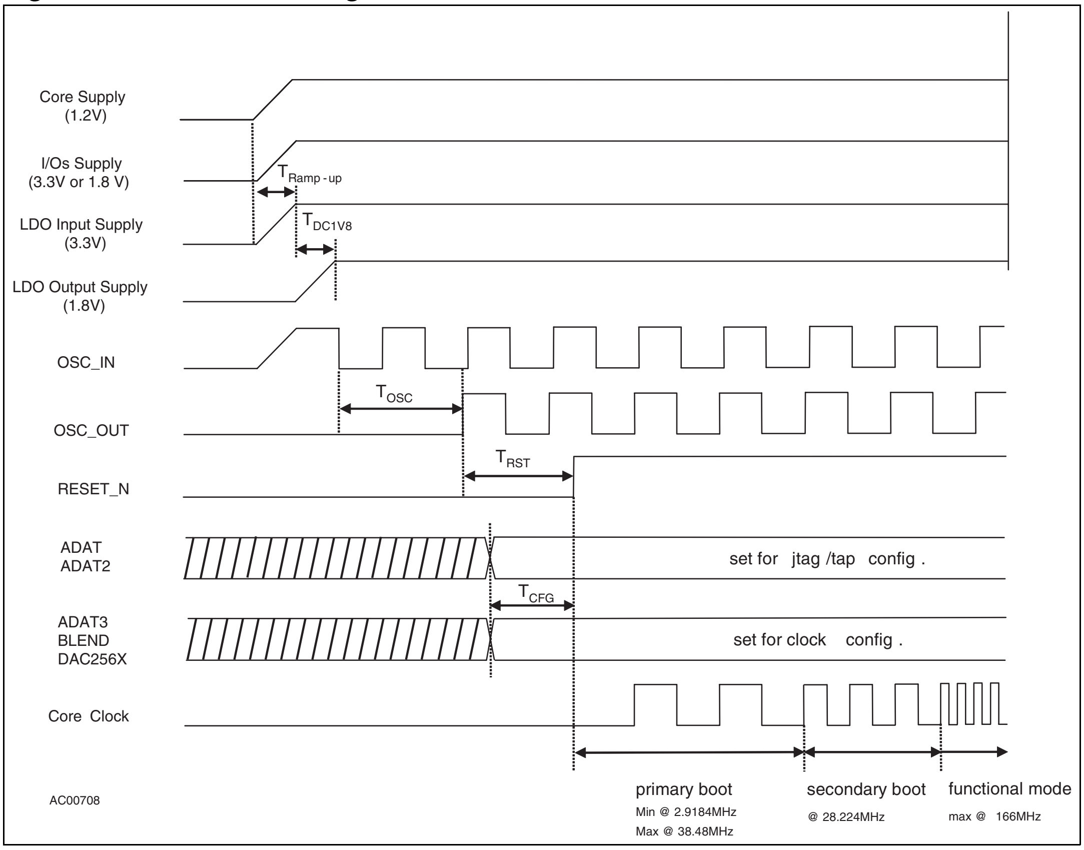
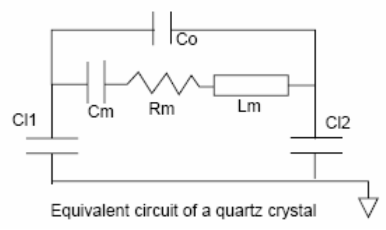


Table 4. Power on timing parameters

Symbol	Parameter	Min	Max	Unit
$T_{ramp\text{-}up}$	External supply ramp-up time	Same ramp-up time for 3.3 V and 1.2 V supply		-
T_{DC1V8}	DC1V8 regulator start-up time	-	1	ms
T_{OSC}(1)	Oscillator start-up time	-	400	µs
T_{RST}	Reset release time	10	-	µs
T_{CFG}	Setup of clock/jtag configuration	0.1	-	µs

1. Oscillator start-up time depends on the crystal connected to the internal oscillator. The given value is estimated for a crystal with these characteristics:

Figure 10. Crystal characteristics



MODEL	
Rm	50 Ohm
Lm	1.33 mH
Cm	26fF
CO	7pF
Cl=Cl1=Cl2	38pF (33pF+5pF parasitic)

5.2.1 Power supply ramp up phase

All power supplies must be ramped-up to their specified levels within the time $T_{Ramp-up}$, set by the external power supply circuit on the board. The ramp up phase of each power domain should start at the same time.

The RESET_N pin must be kept low since the beginning. For normal applications, the TESTMODE pin (Factory test mode enable, see *Table 2*) must be connected to ground.

5.2.2 Oscillator setting time

Once the power supply has reached the operating level, the internal voltage regulator gets functional after T_{DC1V8} = 1 s (see *Table 4*) and starts supplying the 1.8 V voltage to internal IPs such as PLLs and Crystal Oscillator.

The PLL is powered up but not yet functioning since the internal logic keeps it in bypass mode until a stable clock is available and STA680 has entered the secondary boot phase.

As shown in *Figure 9*, if an external crystal is connected to the internal oscillator this will output a correct waveform after T_{OSC} = 400 µs (see *Table 4*).

At this time, if no crystal is used, a digital clock must be supplied according to the instructions detailed in *Section 5.1*.

Either if an external crystal is used or the reference clock is provided through a digital source, the RESET_N pin must be kept low for an additional T_{RST} = 1.1 µs.

As described in *Section 5.1* the internal clock configuration is defined latching on the rising edge of the RESET_N signal the value of the pins ADAT3, BLEND and DAC256X; the value of this three signals must be stable at least T_{CFG} = 0.1 µs before the leading edge of the RESET_N signal.

5.2.3 Boot sequence

Once the RESET_N signal has been released and the power up sequence correctly performed, the STA680 enters the boot procedure, which consists of two phases consisting of device setup and application authentication and download.

During the first phase the STA680 executes the on-chip primary boot code contained in the 32 kilobyte Boot ROM. The primary boot synchronizes the internal cores, initializes the SPI and IIC interfaces and automatically selects the secondary boot code source by searching a pre-defined pattern into UART1, Flash, SPI1, IIC1 and IIC2.

Once the device on which the secondary boot resides has been found, following tasks are performed: the code is authenticated, the SDRAM is initialized and the secondary boot code is downloaded into it.

The downloading speed depends on the device reference clock frequency even if this parameter does not have a big impact on the overall boot time since the dimension of this part of the code is small.

During the second phase of the boot procedure to achieve acceptable boot time the STA680 performs PLLs setup and takes the internal clock frequency to 28.224 MHz (see *Figure 9*) then downloads and validates the application code from the external Flash memory. This last task ends the boot procedure.

5.2.4 Normal operation mode

After the execution of the boot code, the device enters the normal operation mode by jumping to the main program loop.

6 Digital I/O and memory interfaces

6.1 Interfaces: LQFP vs. LFBGA

The STA680 interface set depends on the package option selected, the LFBGA giving the maximum flexibility where the LQFP package has a slightly smaller set of interfaces, due to its smaller pin count.

The differences between the two package options are detailed in *Table 5*.

Table 5. Interface list

Interface name	Direction	LQFP	LFBGA
Baseband interface 1	I	✓	✓
Baseband interface 2 (data only)	I	✓	✓
I^2S audio input	I	✓	✓
I^2S audio output (six channels)	O	✓	✓
I^2C primary interface (Micro)	I/O	✓	✓
I^2C secondary Interface	I/O	x	✓
SPI micro interface	I/O	✓	✓
SPI Flash interface (double chip select)	I/O	✓	✓
SPI Flash interface extension (up to 4 chip select)	I/O	x	✓
SPI SD/MMC	I/O	x	✓
SDRAM interface	I/O	✓	✓
S/PDIF interface	O	✓	✓
UART interface	I/O	✓	✓
4 GPIO lines	I/O	x	✓
JTAG test interface (boundary scan only)	I/O	✓	✓

6.2 Tuner interface

The STA680 provides two digital baseband interfaces, named BBI1 and BBI2, through which the demodulated IBOC signals can enter the HD Radio decoder. The baseband Tuner accepts the analog signal from the RF Tuner, samples it, performs down conversion and filtering, and sends the zero-IF signal across a baseband interface (BBI) to the STA680.

Using two interfaces the STA680 is able to decode two channels at the same time, allowing the implementation of features such as the background scanning of HD Radio channels in search of traffic or weather information.

The BBI consists of four-wires, 16 bit wide I and Q data and two clocks. MSB is always transmitted first. All signals are assumed to be zero-if.

The native rate for FM is 744.1875 kS/s and for AM it is 46.51171875 kS/s. Sample rates of 650 kS/s, 675 kS/s, 882 kS/s and 912 kS/s are acceptable via the use of a sample rate converter.

BBI2 is similar to BBI1 except BBI2 doesn't have center filter so it is intended to be used for digital modulated signal only. For pin description refers to the *Table 5*.

Table 6. Baseband interfaces pin list

Pin name	Designation	Type	Drive
BB1_WS	Secondary base band interface word strobe	I	-
BB1_BCK	Primary baseband interface bit clock	I	-
BB1_I	Primary baseband interface serial I data	I	-
BB1_Q	Primary baseband interface serial Q data	I	-
BB2_WS	Secondary baseband interface word strobe	I	-
BB2_BCK	Secondary baseband interface bit clock	I	-
BB2_I	Secondary baseband interface serial I data	I	-
BB2_Q	Secondary baseband interface serial Q data	I	-

The data stream of the baseband interface varies depending on the mode selected.

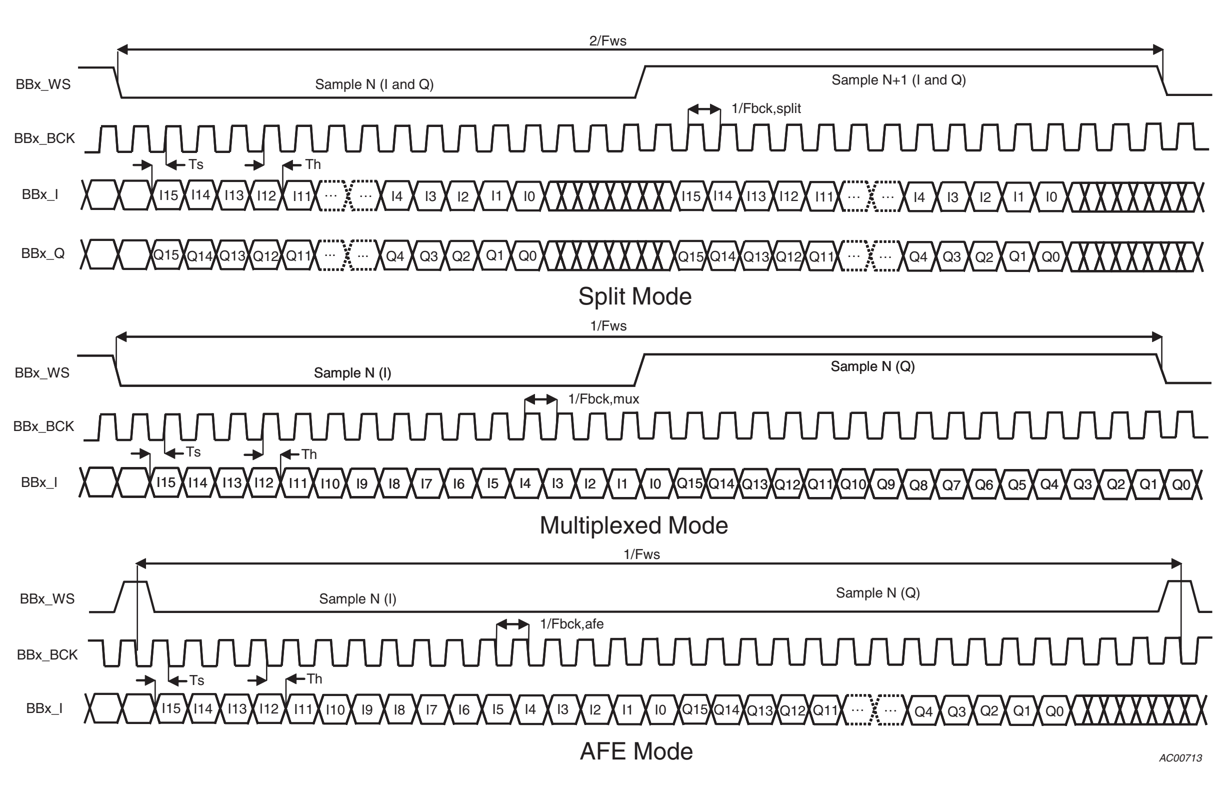
Split mode splits I and Q data onto the BB1_I and BB1_Q pins, respectively. The rising and falling edges of BB1_WS mark the beginning of each I and Q pair.

Multiplexed mode places the I and Q data onto the BB1_I data pin. The falling edge of BB1_WS marks the start of the I data and the rising edge marks the start of Q data.

AFE mode uses a single clock pulse on BB1_WS to indicate the start of I data followed by Q data using the BB1_I pin only.

Figure 11 show signals waveform for the three modes.

Figure 11. BBI waveforms and timings



In *Table 7* are reported the timing values for the BB interface.

Table 7. BBI timing values

Symbol	Parameter	Condition	Working rate					Unit
			Min.				Max.	
Fws	Word strobe	-	650	675	744.188	882	912	kHz
Fbck,split	Bit clock in split mode	-	16 x Fws	-	-	-	66	MHz
Fbck,mux	Bit clock in multiplexed mode	-	32 x Fws	-	-	-	32 x Fws	MHz
Fbck,afe	Bit clock in AFE mode	-	32 x Fws	-	-	-	66	MHz
Th	Data hold time	-	4	-	-	-	-	ns
Ts	Data setup time	-	8	-	-	-	-	ns

6.3 Audio interface (AIF)

The AIF (Audio Interface) is used for the communication with external digital signal sources and receivers. The main AIF features are:

- 1 Input SAI interface.
- 3 Output SAI interface.
- 1 S/PDIF transmitter.
- Audio Sample Rate Converter (ASRC).
- I/O sample rates: 44.1 kHz, 45.6 kHz, 48 kHz.

The AIF includes 1 Input SAI interface, 3 Output SAI interface and 1 S/PDIF (industry standard) transmitter. The receivers and transmitters can be used either in master-mode, running with the STA680 internal audio frequency of 44.1 kHz or in slave mode running with a frequency determined by the external device. In slave mode, in order to adapt the external data rate to the internal audio data rate, it is possible to use an internal Audio Sample Rate Converter (ASRC, see *Chapter 6.3.4*).

Table 8. AIF pin list

Pin name	Designation	Type	Drive
AUDIO_IN_AWS	Digital audio input word strobe	I/O	-
AUDIO_IN_ABCK	Digital audio input bit clock	I/O	-
AUDIO_IN_ADAT	Digital audio input serial data	I	-
AWS	Digital audio output word strobe	I/O	4mA
ABCK	Digital audio output clock	I/O	4mA
ADAT	Digital audio output serial data	O	4mA
ADAT2	Digital audio output serial data channel 2	O	4mA
ADAT3	Digital audio output serial data channel 3	O	4mA
DAC256X	Digital audio output oversampling clock (256 x Fs)	O	4mA
SPDIF	Digital audio output in SPDIF format	O	4mA
BLEND	Digital audio output blend output	O	4mA

6.3.1 Output serial audio interface (SAI)

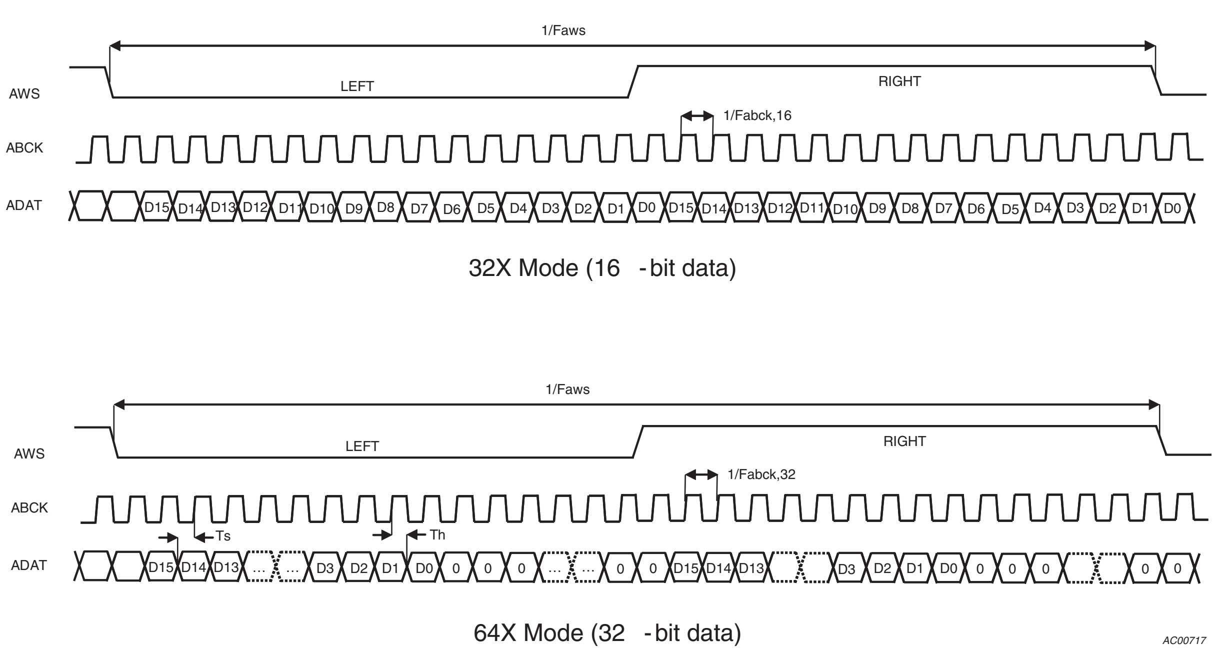
The output serial audio interface is used to send decoded audio samples from the HD Radio Decoder to an external IC for audio processing, or directly to a digital power amplifier.

The output SAI is an I2S interface which provides audio samples in stereo at a 44,1 kS/s sample rate. Other sample rates may be provided by means of the internal ASRC (see *Chapter 6.3.4*).

The output SAI interface shares the word strobe and the bit clock signal with three data output signals in order to support up to a total of 3 stereo channels of audio output. For interfacing the STA680 to an external DAC an oversampling clock whose frequency is 256 times the sampling frequency is provided. For pin description refers to *Table 8*.

The output SAI supports a 32x or 64x bit clock. The 32x clock mode shifts out serial data with no padding. The 64x clock mode shifts out the 16-bit audio data first followed by 16 bits of zero padding. *Figure 12* shows timing diagrams for the supported modes.

Figure 12. Serial audio interface waveforms and timings



In *Table 9* are reported the timing values for the output SAI interface.

Table 9. Serial audio interface timing values

Symbol	Parameter	Condition	Working rate			Unit
Faws	Word strobe	-	44.1 ±10 Hz	45.6 ±15 Hz	48 ±15 Hz	kHz
Fabck,16	Bit clock for 16-bit data	-	32 x Faws			MHz
Fabck,32	Bit clock for 32-bit data	-	64 x Faws			MHz
Th	Data hold time	-	5			ns
Ts	Data setup time	-	20			ns

6.3.2 Input serial audio interface

The input serial audio interface is used to receive the legacy AM/FM demodulated samples from an external AM/FM Tuner for blending purpose.

The input SAI is an I2S interface which accepts 16 bit audio samples in stereo at a 44,100 S/s sample rate. Other sample rates may be supported by means of the internal ASRC. For pin description refers to *Table 8*.

The input SAI supports a 32x or 64x bit clock. The 32x clock mode shifts out serial data with no padding. The 64x clock mode shifts out the 16-bit audio data first followed by 16 bits of zero padding. *Figure 12* shows timing diagrams for the supported modes.

6.3.3 S/PDIF interface

The S/PDIF Interface is an output only. It is compliant to the standard IEC 958 type II. For pin description refers to *Table 8*.

6.3.4 Audio sample rate converter (ASRC)

The STA680 supports various external host audio interfaces. The audio sample rate converter is designed to interface the audio output to systems with local master audio clock sources.

Output sample rates of 44,100 (± 10 Hz), 45,600 (± 15 Hz) and 48,000 (± 15 Hz) are acceptable. Total harmonic distortion plus noise (THD+N) at 1 kHz is greater than 85 dB down (0.0056%).

One stereo channel (i.e. single ADAT line) either from the input SAI or from the output SAI can be used with the audio sample rate converter.

In applications where the STA680 supplies the master clock to the audio D/A converter, the ASRC will be bypassed.

6.4 Serial peripheral interfaces (SPI)

The STA680 provides three serial peripheral interfaces, each one intended for a different and specific purpose:

- SPI1 - The first SPI is intended for communicating with the Host Microcontroller. Alternatively to this purpose can be also the Host Micro I^2C Interface (see *Chapter 6.4.1*)
- SPI2 - The second SPI has been taught to interface the STA680 with the external an external flash typically used to store the application code.
- SPI3 - The third SPI allow the HD Radio decoder to control an external SD/MMC card.

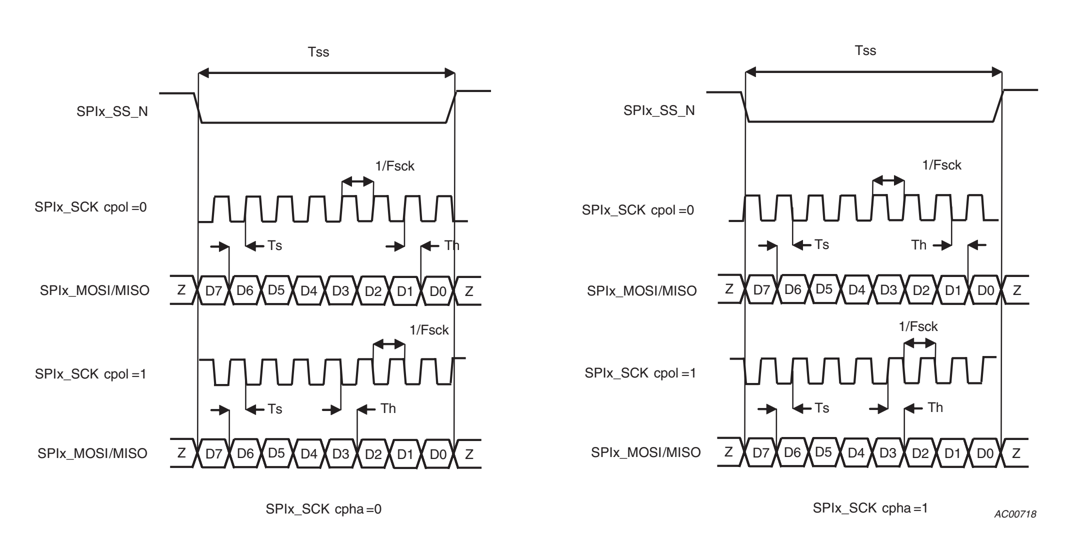
For master mode the SPI clock frequency is a divide down by n of the internal peripheral clock frequency, where n is an integer number comprised between 2 and 65536. The maximum SPI clock frequency in master mode is 25 MHz.

For slave mode the maximum input frequency value accepted for the SPI clock from an external device is a function of the internal peripheral clock.

In particular the maximum frequency is $F_{SPI} = \frac{F_{perif}}{8}$, where F_{perif} is the frequency of the clock feeding the peripheral bus and blocks

Figure 13 shows timing diagrams and waveform for the three SPI.

Figure 13. SPI interface timings diagrams and waveforms



In *Table 10* are reported the timing values for the SPI interface.

Table 10. SPI interface timing values

Symbol	Parameter	Condition	Working rate		Unit
			Min.	Max.	
Tss	Chip select	-	8/Fsck	-	ns
Fsck	Serial bit clock, slave mode	-	1.076	8000	kHz
Fsck	Serial bit clock, master mode	-	1.076	25000	kHz
Th	Data hold time	-	7	-	ns
Ts	Data setup time	-	15	-	ns

6.4.1 Host micro serial peripheral interface (SPI1)

The Host Micro SPI is used as a host processor interface. The usage of this interface is optional because the STA680 is able to communicate with an external microcontroller also via I^2C protocol (see *Chapter 6.4.5*, Host micro I^2C interface).

The Host Micro SPI is a slave only interface.

For pin description see *Table 11*.

Table 11. Host Micro SPI pin list

Pin name	Designation	Type	Drive
SPI1_MISO	Host Micro SPI data master in/slave out	O	4mA
SPI1_MOSI	Host Micro SPI data master out/slave in	I	-
SPI1_SCK	Host Micro SPI clock	i	4mA
SPI1_SS_N	Host Micro SPI active-low slave select 1	i	4mA

6.4.2 Flash serial peripheral interface (SPI2)

The Flash SPI is useful for storing boot code and other configuration parameters. The minimum required capacity for this purpose is 1 Mbit.

The STA680 is SPI master only on the FLASH bus. No glue logic is necessary to connect an external Flash to the HD Radio Decoder.

In the BGA package up to 4 chips selects are available. For pin description see *Table 2*.

Table 12. Flash SPI pin list

Pin name	Designation	Type	Drive
SPI2_MISO	Flash SPI data master in/slave out	I	-
SPI2_MOSI	Flash SPI data master out/slave in	O	4mA
SPI2_SCK	Flash SPI clock	O	4mA
SPI2_SS_N	Flash SPI active-low slave select 1	O	4mA
SPI2_SS1_N	Flash SPI active-low slave select 2	O	4mA
SPI2_SS2_N	Flash SPI active-low slave select 3 (1)	O	4mA
SPI2_SS3_N	Flash SPI active-low slave select 4 (1)	O	4mA

1. Only available in BGA package.

6.4.3 SD/MMC serial peripheral interface (SPI3)

The SPI SD/MMC SPI allows to connect the STA680 to a Secure Digital Card or a Multimedia Card for data storage purposes.

This interface can be configured to be master only and is available only in the BGA Package. For pin description see *Table 13*.

Table 13. SD/MMC SPI pin list

Pin name	Designation(1)	Type	Drive
SPI3_MISO	SD/MMC SPI data master in/slave out	I	4mA
SPI3_MOSI	SD/MMC SPI data master out/slave in	O	4mA
SPI3_SCK	SD/MMC SPI clock	O	4mA
SPI3_SS_N	SD/MMC SPI active-low slave select 1	O	4mA

1. Only available in BGA package

6.4.4 I^2C interfaces

The STA680 provides two I^2C interfaces that can be used to communicate with the Host Microcontroller. The first one may be used by the Host Micro in replacement of the SPI1 to control the main function of the HD Radio Decoder. The second one is an auxiliary interface and is available only in the LFBGA package option. For pin description see *Table 14*.

Table 14. Host and auxiliary I^2C interface pin list

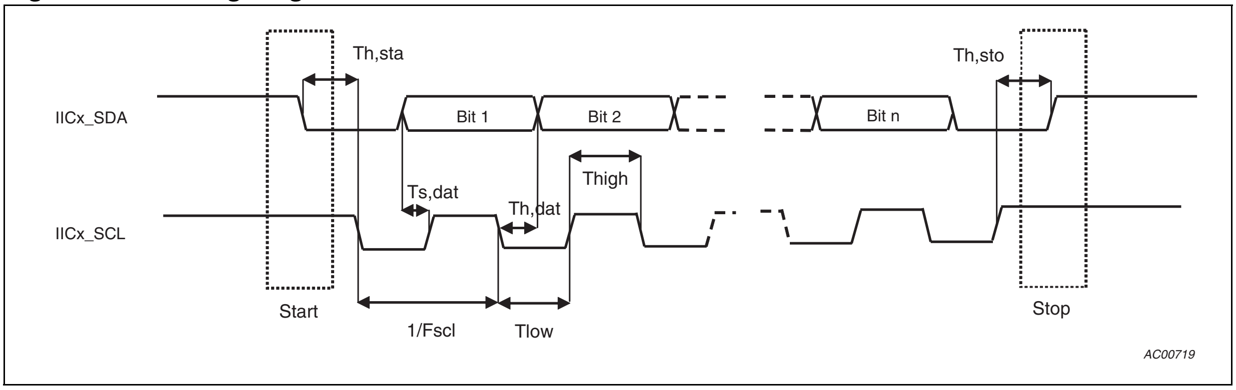
Pin name	Designation	Type	Drive
IIC1_SCL	Host Micro I^2C interface serial clock line	I/O	4mA
IIC1_SDA	Host Micro I^2C interface serial data line	I/O	4mA
IIC1_DA (1)	Host Micro I^2C interface data acknowledged	I/O	4mA
IIC2_SCL	Auxiliary I^2C interface serial clock line	I/O	4mA
IIC2_SDA	Auxiliary I^2C interface serial data line	I/O	4mA
IIC2_DA (1)	Auxiliary I^2C interface data acknowledged	I/O	4mA

1. Only available in BGA package.

The data pins of the two I^2C interfaces are open drain drivers and must have resistive pull-up conforming to Philip's IIC specification.

Figure 14 shows timing diagrams and waveform for the two I^2C interfaces.

Figure 14. Timing diagrams and waveform for the two I^2C interfaces



In *Table 15* are reported the timing values for the I^2C interface.

Table 15. I^2C interface timing values

Symbol	Parameter	Condition	Standard-mode		Fast-mode		Unit
			Min.	Max.	Min.	Max.	
Fscl	Scl clock frequency	-	-	100	-	400	kHz
Tlow	Low period of scl clock	-	4.7	-	1.3	-	µs
Thigh	High period of scl clock	-	4	-	0.6	-	µs
Th,dat	Data hold time	-	5	-		-	µs
Ts,dat	Data setup time	-	250	-	100	-	µs
Th,sta	Hold time for start condition	-	4	-	0.6	-	µs
Ts,sto	Setup time for stop condition	-	4	-	0.6	-	µs

6.4.5 Host micro I^2C interface (I2C1)

The Host Micro I^2C Interface enables the host processor to pass commands, diagnostic information, and data between the host processor and HD Radio Decoder.

The I2C1 interface is a standard I^2C interface where the STA680 acts as a slave to the Host Micro and only responds to requests for information. It is also configurable by the Host Micro to work as a master to better support bi-directional flow of data and audio.

The I2C1 interface supports 7-bit addressing and 8-bit data. It can run in both standard mode (serial clock frequency up to 100 kHz) and fast mode (up to 400 kHz). The I^2C device addresses are reported in *Table 16*.

Although not part of the IIC standard, an additional control line called IIC1_DA is provided. This line is useful for indicating when data is available and can be polled by either master or slave.

Table 16. I2C1 interface device address

I2C1	Primary address	Secondary address
Read Address	0101111b	0101101b
Write Address	0101110b	0101100b

6.4.6 Auxiliary I^2C interface (I2C2)

The Auxiliary I^2C interface can be programmed to be a master or slave. The usage of this interface by the host processor is optional and by default it is disabled after reset.

The I2C2 interface supports 7-bit addressing and 8-bit data. It can run in both standard mode (serial clock frequency up to 100 kHz) and fast mode (up to 400 kHz). The I^2C device addresses are reported in *Table 17*.

Although not part of the IIC standard, an additional control line called IIC1_DA is provided. This line is useful for indicating when data is available and can be polled by either master or slave.

Table 17. I2C2 interface device address

I2C2	Primary Address	Secondary Address
Read Address	0101011b	0101001b
Write Address	0101010b	0101000b

6.5 SDRAM interface

The SDRAM interface supports up to 32M x 16 SDRAM and supports both standard and mobile protocols. For pin description see *Table 18*

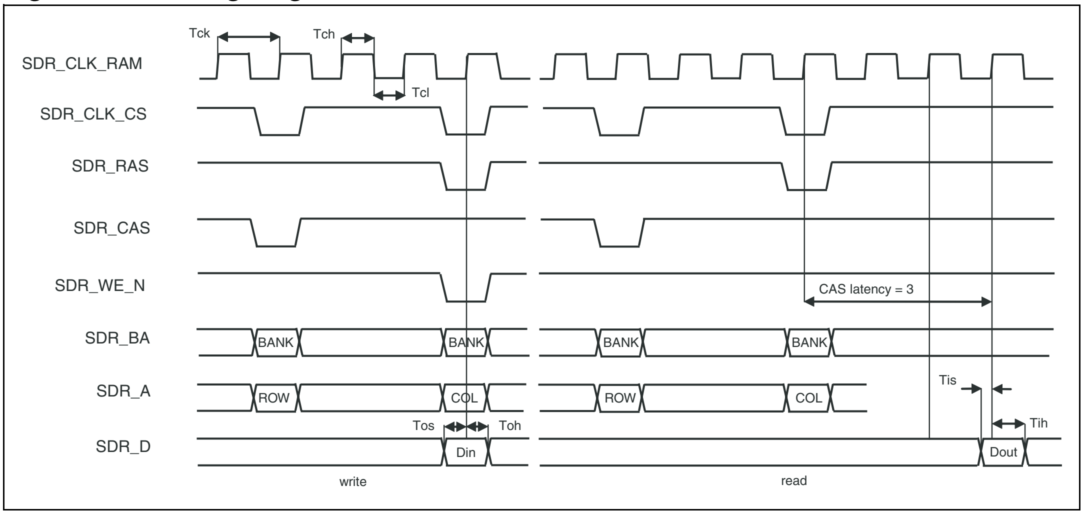
Table 18. SDRAM Interface pin description

Pin Name	Designation	Type	Drive
SDR_D[0:15]	SDRAM interface data bus	I/O	4 mA
SDR_A[0:12]	SDRAM interface address bus	O	4 mA
SDR_BA[0:1]	Bank address	O	4 mA
SDR_CAS_N	Active-low column address strobe	O	8 mA
SDR_RAS_N	Active-low row address strobe	O	8 mA
SDR_WE_N	Active-low write enable	O	8 mA
SDR_CS_N	Active-low chip select	O	8 mA
SDR_DQM0	low-byte data input/output mask	O	4 mA
SDR_DQM1	high-byte data input/output mask	O	4 mA
SDR_CKE	Clock enable	O	4 mA
SDR_CLK_RAM3V3	Clock to SDRAM for 3.3 V interface	O	8 mA
SDR_FEED_CLK	Feedback clock from SDRAM	I	8 mA

The minimum required SDRAM size for single channel application is 64 Mbit while for a dual channel application at least 128 Mbit are needed.

Figure 15 shows timing diagrams and waveform for the SDRAM interface.

Figure 15. Timing diagrams and waveform for the SDRAM interface



In *Table 19* are reported the timing values for the SDRAM interface.

Table 19. SDRAM interface timing values

Symbol	Parameter	Condition	Software application	Min.	Max.	Unit
Tck	SCL clock period	Core in normal drive	Full rate	7.35	-	ns
			Half rate	12.05	-	
		Core in overdrive	Full rate	6.25	-	
			Half rate	12.05	-	
Tch	CLK high level width	-	-	2.5	-	ns
Tcl	CLK low level width	-	-	2.5	-	ns
Toh	Data out hold time	-	-	0.9	-	ns
Tos	Data out setup time	-	-	1.5	-	ns
Tis	Data In setup time	-	-	0.8	-	ns
Tih	Data In hold time	-	-	1.6	-	ns
Tt	Transition time	-	-	-	1.2	ns

The frequency specification for the SDRAM interface depends on the supply condition of the core and on the software application.

Higher supply of the core allows higher speed on the SDRAM interface:

- Core in normal drive: SDRAM interface works at a maximum speed of 136MHz when VDDcore = 1.2V;
- Core in over drive: SDRAM interface works at a maximum speed of 160MHz when VDDcore = 1.4V

For power saving and less interference on board, the SDRAM speed can be programmed to work at half speed respect to the internal data processing:

- Full Rate SW application: SDRAM interface works at the same frequency of the internal data processing;
- Half Rate SW application: SDRAM interface works at half frequency respect to the internal data processing

7 Electrical specifications

7.1 Absolute maximum ratings

Table 20. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDD	Core supply voltage	1.47	V
VDD_GEN_IO	Generic IO supply voltage	3.6	V
VDD_FSH_IO	Flash IO supply voltage	3.6	V
VDD_RAM_IO	SDRAM IO supply voltage	3.6	V
VDD_OSC	Osc 1V8 supply voltage	1.95	V
VDD_PLL_ANA	Pll analog supply voltage	2.75	V
VDD_PLL_DIG	Pll digital supply voltage	1.47	V
VDD_SAF	Saf core supply voltage	1.47	V
V_i	Voltage on input pin	-0.5 to (VDDIO* + 0.5)	V
V_o	Voltage on output pin	-0.5 to (VDDIO* + 0.5)	V
T_{stg}	Operative storage temperature	-40 to +150	°C
T_j	Operative junction temperature	-40 to +125	°C
T_{amb}	Operative ambient temperature	-40 to +85	°C

7.2 Thermal data

Table 21. Thermal data

Symbol	Parameter	LQFP	LFBGA	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient(1)	30	35	°C/W

1. According to JEDEC specification on a 4 layers board.

7.3 Operating conditions

Table 22. DC electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
VDD	Core supply voltage	Normal drive		1.14	1.2	1.26	V
		Over drive		1.33	1.4	1.47	V
VDD_GEN_IO	Generic IO supply voltage	-		3.0	3.3	3.6	V
VDD_FSH_IO	Flash IO supply voltage	-		3.0	3.3	3.6	V
VDD_RAM_IO	SDRAM IO supply voltage	-		3.0	3.3	3.6	V
VDD_OSC	Oscillator analog supply voltage	-		1.7	1.8	1.95	V
VDD_PLL_ANA	PLL analog supply voltage	-		1.7	1.8	2.75	V
VDD_PLL_DIG	PLL digital supply voltage	Normal drive		1.14	1.2	1.26	V
		Over drive		1.33	1.4	1.47	V
VDD_SAF	SAF supply voltage	Normal drive		1.14	1.2	1.26	V
		Over drive		1.33	1.4	1.47	V
IDD_CORE(1)	Core supply current	T_{amb}=25°C	VDD=1.20V	-	105	-	mA
			VDD=1.26V	-	110	-	mA
		T_{amb}= 85°C	VDD=1.20V	-	-	260	mA
			VDD=1.26V	-	-	280	mA
IDD_IO(1)	IO supply current	T_{amb}=25°C	VDD_IO(2)=3.3V	-	40	-	mA
			VDD_IO=3.6V	-	45	-	mA
		T_{amb}= 85°C	VDD_IO=3.3V	-	-	55	mA
			VDD_IO=3.6V	-	-	58	mA
Pd(1)	Power dissipation	T_{amb}=25°C	typical supply	-	250	-	mW
		T_{amb}=85°C	max supply	-	-	600	mW
Iil	Low level input leakage current(3)	Vi = 0V		-	-	1.9	µA
Iih	High level input leakage current(3)	Vi = VDD_GEN_IO(4)		-	-	1.9	µA
Ilpu	High level input leakage current on pull up(5)	Vi = VDD_GEN_IO(4)		-	-	2.9	µA
Ilpd	Low level input leakage current on pull-down(6)	Vi = 0V		-	-	10	µA
Ipu	Pull-up current	Vi = 0V		-	-	72	µA
Ipd	Pull-down current	Vi = VDD_GEN_IO(4)		-	-	72	µA

Table 22. DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Rpu	Equivalent pull-up resistance(7)	Vi = 0V	50	-	-	KΩ
Rpd	Equivalent pull-down resistance(8)	Vi = VDD_GEN_IO(4)	50	-	-	KΩ
Vil	Low level input voltage	3.3 supply mode	-0.3	-	0.8	V
Vih	High level input voltage	3.3 supply mode	2.0	-	VDD_GEN_IO +0.3	V
Vhyst	Input hysteresis voltage	3.3 supply mode	50	-	-	mV
Voh	Output high voltage	Ioh =XmA(9)	VDD_RAM_IO – 0.2V	-	-	V
Vol	Output low voltage	Iol =XmA(9)	-	-	0.2	V
Vesd	Electrostatic discharge voltage	Human Body Model	-	-	2000	V
		Machine Model	-	-	200	V
		Charge device Model	-	-	500	V
Ilatchup	Injection current	Maximum operating junction temperature 125 °C	100	-	-	mA
VDD_RAM_IO	SDRAM IO supply voltage	-	3.0	3.3	3.6	V
Iil_ram	Low level input leakage current(3)	Vi = 0V	-	-	-	µA
Iih_ram	High level input leakage current(3)	Vi = VDD_RAM_IO	-	-	-	µA
Ilpu_ram	High level input leakage current on pull up(5)	Vi = VDD_RAM_IO	-	-	-	µA
Ilpd_ram	Low level input leakage current on pull-down(6)	Vi = 0V	-	-	-	µA
Ipu_ram	Pull-up current	Vi = 0V	44		122	µA
Ipd_ram	Pull-down current	Vi = VDD_RAM_IO	29		122	µA
Rpu_ram	Equivalent pull-up resistance(7)	Vi = 0V	29		67	KΩ
Rpd_ram	Equivalent pull-down resistance(8)	Vi = VDD_RAM_IO	29		103	KΩ
Vil_ram	Low level input voltage	-	0.8	-	-	V
Vih_ram	High level input voltage	-	-	-	2	V
Vhyst_ram	Schmitt trigger hysteresis	-	300	-	800	mV

Table 22. DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voh_ram	High level output voltage	Ioh = -XmA(9)	VDD_RAM_IO -0.3	-	-	V
Vol_ram	Low level output voltage	Iol =XmA(9)	-	-	0.3	V

1. Current consumption and power dissipation measured for single channel software application running at 127MHz.
2. VDD_IO = VDD_GEN_IO + VDD_FSH_IO + VDD_RAM_IO.
3. Performed on all the input pins excluded the pull-down and pull-up ones.
4. VDD_GEN_IO may be VDD_FHS_IO or VDD_GEN_IO depending on interface considered.
5. Performed only on the Input pins with pull up.
6. Performed only on the Input pins with pull down.
7. Guaranteed by Ipu measurements.
8. Guaranteed by Ipd measurements.
9. XmA = 4mA for a BD4, 8mA for BD8 pad type.

8 Package information

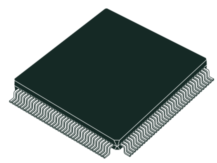
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 16. LQFP144 (20x20mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.6890	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP144 (20x20x1.40mm)
Low profile plastic **Q**uad **F**lat **P**ackage

Note 1: Exact shape of each corner is optional.

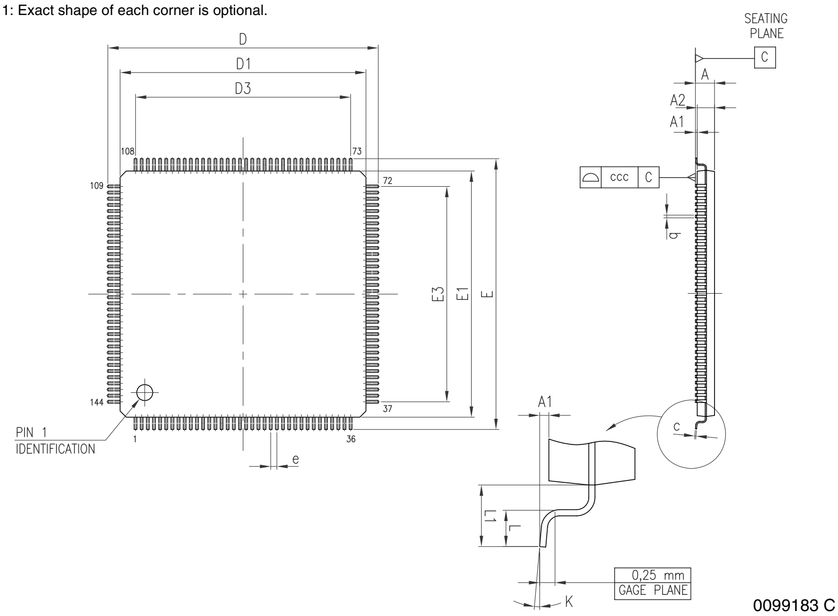
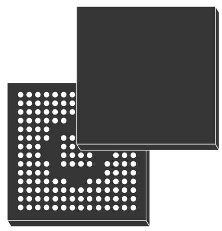


Figure 17. LFBGA 168 balls (12x12x1.4 mm) mechanical data and package dimensions

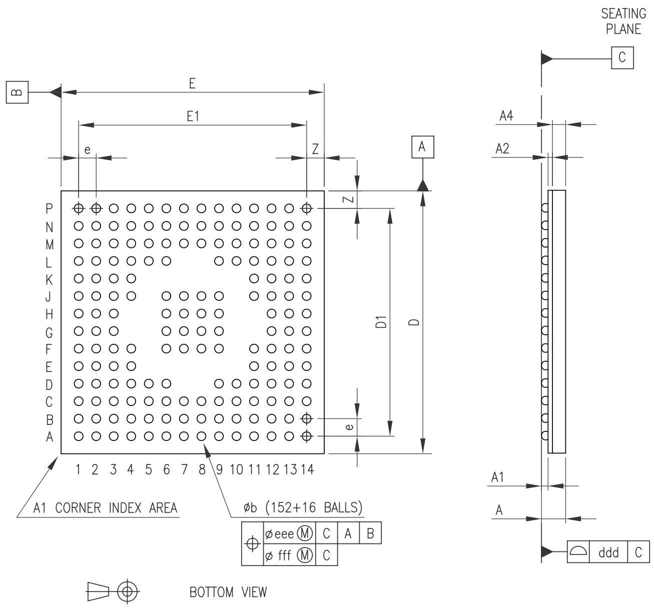
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.400			0.0551
A1	0.210			0.0083		
A2		0.200			0.0078	
A4			0.800			0.0315
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	11.850	12.000	12.150	0.4665	0.4724	0.4783
D1		10.400			0.4094	
E	11.850	12.000	12.150	0.4665	0.4724	0.4783
E1		10.400			0.4094	
e		0.800			0.0315	
Z		0.800			0.0315	
ddd			0.100			0.0039
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 12 x 12 x 1.4mm

LFBGA 168 balls
Low profile **F**ine Pitch **B**all **G**rid **A**rray



8123111 B

9 Revision history

Table 23. Document revision history

Date	Revision	Changes
25-Jul-2008	1	Initial release.
19-Dec-2008	2	Update ECOPACK® information in *Section 8 on page 44*.
31-Jul-2009	3	Added *Section 2: HD Radio™ system on page 7*. Changed *Table 2*, *4*, *7*, *12*, *13*, *14*, *19* and *22*. Changed *Figure 4*, *5*, *6*, *7*, *8* and *13*. Add *Figure 10: Crystal characteristics on page 26*.