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# MOS FIELD EFFECT TRANSISTOR $\mu$ PA1764

# SWITCHING DUAL N-CHANNEL POWER MOS FET INDUSTRIAL USE

# DESCRIPTION

The  $\mu$  PA1764 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

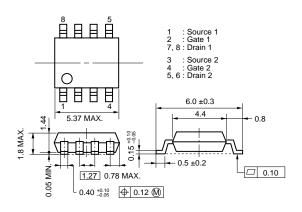
# **FEATURES**

- Dual chip type
- Low on-state resistance  $R_{DS(on)1} = 27 \text{ m}\Omega \text{ TYP.}$  (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 3.5 A)  $R_{DS(on)2} = 32 \text{ m}\Omega \text{ TYP.}$  (V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 3.5 A)  $R_{DS(on)3} = 34 \text{ m}\Omega \text{ TYP.}$  (V<sub>GS</sub> = 4.0 V, I<sub>D</sub> = 3.5 A)
- Low input capacitance C<sub>iss</sub> = 1300 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

# **ORDERING INFORMATION**

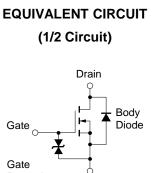
PART NUMBER	PACKAGE
μPA1764G	Power SOP8

# PACKAGE DRAWING (Unit : mm)



# ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	60	V	
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V	
Drain Current (DC) (Tc = 25°C)	D(DC)	±7	А	
Drain Current (pulse) <sup>Note1</sup>	D(pulse)	±28	А	
Total Power Dissipation (1 unit) Note2	Р⊤	1.7	W	
Total Power Dissipation (2 unit) Note2	Р⊤	2.0	W	
Channel Temperature	$T_{ch}$	150	°C	
Storage Temperature	Tstg	–55 to + 150	°C	
Single Avalanche Current Note3	las	7	А	
Single Avalanche Energy Note3	Eas	98	mJ	



Source

Protection

Diode

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1%

**2.**  $T_A = 25^{\circ}C$ , Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm

- 3. Starting T\_ch = 25°C, V\_DD = 30 V, R\_G = 25  $\Omega,$  V\_Gs = 20  $\rightarrow$  0 V
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

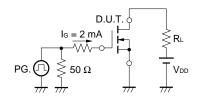
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	loss	Vds = 60 V, Vgs = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate Cut-off Voltage	VGS(off)	Vds = 10 V, Id = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	<b>y</b> fs	Vds = 10 V, Id = 3.5 A	5.0	9.0		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Id = 3.5 A		27	35	mΩ
	RDS(on)2	Vgs = 4.5 V, Id = 3.5 A		32	42	mΩ
	RDS(on)3	Vgs = 4.0 V, Id = 3.5 A		34	46	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		1300		pF
Output Capacitance	Coss	Vgs = 0 V		230		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		110		pF
Turn-on Delay Time	td(on)	Vdd = 30 V, Id = 3.5 A		15		ns
Rise Time	tr	Vgs = 10 V		69		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 10 Ω		65		ns
Fall Time	tr			27		ns
Total Gate Charge	QG	Vdd = 48 V		29		nC
Gate to Source Charge	Q <sub>GS</sub>	Vgs = 10 V		3.6		nC
Gate to Drain Charge	Qgd	ID = 7.0 A		7.4		nC
Body Diode Forward Voltage	VF(S-D)	IF = 7.0 A, VGS = 0 V		0.84		V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		66		nC

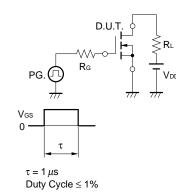
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

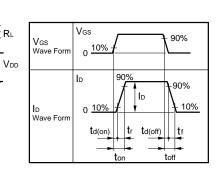
PG.  $V_{GS} = 20 \rightarrow 0 V$   $V_{DD}$   $V_{DD}$ 

# **TEST CIRCUIT 3 GATE CHARGE**



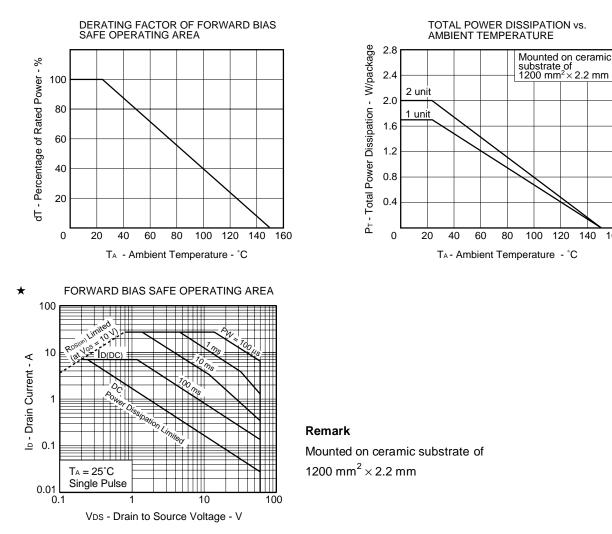
## **TEST CIRCUIT 2 SWITCHING TIME**



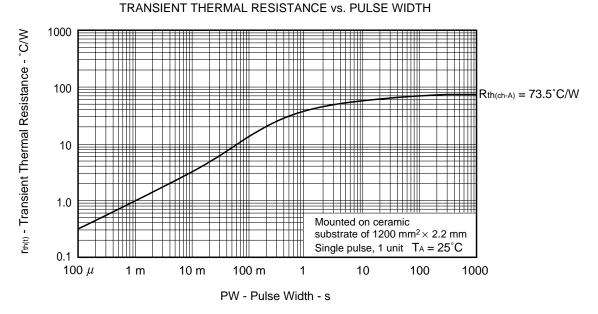


140 160





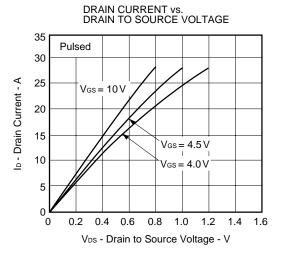
## TYPICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)



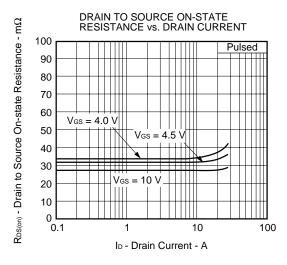
Data Sheet G14329EJ2V0DS

100 Pulsed  $V_{DS} = 10 V$ Drain Current - A 10  $T_A = 150^{\circ}C$ T<sub>A</sub> = 75°C T<sub>A</sub> = 25°Ç 1 -25°C TA= -0.1 0.01 2 3 4 5 6 Vgs - Gate to Source Voltage - V

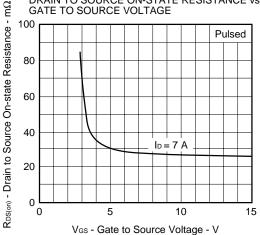
FORWARD TRANSFER CHARACTERISTICS



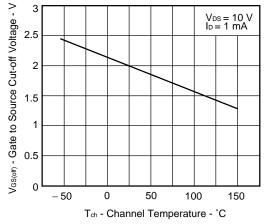
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT 100 V<sub>DS</sub> = 10 V Pulsed S |<sub>yis</sub>| - Forward Transfer Admittance -100 100 T₄ = −25°C  $T_A = 25^{\circ}C$ 75°C TA=  $T_A = 150^{\circ}C$ Ħ 0.01 0.1 10 100 1 ID - Drain Current - A



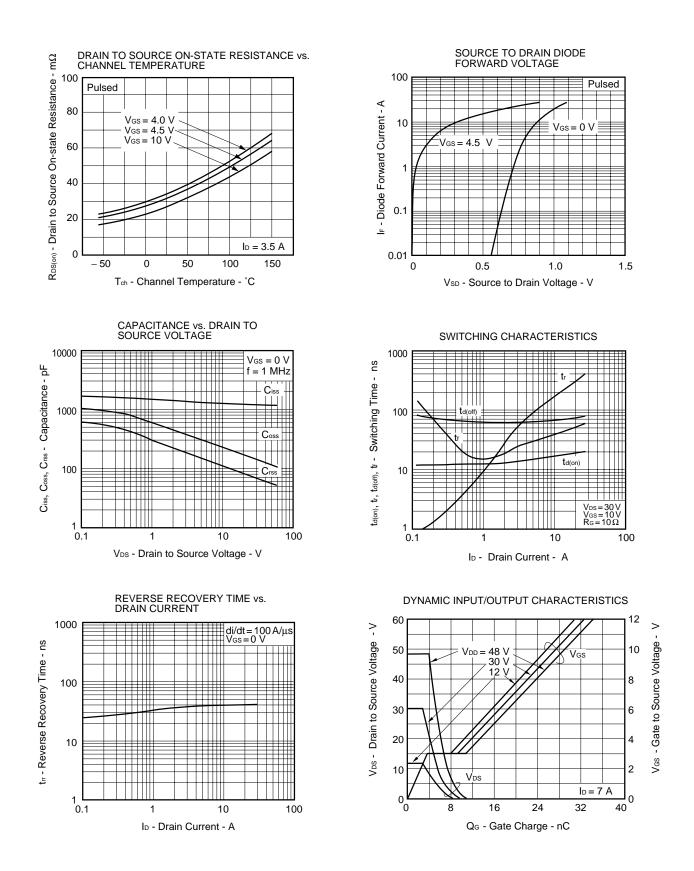
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

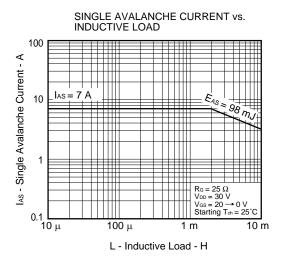


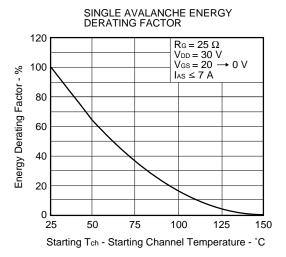
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



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[MEMO]

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