Mechanical and Electrical Specifications

Table 8 and Figure 19 illustrate the timing requirements for the microprocessor interface. The parameter t_{cyc} is the period of the receive DS3/E3 clock (DS3CKI). This clock signal is used in the read circuit of the microprocessor to ensure that no status events are missed and that counter values are accurate when read.

Read operation requires the read strobe to be low for three t_{cyc} clock cycles ensuring that changing status and error counts are properly processed. If a gapped clock is applied to the circuit, it is sufficient to allow three receive clock cycles between read strobes to allow a latching circuit to clear in the microprocessor interface.

Table 8. Microprocessor Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{as}	Address Setup before ALE Low	7	-	-	nsec
t_{cale}	Controller ALE Pulse Width	34	-	-	nsec
t_{ah}	Address Hold after ALE Low	10	-	-	nsec
t_{rwa}	RD*/WR* High to ALE High	10	-	-	nsec
t_{adwrh}	Address/Select to WR* High	117	-	-	nsec
t_{adrdl}	Address/Select to RD* Low	17	-	-	nsec
t_{wrw} (Read Operation)	RD* Pulse Width[1]	$3*t_{cyc}$	-	-	nsec
t_{wrw} (Write Operation)	WR* Pulse Width	100	-	-	nsec
t_{rdd}	RD* Low to Data Available	-	-	30	nsec
t_{rdh}	Read Data Hold Time[2]	3	-	-	nsec
t_{clcl}	ALE Low to RD*/WR* Low	10		-	nsec
t_{ds}	Data Stable Before WR* High	25	-	-	nsec
t_{dh}	Data Hold after WR* High	10	-	-	nsec
t_{sh}	Address/Select Hold after RD*/WR* Low	110	-	-	nsec
—	Controller Port Cycle Time	154	-	-	nsec

1. T_{cyc} = Period of clock connected to the DS3CKI pin.
2. The external address/data bus capacitance will increase the data hold time if the bus remains undriven.

Figure 19. Microprocessor Interface Timing

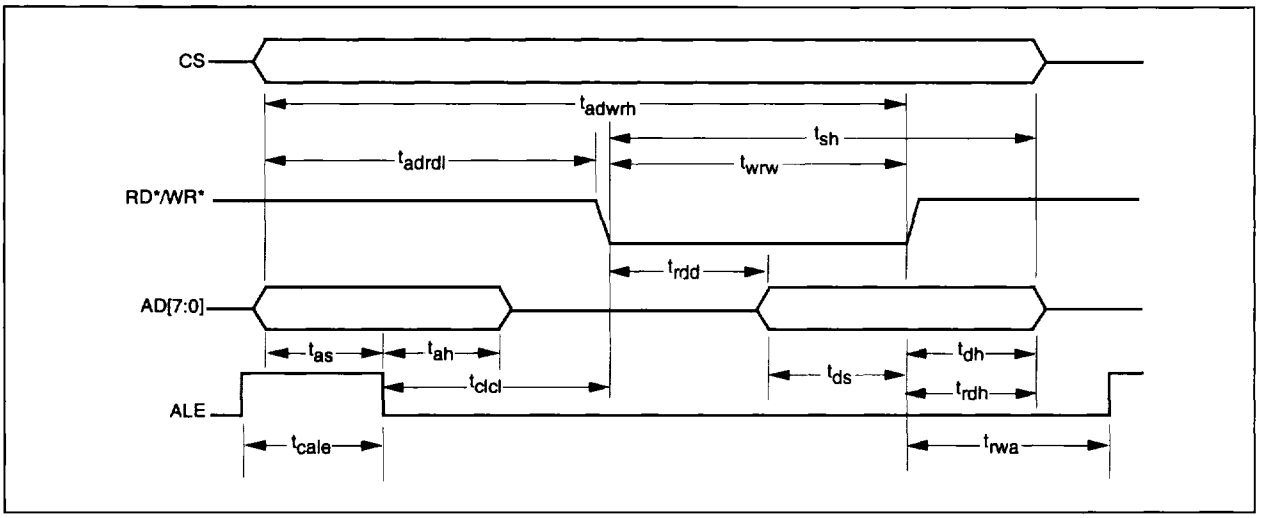


Figure 20 and Table 9 through Table 11 illustrate the clock and data relationships for all output and input signals. Propagation delays for the output signals are listed below. The output signal timings are relative to the listed edge of the clock. Clock outputs derived from clock inputs are listed with the edge as both. This means that the delay number given applies for either edge. Input signals should have setup and hold times with respect to the listed edge of the given input clock. All times are listed in nanoseconds and are measured with 30 pF loading on the output pins.

Table 9. Clock Timing Requirements

Timing Requirements	Clock	Min	Typ (44.736 MHz)	Typ (34.368 MHz)	Units
Low Pulse Width - p_{wl}	RXCKI, DS3CKI, TXCKI	5.0	11.2	14.55	nsec
High Pulse Width - p_{wh}	RXCKI, DS3CKI, TXCKI	5.0	11.2	14.55	nsec
Cycle Time - t_{cyc}	RXCKI, DS3CKI, TXCKI	19.0	22.4	29.1	nsec

Figure 20. Output and Input Signal Timing

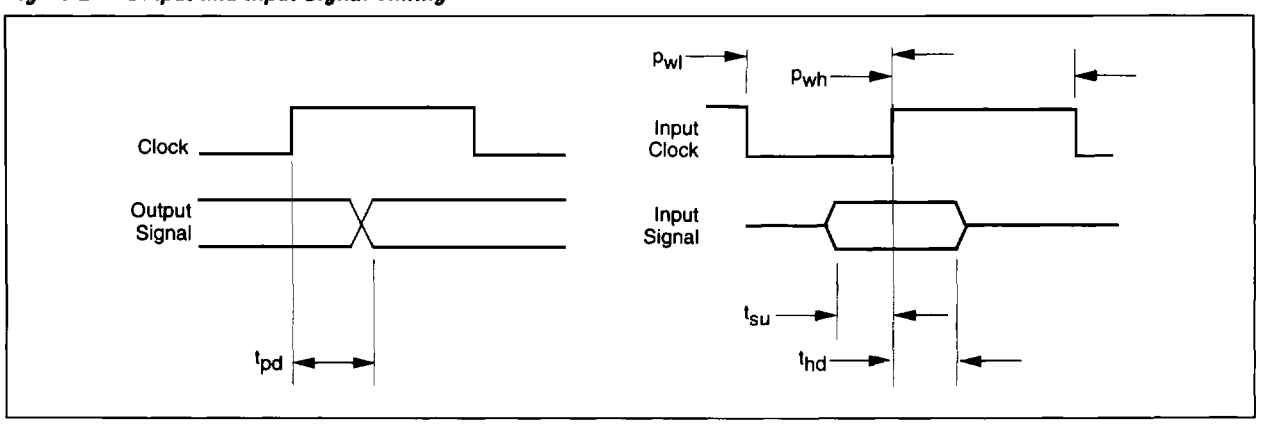


Table 10. Output Signal Timing

Output Symbol	Clock	t_{pd} min.	t_{pd} max	Edge	Units
RXCLK	DS3CKI/RXCKI	2.8	13.0	Rising	nsec
RXMSY	RXCLK	1.8	5.0	Rising	nsec
RXDAT	RXCLK	1.6	5.2	Rising	nsec
RXCCK	RXCLK	3.2	9.1	Rising	nsec
CBITO	RXCCK	t_{cyc}+1.0	t_{cyc}+2.0	Rising	nsec
RXOVH	RXCLK	2.5	11.1	Rising	nsec
RXBCK	RXCLK	2.0	10.0	Falling	nsec
RXGAPCK	DS3CKI/RXCKI	2.8	22.0	Both	nsec
RXGAPCK	RXCLK	1.0	9.0	Both	nsec
RDAT[7] /TXNRZ	TCLKO	1.2	7.0	Rising	nsec
TXPOS/TXNEG	TCLKO	1.2	8.2	Rising	nsec
TXSYO	TXCKI	3.2	11.1	Rising	nsec
TXGAPCK	TXCKI	2.2	11.7	Both	nsec
TXBCK	TXCKI	3.0	16.0	Rising	nsec
TCLKO	TXCKI	2.8	12.8	Rising	nsec
TXOVH	TXCKI	3.4	15.6	Falling	nsec

Table 11. Input Setup/Hold Timing

Input Symbol	Clock	t_{su} min	t_{hld} min	Edge	Units
CBITI	TXCCK	2 * t_{cyc}	4 * t_{cyc}	Falling	nsec
TDAT[7:0] (Parallel Mode)	TXBCK	–2 * t_{cyc}	Full TXBCK Period	Rising	nsec
SNDMSG,SNDFCS	TXBCK	–2 * t_{cyc}	Full TXBCK Period	Rising	nsec
TXSYI	TXCKI	1.0	6.0	Rising	nsec
TXDATI	TXCKI	1.0	6.0	Falling	nsec
TXENI	TCLKO	9.0	0.0	Rising	nsec
LCVERRI	TCLKO	9.0	0.0	Rising	nsec
RXPOS, RXNEG	DS3CKI	1.0	5.0	Rising	nsec

Environmental Conditions

Power Requirements and Temperature Range

Stresses above those listed as Absolute Maximum Ratings (Table 12) may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	Volts
Input Voltage	V_{IN}	–0 to V_{DD} +0.3	Volts
Output Voltage	V_{OUT}	–0.3 to V_{DD} +0.3	Volts
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +150	°C
Operating Supply Voltage	V_{DD}	+4.75 to +5.25	Volts

Electrical Characteristics

DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. All outputs are CMOS drive levels and can be used with CMOS or TTL logic (see Table 13 and Table 14). Specific characteristics given in Tables 13 and 14 apply over an operating temperature range of –40° to +85°C and a supply voltage range of 4.75 to 5.25 volts, unless otherwise noted.

Table 13. DC Characteristics

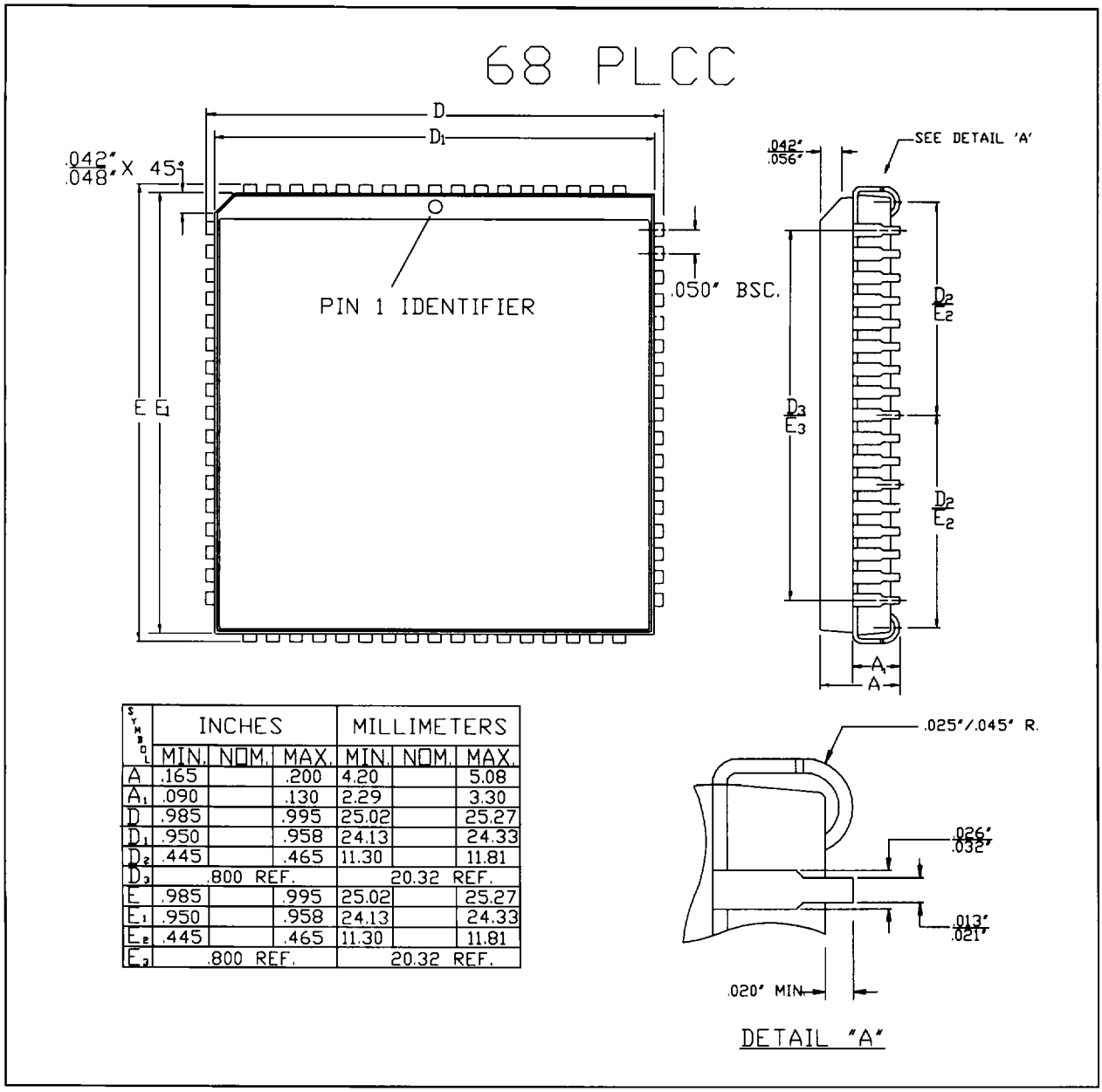
Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75	5.00	5.25	V
V_{OH}	All Outputs, except as noted in Table 14	I_{OH} = – 4 mA	2.4	4.5		V
V_{OL}	All Outputs, except as noted in Table 14	I_{OL} = 4 mA	–	0.2	0.4	V
V_{IH}	Input Voltage High		2.0	–	–	V
V_{IL}	Input Voltage Low		–	–	0.8	V
I_{DD}	Supply Current	V_{DD} = 5.25 V @ 52 MHz	–	–	175	mA
I_{DD}	Supply Current	V_{DD} = 5.25 V @ 45 MHz	–	–	150	mA
I_{IL}	Input Leakage Current		–	±1.0	±10	µA
C_{IN}	Input Capacitance	Inputs and AD[7:0]	–	–	3	pF
C_{OUT}	Output Capacitance	All Outputs	–	–	10	pF
–	ESD Protection	MIL-STD-883C Method 3015	2	>3	–	kV
–	Latch-up Input Current	JEDEC JC-40.2	150	>400	–	mA

Table 14. Output Drive Capability

Output	Pin	Drive Current @ V_{OH} or V_{OL}
RXCLK	22	±8 mA
IDLE	24	±2 mA
VALFCS	25	±8 mA
RDAT[5, 3, 2, 1, 0]	32, 30, 29, 28, 27	±2 mA
CBITO	37	±2 mA
RXCCK	38	±2 mA
TESTO	41	±2 mA
TXCCK	46	±2 mA
TXBCK	57	±8 mA
CNTINT	62	±2 mA
DLINT	63	±2 mA

Mechanical Specifications

Figure 21. 68–Pin Plastic Leaded Chip Carrier (J-Bend)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D_1	.950		.958	24.13		24.33
D_2	.445		.465	11.30		11.81
D_3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E_1	.950		.958	24.13		24.33
E_2	.445		.465	11.30		11.81
E_3	.800 REF.			20.32 REF.		