Linear Power PSoC™ Devices

1.0 Features

1.1 Key Features

- Extended Operating Voltage of 2.5V to 36V
- 2 HV Linear Opamp Control Loops for Driving Power PFETs
- 2 HV Analog Sense Inputs
- 4KB of Flash
- 256 Bytes of SRAM

1.2 Improved Features

- Very Low Current Mode for 100 nA Sleep (Deep Sleep)
- Analog Absolute Accuracy (0.75%)
- Additional Flexibility for Sleep Modes
- 2 Comparators with DAC References
- 6- to 12-Bit ADC (20 Ksps at 8 Bits)
- Configurable Analog Mux, 10:1 or 5:2 Differential
- Configurable Digital Blocks
  - 8- to 16-Bit Timers and Counters
  - Connectable to All GPIO Pins
  - Digital Blocks can Drive Outputs to 36V
  - Complex Peripherals by Combining Blocks

1.3 Applications

- Battery Chargers (Linear or Fly Back)
- White LED Drivers
- Temperature Sensor (Thermistor, Thermocouple)

2.0 Block Diagram

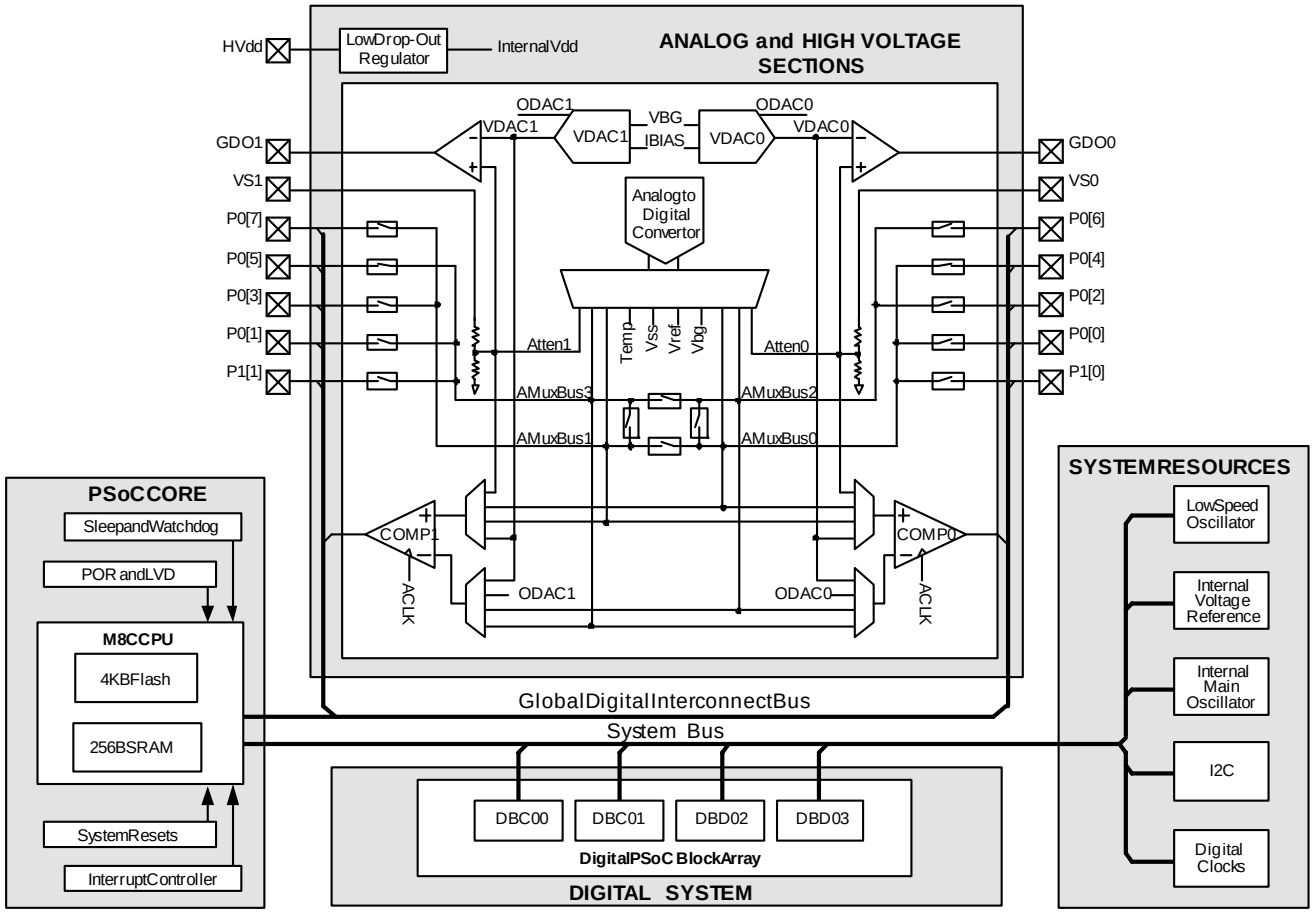


Figure 2-1. Block Diagram

3.0 Complete Feature List

- Extended Operating Voltage of 2.5V to 36V
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Low Power at High Speed
  - Industrial Temperature Range: -40°C to +85°C
- Additional Flexibility for Sleep Modes
  - Select when System Resources are Shut Down
  - Very Low Current Mode for 100 nA Sleep (Deep Sleep)
- 2 Advanced Power PSoC Blocks
  - 2 High Voltage Analog Sense Inputs
  - 2 High Voltage Linear Opamp Control Loops for Driving Power PFETs
- Advanced Analog Blocks
  - Analog Absolute Accuracy (0.75%)
  - 2 Comparators with DAC References
  - 6- to 12-Bit ADC (20 Ksps at 8 Bits)
  - Configurable Analog Mux, 10:1 or 5:2 Differential
- 4 Advanced Digital Blocks
  - 8- to 16-Bit Timers and Counters
  - Connectable to All GPIO Pins
  - Complex Peripherals by Combining Blocks
- Flexible On-Chip Memory
  - 4KB Flash Program Storage 50,000 Erase/Write Cycles
  - 256 Bytes SRAM
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates (64-Byte Blocks)
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Precision, Programmable Clocking
- Complete Development Tools
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128KB Trace Memory
  - Free Application Generation Software (PSoC Express™)
- Additional System Resources
  - I2C™ Master, Slave, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
  - 4-Bit Current References

3.1 Differences from CY8C42x23

- The CY8C41x23 is a cost-reduced version of the CY8C42x23 and targets linear-control applications.
- The HVO pin and current DACs have been eliminated and the PWM with deadband capability has been removed from the digital blocks.

4.0 PSoC Functional Overview

The key feature set of the Linear Power PSoC family is the ability to be powered from and connect to voltages above the standard 5V logic voltage used by most microcontrollers. The PSoC's HV_{dd} pin can connect to a supply voltage of up to 36V. Internally, an LDO regulator converts the supply voltage to 5V for powering the analog system, digital system, the core, and the GPIO.

High voltage signals can be connected to the analog circuitry through one of two selectable attenuators, each having three ranges. These precision dividers reduce the external analog voltage by a factor of 4, 8, or 16. This allows single-ended or differential signals with up to 36V common mode to be measured with the ADC. The GPIO pins are not high-voltage tolerant. Signals with voltages exceeding V_{GPIO} (as shown in the Absolute Maximum Ratings table, *8.2*) **cannot** be connected to the GPIO pins (P0 [7:0] and P1 [1:0]). Doing so will damage the device.

The Linear Power PSoC family consists of several *Mixed-Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low-cost single-chip programmable component. A Linear Power PSoC device includes configurable analog, digital, and power blocks, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The PSoC architecture, as illustrated in *Figure 2-1*, is comprised of five main areas: the Core, the System Resources, the Digital System, the Analog System, and the Power Control System. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each PSoC device includes 4 digital blocks and up to 10 general purpose IO (GPIO). The GPIO provide access to the global digital and analog interconnects.

4.1 Linear Power PSoC Core

The Linear Power PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as digital clocks for increased flexibility of the PSoC mixed-signal arrays; I2C functionality for implementing master, slave, and multi-master; an internal voltage reference of 1.3V for a number of analog PSoC subsystems; and various system resets supported by the M8C.

4.2 Digital System

The Digital System is composed of 4 Basic (Type C) digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. A sampling of digital block configurations is listed below.

- Counters (8 to 32 bit)
- Timers (8 to 32 bit)

The digital blocks can be connected to any GPIO through a set of global buses that can route any signal to any pin. The buses also allow signal multiplexing and the combining of signals through logic operations. This configurability frees designs from the constraints of a fixed peripheral controller.

4.3 Multiple Sleep Modes

The CY8C41x23 devices can have some of the system resources (the SleepTimer/Watchdog Timer, the Voltage Regulator or the Power Supply Supervisor) powered down in order to achieve the desired level of sleep current. Sleep modes with current levels from 750 µA in idle to 0.1 µA in deep sleep, and wakeup times from instantaneous to 400 µsec are available. Deeper sleep modes have longer wakeup times and sleep modes with more resource power typically have shorter wakeup times.

4.4 Analog System

The CY8C41x23 devices have solid analog performance, low (100 µV) offsets, reduced temperature sensitivity, and are capable of measuring 0.75% absolute voltage accuracy.

The Analog System is composed of configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Following are some of the more common PSoC analog functions (most available as user modules).

- Analog-to-digital converters (up to 12-bit resolution with single-ended or differential inputs).
- Adjustable input gain of 1/4, 1, 4, or 16 for the ADC.
- Pin-to-pin comparator with low power mode for operation during sleep.
- Single-ended or differential comparators (up to 2) with absolute (1.3V) reference or internal DAC reference.
- 1.3V reference (as a System Resource).

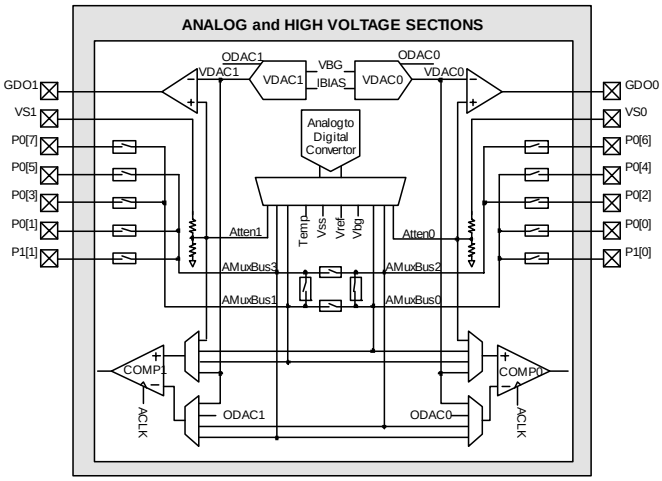


Figure 4-1. Analog Block Diagram

4.5 High Voltage Interface

The Gate Drive Outputs (GDO0 and GDO1) can each be used to drive the gate of a high-side PFET in a linear regulator. The GDO0 and GDO1 outputs will drive between HV_{dd}-5V and HV_{dd}. The Gate Drive Outputs are driven by an amplifier and used to control a PFET in a linear mode. A sense voltage can be fed back to the amplifier through an HV attenuator to implement a constant voltage or constant current driver. The output of the VDAC can be used to set the target voltage of the regulator.

4.6 The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin in ports P0 and P1. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. This bus is split into four sections, AMux Bus 0 and AMux Bus 2, which connect to the even port pins and AMux Bus 1 and AMux Bus 3, which connect to the odd port pins.

The four sections can be combined to support dual-channel single-end processing, single-channel differential processing, or dual-channel differential processing. They can also be connected as one bus that can route to all GPIO pins.

Other multiplexer applications include:

- Chip-wide mux that allows analog input from up to 10 GPIO pins.
- Crosspoint connection between any GPIO pin combinations.

4.7 Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems implemented in a single power block. Additional resources include an I2C master and slave, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I2C module provides 50-, 100-, and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

4.8 Development Tools

- Standard Cypress PSoC IDE tools are available for debugging the CY8C41x23 family of parts. However, the additional trace length and a minimal ground plane in the Flexpod can create noise problems that make it difficult to debug a Power PSoC design. A custom bonded On-Chip Debug (OCD) device is available in an 32-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and can be connected to the ICE through a high density connector.
- In-System Serial Programming (ISSP) is available. However, ISSP for Power PSoC differs from ISSP for standard PSoC devices. With Power PSoC devices, the power pin (HV_{dd}) should not be connected directly to the V_{dd} pin of the ISSP connector. Doing so can damage the programming device.

5.0 Typical Linear Power PSoC Applications

5.1 Linear White LED Driver

A white LED driver is a constant current power supply. By driving the same current through a set of LEDs in series, the intensity of the LEDs can be closely matched. The CY8C41x23 Linear Power PSoC can be configured as a constant voltage or constant current linear supply. In this configuration, the HV_{dd} voltage is high enough to drive the LEDs in series and current regulation is needed. White LEDs typically have a forward voltage of around 4V, so in the four LED configuration shown in *Figure 5-1*, HV_{dd} would have to be around 16V (plus allowance for voltage losses in the FET and the current sense resistor, R_{ISENSE}). The HV_{dd} voltage is converted to 5V by the internal Low Drop-Out Regulator for use by the Power PSoC Core.

To maintain constant voltage, the gate of the External PFET is controlled by the GDO0 pin and driven in a linear mode. The voltage at the top of the load, connected to VS0, is attenuated by the internal resistive element, Atten0. The voltage out of the attenuator is fed into the positive terminal of an amplifier configured as a voltage follower. The amplifier's negative input is connected to the output of the voltage DAC, VDAC0. This creates a feedback loop that maintains the VS0 node at a voltage proportional to the VDAC0 setting. The Atten0 output is also connected to the ADC so the control software can monitor the output voltage.

To maintain constant current, the voltage across the R_{ISENSE} resistor is routed through pin P0[4] and AMuxBus0 to the ADC where it is monitored. The control software adjusts the VDAC0 setting, based on current sense measurements, to achieve the desired current through the load.

5.1.1 Resources

This application could connect the R_{ISENSE} resistor to any of the GPIO pins (P0[7:0] and P1[1:0]). The Linear Power PSoC still has all of its digital resources, half of the high voltage resources, one VDAC, two IDACs, seven of the analog multiplexer channels to the ADC, and over 90% of the CPU available for other tasks.

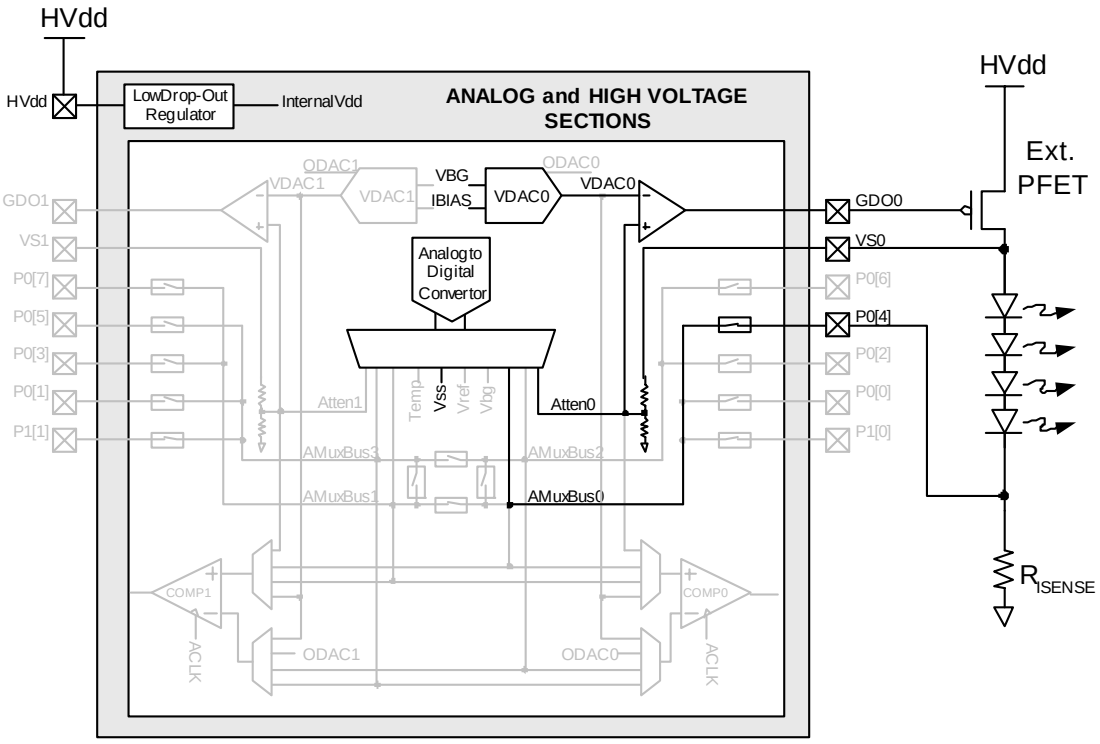


Figure 5-1. Linear White LED Driver

5.2 Linear Battery Charger

A battery charger is constant current and constant voltage power supply. At different points in a charging cycle a Lithium Ion battery requires a constant current or a constant voltage to be applied. The CY8C41x23 Linear Power PSoC can be configured as a constant voltage or constant current linear supply. In this configuration, the HV_{dd} voltage is high enough to drive one or more battery in series. Lithium Ion batteries have a fully charged voltage of 4.2V. With the two-cell configuration in *Figure 5-2*, HV_{dd} would have to be at least 8.4V (plus allowance for voltage losses in the FET and the current sense resistor, R_{ISENSE}). The HV_{dd} voltage is converted to 5V by the internal Low Drop-Out Regulator for use by the Power PSoC Core.

To maintain constant voltage, the gate of the External PFET is controlled by the GDO0 pin and driven in a linear mode. The voltage at the top of the load, connected to VS0, is attenuated by the internal resistive element, Atten0. The voltage out of the attenuator is fed into the positive terminal of an amplifier configured as a voltage follower. The amplifier's negative input is connected to the output of the voltage DAC, VDAC0. This creates a feedback loop that maintains the VS0 node at a voltage proportional to the VDAC0 setting. The Atten0 output is also connected to the ADC so the control software can monitor the output voltage. The accuracy of the ADC and the control loop are better than 0.75%. Meeting high accuracy is critical to Lithium Ion batteries.

To maintain constant current, the voltage across the R_{ISENSE} resistor is routed through pin P0[4] and AMuxBus0 to the ADC where it is monitored. The control software adjusts the VDAC0 setting, based on current sense measurements, to achieve the desired current through the load. The current sense voltage is also connected to the positive input of COMP0. The negative input of COMP0 is controlled by the output of ODAC0. If the current sense voltage exceeds the ODAC0 setting, the output of the comparator will be latched high. This acts as an over-current detection circuit, which can be cleared by the control software. The output of the comparator, COMP0, can be connected to the enable of the GDO0 output driver. This configures the Power PSoC so that an over-current condition will shut off the External PFET.

5.2.1 Resources

This application could connect the R_{ISENSE} resistor to any of the GPIO pins (P0[7:0] and P1[1:0]). The Linear Power PSoC still has all of its digital resources, half of the high voltage resources, one VDAC, two IDACs, seven of the analog multiplexer channels to the ADC, and over 90% of the CPU available to implement the battery charging algorithm and other tasks.

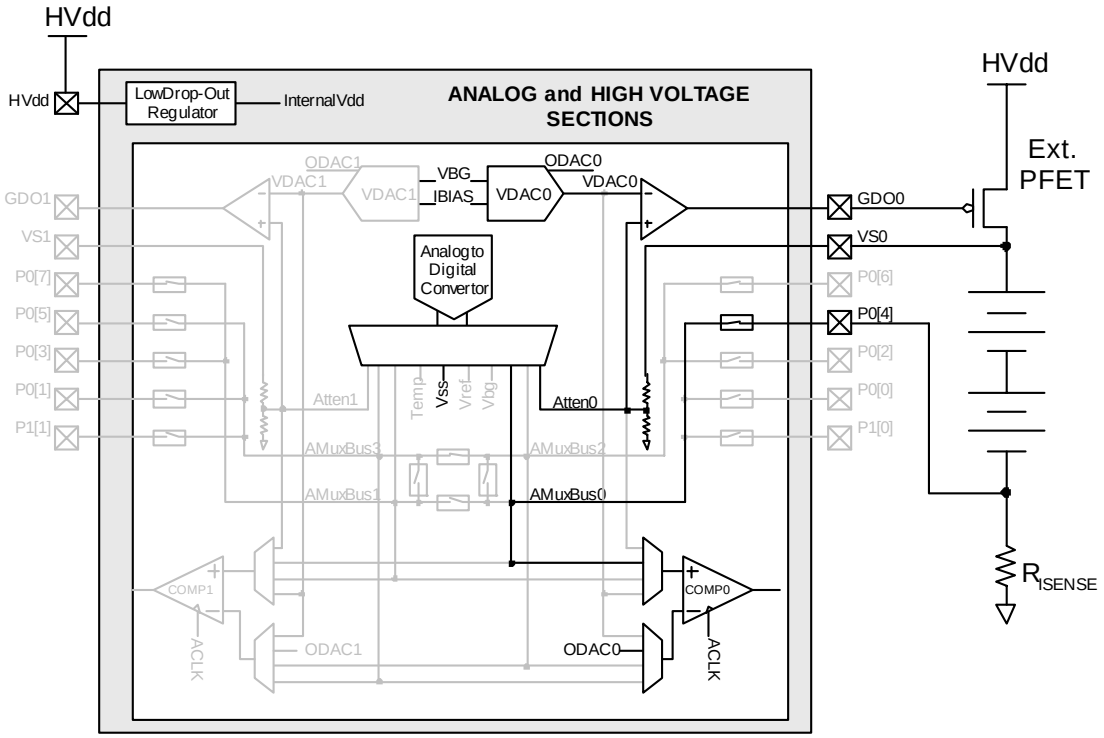


Figure 5-2. Linear Battery Charger

6.0 Pin Assignment

This section lists, describes, and illustrates all Linear Power PSoC device pins and pinout configurations. For up-to-date ordering, pinout, and packaging information, go to http://www.cypress.com/psoc.

6.1 Pinouts

PSoC devices are available in a variety of packages. Refer to the following information for details on individual devices. Every port pin (labeled with a “P”) in the following tables and illustrations is capable of digital IO.

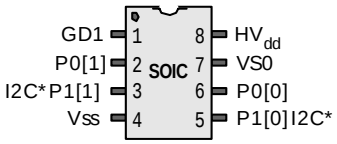
6.1.1 8-Pin SOIC Part Pinouts

The 8-pin SOIC part is for the CY8C41123 PSoC device.

8-Pin Part Pinout (SOIC)

Pin No.	Digital	Analog	Name	Description
1		HVO	GD1	High Side Linear Gate Driver 1
2	IO	I	P0[1]	
3	IO	I	P1[1]	I2C Clock*
4	Power		Vss	Ground Connection
5	IO	I	P1[0]	I2C Data*
6	IO	I	P0[0]	
7		HVI	VS0	High Voltage Sense 0
8	Power		HV_{dd}	Supply Voltage

CY8C41123 PSoC Device



LEGEND I = Input 5V Only, O = Output 5V Only, HV = High Voltage.

* These are the ISSP pins, which are not HighZ at POR (Power On Reset). See the *Power PSoC Mixed-Signal Array Technical Reference Manual* for details.

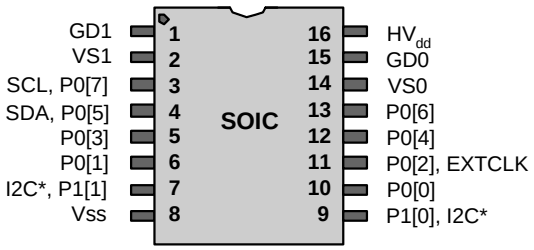
6.1.2 16-Pin SOIC Part Pinouts

The 16-pin SOIC part is for the CY8C41223 PSoC device.

16-Pin Part Pinout (SOIC)

Pin No.	Digital	Analog	Name	Description
1		HVO	GD1	High Side Linear Gate Driver 1
2		HVI	VS1	High Voltage Sense 1
3	IO	I	P0[7]	I2C Clock
4	IO	I	P0[5]	I2C Data
5	IO	I	P0[3]	
6	IO	I	P0[1]	
7	IO	I	P1[1]	I2C Clock*
8	Power		Vss	Ground Connection
9	IO	I	P1[0]	I2C Data*
10	IO	I	P0[0]	
11	IO	I	P0[2]	Optional External CLK Input (EXTCLK)
12	IO	I	P0[4]	
13	IO	I	P0[6]	
14		HVI	VS0	High Voltage Sense 0
15		HVO	GD0	High Side Linear Gate Driver 0
16	Power		HV_{dd}	Supply Voltage

CY8C41223 PSoC Device



LEGEND I = Input 5V Only, O = Output 5V Only, HV = High Voltage.

* These are the ISSP pins, which are not HighZ at POR (Power On Reset). See the *Power PSoC Mixed-Signal Array Technical Reference Manual* for details.

6.1.3 32-Pin QFN Part Pinouts

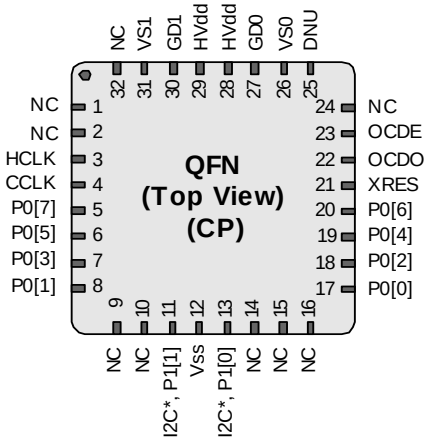
The 32-pin QFN part is for the CY8C41000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

32-Pin OCD Part Pinout (QFN**)

Pin No.	Digital	Analog	Name	Description
1			NC	No Connection
2			NC	No Connection
3	OCD		HCLK	On-Chip Debug Clock
4	OCD		CCLK	On-Chip Debug Clock
5	IO	I	P0[7]	I2C Clock
6	IO	I	P0[5]	I2C Data
7	IO	I	P0[3]	
8	IO	I	P0[1]	
9			NC	No Connection
10			NC	No Connection
11	IO	I	P1[1]	I2C Clock*
12	Power		Vss	
13	IO	I	P1[0]	I2C Data*
14			NC	No Connection
15			NC	No Connection
16			NC	No Connection
17	IO	I	P0[0]	
18	IO	I	P0[2]	Optional External CLK Input (EXTCLK)
19	IO	I	P0[4]	
20	IO	I	P0[6]	
21	I		XRES	External Reset
22	OCD		OCDO	On-Chip Debug Data
23	OCD		OCDE	On-Chip Debug Data
24			NC	No Connection
25			DNU	Do Not Use
26		HVI	VS0	High Voltage Sense 0
27	HVO	HVO	GD0	High Side Gate Driver 0
28	Power		HV_{dd}	Supply Voltage
29	Power		HV_{dd}	Supply Voltage
30	HVO	HVO	GD1	High Side Gate Driver 1
31		HVI	VS1	High Voltage Sense 1
32			NC	No Connection
CP	Power		Vss	Center Pad Must be Connected to Ground

CY8C41000 OCD PSoC Device



Not for Production

LEGEND I = Input 5V Only, O = Output 5V Only, HV = High Voltage, NC = No Connection, OCD = On-Chip Debug.

* These are the ISSP pins, which are not HighZ at POR (Power On Reset). See the *Power PSoC Mixed-Signal Array Technical Reference Manual* for details.

** The QFN package has a center pad that must be connected to ground (Vss).

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

7.0 Registers

This section discusses the registers of the Power PSoC device. It lists all the registers in mapping tables, in address order.

7.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

7.2 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASC00CR0	84	RW		C4	
PRT1IE	05	RW		45		ASC00CR1	85	RW		C5	
PRT1GS	06	RW		46		ASC00CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASC00CR3	87	RW	IDAC_D	C7	RW
HVP2_DR	08	RW		48		ASC01CR0	88	RW	P0_MUX	C8	RW
	09			49		ASC01CR1	89	RW	P1_MUX	C9	RW
	0A			4A		ASC01CR2	8A	RW		CA	
	0B			4B		ASC01CR3	8B	RW		CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	R	AC0_MUX	60	RW	PWR0_CR	A0	RW	INT_MSK0	E0	RW
DBC00DR1	21	W	AC0_CR0	61	RW	PWR1_CR	A1	RW	INT_MSK1	E1	RW
DBC00DR2	22	RW	AC0_CR1	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	RW	AC0_CR2	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	R	AC0_MSP	64	RW	AA_REF	A4	RW		E4	
DBC01DR1	25	W	AC0_LSP	65	RW		A5			E5	
DBC01DR2	26	RW	AC0_MSR	66	RW		A6			E6	
DBC01CR0	27	RW	AC0_LSR	67	RW	VDAC_CR	A7	RW		E7	
DBD02DR0	28	R	AC0_CC	68	#	VDAC_DR0	A8	RW		E8	
DBD02DR1	29	W		69		VDAC_DR1	A9	RW		E9	
DBD02DR2	2A	RW		6A			AA			EA	
DBD02CR0	2B	RW		6B			AB			EB	
DBD03DR0	2C	R	TMP_DR0	6C	RW		AC			EC	
DBD03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DBD03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBD03CR0	2F	RW	TMP_DR3	6F	RW		AF			EF	
	30		CMP_SYN	70	RW	RDI0RI	B0	RW		F0	
	31		CMP_LFN0	71	RW	RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33		CMP_LMD	73	RW	RDI0LT0	B3	RW		F3	
	34		CMP_CDS	74	RW	RDI0LT1	B4	RW		F4	
	35		CMP_CIS	75	RW	RDI0RO0	B5	RW		F5	
	36		CMP_RDC	76	RW	RDI0RO1	B6	RW		F6	
	37		CMP_GOEN0	77	RW	RDI0GF	B7	RW	CPU_F	F7	RL
	38			78			B8			F8	
	39		CMP_CLK	79	RW		B9			F9	
	3A		CMP_CR	7A	RW		BA			FA	
	3B		CMP_SRC	7B	RW		BB			FB	
	3C		CMP_MUX0	7C	RW		BC			FC	
	3D		CMP_MUX1	7D	RW		BD		CPU_SCR2	FD	RSW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

7.3 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87		IDAC_CR	C7	RW
HVP2_DM0	08	RW		48			88			C8	
HVP2_DM1	09	RW		49			89			C9	
HVP2_DS0	0A	RW		4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94		AC0_GOEN	D4	RW
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		AC0_CLK	D8	RW
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		SLP_CR0	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		SLP_CR1	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		SLP_CR2	A2	RW	OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
DBC01FN	24	RW		64		BUS_TOP	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW		65			A5			E5	
DBC01OU	26	RW		66			A6			E6	
	27			67			A7			E7	
DBD02FN	28	RW		68		VDAC_TR	A8	RW	IMO_TR	E8	W
DBD02IN	29	RW		69		VDAC_ITRIP0	A9	RW	LSO_TR	E9	RW
DBD02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB			EB	
DBD03FN	2C	RW	TMP_DR0	6C	RW	RDIV0	AC	RW		EC	
DBD03IN	2D	RW	TMP_DR1	6D	RW		AD		AA_TR	ED	RW
DBD03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33			73		RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36			76		RDI0RO1	B6	RW		F6	
	37			77		RDI0GF	B7	RW	CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		CPU_SCR2	FD	RSW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

8.0 Electrical Specifications

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

8.1 Frequencies

Refer to Table 8.4 for the electrical specifications on the internal main oscillator (IMO) using slow IMO (SLIMO) mode, which is set using the CPU_SCR1 register.

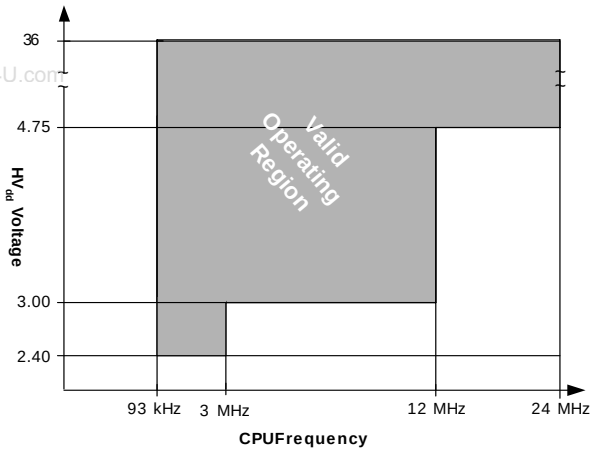


Figure 8-1a. Supply Voltage versus CPU Frequency

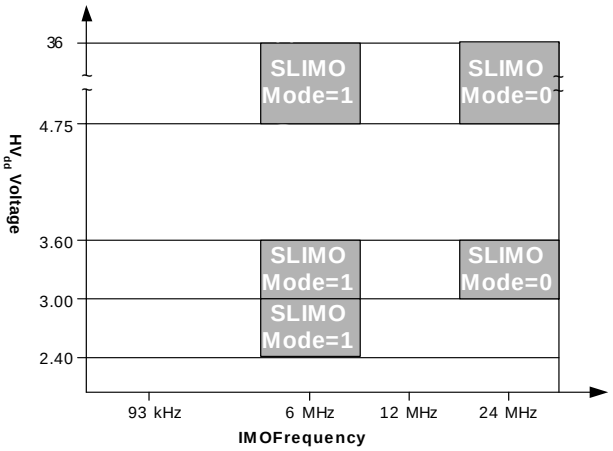


Figure 8-1b. IMO Frequency Trim Options

8.2 Absolute Maximum Ratings[a]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T_{STG}	Storage Temperature	Higher storage temperatures will reduce data retention time.	-50	–	+100	°C
T_A	Ambient Temperature with Power Applied		-40	–	+85	°C
HV_{dd}	Supply Voltage on HV_{dd} Relative to Vss		-0.5	–	+40	V
V_{GPIO}	DC Input to any Low Voltage Input Pin	HV_{dd} ≤ 5.0V.	-0.5	–	HV_{dd} + 0.5	V
V_{GPIO36}	DC Input to any Low Voltage Input Pin	HV_{dd} > 5.0V.	-0.5	–	5.5	V
V_{GD}	DC Input to any Gate Drive Pin		HV_{dd} - 5.5	–	HV_{dd} + 0.5	V
V_{VS}	DC Input to High Voltage Sense Pin		-0.5	–	HV_{dd} + 0.5	
V_{HVO}	DC Applied to High Voltage Outputs in High-Z State		-0.5	–	HV_{dd} + 0.5	
I_{MIO}	Maximum Current into any Low Voltage Port Pin		-25	–	+50	mA
I_{MIOHV}	Maximum Current into any High Voltage Port Pin		-50	–	+50	mA

8.2 Absolute Maximum Ratings[a] (continued)

I_{MIOGD}[b]	Maximum Current into any Gate Drive Pin		-10	–	10	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD.	2000	–	–	V
ESD_{HV}	Electro Static Discharge to High Voltage Port Pin	Human Body Model ESD.	2000	–	–	V
LU	Latch-up Current		–	–	200	mA

a. Operation at these conditions degrades reliability.
b. Cannot result in pin voltage exceeding V_{GD} limits or thermal specifications being exceeded.

8.3 Operating Temperature

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T_A	Ambient Temperature		-40	–	+85	^oC
T_J	Junction Temperature	The temperature rise from ambient to junction is package specific. See “Thermal Impedances per Package” on page 32. The system designer must limit the power consumption to comply with this requirement.	-40	–	+100	^oC

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.4 DC Chip-Level Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
HV_{dd}	Supply Voltage	See DC POR and LVD specifications table 8.14 on page 20.	2.5	–	36	V
I_{DD}	Supply Current, IMO = 24 MHz	Conditions are HV_{dd} = 5.0V, T_A = 25 ^oC, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.	–	3	4	mA
I_{DD36}	Supply Current, IMO = 24 MHz	Conditions are HV_{dd} = 36V, T_A = 25 ^oC, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.	–	3	4	mA
I_{DD3}	Supply Current, IMO = 6 MHz	Conditions are HV_{dd} = 3.3V, T_A = 25 ^oC, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz.	–	1.2	2	mA

8.4 DC Chip-Level Specifications (continued)

I_{DD27}	Supply Current, IMO = 6 MHz	Conditions are HV_{dd} = 2.7V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz, analog power = off. SLIMO mode = 1. IMO = 6 MHz.	–	1.1	1.5	mA
I_{RESET}	Supply Current while Reset	Conditions are HV_{dd} = 5.0V, -40 °C ≤ T_A ≤ 85 °C.	–	–	250	µA
I_{SBI}	Supply Current in Idle Mode	Conditions are with internal slow speed oscillator, HV_{dd} = 3.3V, -40 °C ≤ T_A ≤ 85 °C, analog power = off.	–	–	750	µA
I_{SB}	Supervised Sleep Current (POR, LVD, SleepTimer, WDT, and Voltage Regulation)	Conditions are with internal slow speed oscillator, HV_{dd} = 3.3V, -40 °C ≤ T_A ≤ 85 °C, analog power = off.	–	2.8	3	µA
I_{SBR}	Regulated Sleep Current (No POR, No LVD, but with SleepTimer, WDT, and Voltage Regulation)	Conditions are with internal slow speed oscillator, HV_{dd} = 3.3V, -40 °C ≤ T_A ≤ 85 °C, analog power = off.	–	–	1	µA
I_{SBW}	Watchdog Sleep Current (No POR, No LVD, No Sleep-Timer, No Voltage Regulation but with WDT)	Conditions are with internal slow speed oscillator, HV_{dd} = 3.3V, T_A = 25 °C, analog power = off.	–	0.5	–	µA
I_{SBD}	Deep Sleep Current (No POR, No LVD, No Sleep-Timer, No Voltage Regulation and No WDT	Conditions are bypass mode on, deep sleep enabled, HV_{dd} = 3.3V, T_A = 25 °C, analog power = off.	–	0.1	–	µA
I_{SBDHV}	Deep Sleep Current at HV (No POR, No LVD, No Sleep-Timer, No Voltage Regulation and No WDT	Conditions are analog power off, deep sleep enabled, HV_{dd} = 6V, T_A = 25 °C.	–	((HV_{dd} - 6) / 2) + 0.1	–	µA
V_{REF}	Reference Voltage (Bandgap)	Trimmed for HV_{dd} > 3.0V.	1.291	1.30	1.309	V
V_{REF27}	Reference Voltage (Bandgap)	Trimmed for HV_{dd} = 2.5V to 3.0V.	1.16	1.30	1.33	V

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.5 4.75V to 36V DC GPIO Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
R_{PU}	Pull-up Resistor		4	5.6	8	kΩ
R_{PD}	Pull-down Resistor		4	5.6	8	kΩ
V_{OH}[a]	High Output Level	IOH = 10 mA, HV_{dd} = 4.75V to 36V maximum 40 mA on even port pins (for example, P0[2], P1[0]), maximum 40 mA on odd port pins (for example, P0[3], P1[1]).	3.6	–	5.4	V
V_{OL}[a]	Low Output Level	IOL = 25 mA, HV_{dd} = 4.75V to 36V maximum 90 mA on even port pins (for example, P0[2], P1[0]), maximum 90 mA on odd port pins (for example, P0[3], P1[1]).	–	–	0.75	V
V_{IL}	Input Low Level	HV_{dd} = 4.75V to 36V.	–	–	0.8	V
V_{IH}	Input High Level	HV_{dd} = 4.75V to 36V.	2.1	–	–	V
V_H	Input Hysteresis		–	60	–	mV
I_{IL}	Input Leakage (Absolute Value)	Gross tested to 1 µA.	–	1	–	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF
I_{OH}[b]	Current Supplied while Maintaining 10% Regulation	4.5V ≤ V_{OH} ≤ 5.5V, HV_{dd} = 4.75V to 36V.	5.5	–	–	mA

a. IOH and IOL are also limited by the die temperature. See “Thermal Considerations” on page 31.
b. Odd and even port pins are regulated separately, therefore the current limit total applies separately to all odd port pins and to all even port pins.

8.6 3.0V to 5.0V DC GPIO Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
R_{PU}	Pull-up Resistor		4	5.6	8	kΩ
R_{PD}	Pull-down Resistor		4	5.6	8	kΩ
V_{OH}[a]	High Output Level	IOH = 8 mA, HV_{dd} = 3.0V to 3.6V maximum 30 mA on even port pins (for example, P0[2], P1[0]), maximum 30 mA on odd port pins (for example, P0[3], P1[1]).	HV_{dd} - 1.0	–	HV_{dd}	V
V_{OL}[a]	Low Output Level	IOL = 16 mA, HV_{dd} = 3.0V to 3.6V maximum 60 mA on even port pins (for example, P0[2], P1[0]), maximum 60 mA on odd port pins (for example, P0[3], P1[1]).	–	–	0.75	V
V_{IL}	Input Low Level	HV_{dd} = 3.0V to 3.6V.	–	–	0.8	V
V_{IH}	Input High Level	HV_{dd} = 3.0V to 3.6V.	2.1	–	–	V

8.6 3.0V to 5.0V DC GPIO Specifications (continued)

V_H	Input Hysteresis		–	60	–	mV
I_{IL}	Input Leakage (Absolute Value)	Gross tested to 1 µA.	–	1	–	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF

a. IOH and IOL are also limited by the die temperature. See “Thermal Considerations” on page 31.

8.7 2.5V to 3.0V DC GPIO Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
R_{PU}	Pull-up Resistor		4	5.6	8	kΩ
R_{PD}	Pull-down Resistor		4	5.6	8	kΩ
V_{OH}[a]	High Output Level	IOH = 2 mA, HV_{dd} = 2.5V to 3.0V maximum 16 mA on even port pins (for example, P0[2], P1[0]), maximum 16 mA on odd port pins (for example, P0[3], P1[1]).	HV_{dd} - 1.0	–	HV_{dd}	V
V_{OL}[a]	Low Output Level	IOL = 8 mA, HV_{dd} = 2.5V to 3.0V maximum 40 mA on even port pins (for example, P0[2], P1[0]), maximum 40 mA on odd port pins (for example, P0[3], P1[1]).	–	–	0.75	V
V_{IL}	Input Low Level	HV_{dd} = 2.5V to 3.0V.	–	–	0.8	V
V_{IH}	Input High Level	HV_{dd} = 2.5V to 3.0V.	2.0	–	–	V
V_H	Input Hysteresis		–	60	–	mV
I_{IL}	Input Leakage (Absolute Value)	Gross tested to 1 µA.	–	1	–	nA
C_{IN}	Capacitive Load on Pins as Input	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF
C_{OUT}	Capacitive Load on Pins as Output	Package and pin dependent. Temp = 25°C.	–	3.5	10	pF

a. IOH and IOL are also limited by the die temperature. See “Thermal Considerations” on page 31.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.8 DC Comparator Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OSSYN}	Input Offset Voltage in Synchronous Mode (Absolute Value)		–	–	100	µV
V_{OS}	Input Offset Voltage in Non-Synchronous Mode (Absolute Value)		–	2.5	15	mV
$I_{COMPSYN}$	Current Consumption in Synchronous Mode		–	100	200	µA
I_{COMP}	Current Consumption of Comparator	HV_{dd} = 2.5V to 36V.	–	10	30	µA
I_{COMPLP}	Current Consumption in Low Power Mode	HV_{dd} = 2.5V to 36V.	–	3	10	µA
V_{IN27}	Input Voltage Range	HV_{dd} = 2.5V to 5V.	0	–	HV_{dd}	V
V_{IN36}	Input Voltage Range	HV_{dd} = 5V to 36V.	0	–	5.0	V
V_{INLP27}	Input Voltage Range in Low Power Mode	HV_{dd} = 2.5V to 5V.	0	–	HV_{dd} -1.1	V
V_{INLP36}	Input Voltage Range in Low Power Mode	HV_{dd} = 5V to 36V.	0	–	3.9	V

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.9 DC Analog-to-Digital Converter Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OS}	Input Offset Voltage		–	–	100	µV
V_{IN}	Input Voltage Range	Voltage on Analog Mux Bus.	0	–	3	V
HV_{IN}	High Voltage Sense Input Range	Voltage on Analog Mux Bus.	0	–	HV_{dd}	V
R_{IN}	Input Impedance		–	100K	–	Ω
	Resolution		6	–	12	bits
INL	INL Error		–	–	1	LSb
DNL	DNL Error		–	–	1/2	LSb
	Absolute System Error[a]	Factory trimmed at ADC gains of 1/4, 1, 4, 16.	–	–	0.75%	

a. Maximum error is 11% for HV_{dd} = 2.5V to 3.0V; consistent with V_{REF27} specifications.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.10 DC Linear Control Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OS}	Comparator Input Offset Voltage		–	–	100	µV
RATIO1	Attenuation Resistor Ratio[a]		–	4	–	
RATIO2	Attenuation Resistor Ratio[a]		–	8	–	
RATIO3	Attenuation Resistor Ratio[a]		–	16	–	
R_{ATTEN}	Attenuator Resistance		–	400K	–	Ω
	Control Loop Reference Resolution	Full range is 0V to $V_{REF.}$	–	8	–	bits
V_{DAC}	Loop Control Reference Setting[a]		0	–	V_{REF}	V
V_{OC1}	Pre-Programmed Over-Current Set Point		120	150	180	mV
V_{OC2}	Pre-Programmed Over-Current Set Point		240	300	360	mV
V_{OC3}	Pre-Programmed Over-Current Set Point	With VDAC_CR Mode = 1.	360	450	540	mV
V_{OC4}	Pre-Programmed Over-Current Set Point	With VDAC_CR Mode = 1.	720	900	1080	mV

a. Error in this parameter is included in the Absolute System Error.

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.11 4.75V to 36V DC Linear Gate Drive[a]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OHGD}	High Output Voltage	HV_{dd} = 5V to 36V.	HV_{dd} - 0.1	–	–	V
V_{OLGD}	Low Output Voltage	HV_{dd} = 5V to 36V.	–	HV_{dd} - 5	–	V

a. To maintain the Absolute System Error per table 8.9, the current into or out of the Gate Drive Output must be less than 100 nA.

8.12 2.5V to 5V DC Linear Gate Drive

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OHGD}	High Output Voltage	IOH = 100 nA, HV_{dd} = 2.5V to 5V.	HV_{dd} - 0.1	–	–	V
V_{OLGD}	Low Output Voltage	IOL = 100 nA, HV_{dd} = 2.5V to 5V.	–	–	1.0	V

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.13 DC Analog Mux Bus Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
R_{SW}	Switch Resistance to Common Analog Bus	HV_{dd} ≥ 5V. HV_{dd} = 3.3V. HV_{dd} = 2.7V.	– – –	1000 1500 2000	– – –	Ω Ω Ω

The following table lists guaranteed maximum and minimum specifications for the temperature range: -40°C ≤ T_A ≤ 85°C. Typical parameters apply at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *Power PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT_CR register.

8.14 DC POR and LVD Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
	Vdd Value for PPOR Trip	Vdd must be greater than or equal to				
V_{PPOR0}	PORLEV[1:0] = 00b	2.6V during startup, reset from the	–	2.46	2.50	V
V_{PPOR1}	PORLEV[1:0] = 01b	XRES pin, or reset from Watchdog.	–	2.82	2.95	V
V_{PPOR2}	PORLEV[1:0] = 10b		–	4.55	4.70	V
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b		2.50	2.55	2.61[a]	V
V_{LVD1}	VM[2:0] = 001b		2.85	2.92	2.99[b]	V
V_{LVD2}	VM[2:0] = 010b		2.95	3.02	3.09	V
V_{LVD3}	VM[2:0] = 011b		3.06	3.13	3.20	V
V_{LVD4}	VM[2:0] = 100b		4.37	4.48	4.55	V
V_{LVD5}	VM[2:0] = 101b		4.50	4.64	4.75	V
V_{LVD6}	VM[2:0] = 110b		4.62	4.73	4.83	V
V_{LVD7}	VM[2:0] = 111b		4.71	4.81	4.95	V

a. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.

b. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.15 DC Programming Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations		2.80	–	–	V
I_{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V_{ILP}	Input Low Level During Programming or Verify		–	–	0.8	V
V_{IHP}	Input High Level During Programming or Verify		2.1	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	Driving internal pull-down resistor.	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	Driving internal pull-down resistor.	–	–	1.5	mA
V_{OLV}	Output Low Level During Programming or Verify		–	–	0.75	V
V_{OHV}	Output High Level During Programming or Verify	HV_{dd} = 2.5V to 5V.	HV_{dd} - 1.0	–	HV_{dd}	V
V_{OHV36}	Output High Level During Programming or Verify	HV_{dd} = 5V to 36V.	3.6	5.0	–	V
$Flash_{ENPB}$	Flash Endurance (per block)	Erase/write cycles per block.	50	–	–	KCycles
$Flash_{ENT}$	Flash Endurance (total)[a]	Erase/write cycles.	1,800	–	–	KCycles
$Flash_{DR}$	Flash Data Retention		10	–	–	Years

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.16 3.0V to 36V AC Chip-Level Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8-1b on page 12. SLIMO mode = 0.	23.4	24	24.6[a,b,c]	MHz
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8-1b on page 12. SLIMO mode = 1.	5.85	6	6.15[a,b,c]	MHz
F_{CPU1}	CPU Frequency (5V Nominal)		0.91	24	24.6[a,b]	MHz
F_{CPU2}	CPU Frequency (3.3V Nominal)		0.91	12	12.3[b,c]	MHz
F_{48M}	Digital PSoC Block Frequency	Refer to the AC Digital Block Specifications.	0	48	49.2[a,b,d]	MHz
F_{24M}	Digital PSoC Block Frequency		0	24	24.6[b,d]	MHz
F_{1K}	Internal Low Speed Oscillator Frequency		0.6	1	1.5	kHz
DC24M	24 MHz Duty Cycle		40	50	60	%
Step24M	24 MHz Trim Step Size		–	50	–	kHz
Fout48M	48 MHz Output Frequency	Trimmed. Utilizing factory trim values.	46.8	48.0	49.2[a,c]	MHz
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak		–	300	–	ps
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared		–	–	600	ps
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output		–	–	12.3	MHz
T_{RAMP}	Supply Ramp Time		0	–	–	µs
T_{SBI}	Wakeup Time from Idle Mode		–	–	0	µs
T_{SB}	Wakeup Time from Supervised Sleep		–	–	30	µs
T_{SBR}	Wakeup Time from Regulated Sleep		–	–	30	µs
T_{SBW}	Wakeup Time from Watchdog Sleep		–	–	400	µs
T_{SBD}	Wakeup Time from Deep Sleep		–	–	3	ms

a. 4.75V < HV_{dd} < 36V, -40°C ≤ T_A ≤ 70°C.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for HV_{dd} range.
c. 3.0V < HV_{dd} < 3.6V, -40°C ≤ T_A ≤ 70°C.
d. See the individual user module data sheets for information on maximum frequencies for user modules.

8.17 2.5V to 3.0V AC Chip-Level Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	Trimmed for 2.7V operation using factory trim values. See Figure 8-1b on page 12. SLIMO mode = 0.	11.5	12	12.5[a,b]	MHz
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	Trimmed for 2.7V operation using factory trim values. See Figure 8-1b on page 12. SLIMO mode = 1.	5.76	6	6.24[a,b]	MHz
F_{CPU1}	CPU Frequency (2.7V Nominal)		0.90	3	3.12[a]	MHz
F_{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	Refer to the AC Digital Block Specifications.	0	12	12.5[a,b]	MHz
F_{1K}	Internal Low Speed Oscillator Frequency		0.6	1	1.5	kHz
DC12M	12 MHz Duty Cycle		40	50	60	%
Jitter12M1P	12 MHz Period Jitter (IMO) Peak-to-Peak		–	340	–	ps
Jitter12M1R	12 MHz Period Jitter (IMO) Root Mean Squared		–	–	600	ps
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output		–	–	12.5	MHz
T_{RAMP}	Supply Ramp Time		0	–	–	µs

a. Accuracy derived from Internal Main Oscillator with appropriate trim for HV_{dd} range.
b. See the individual user module data sheets for information on maximum frequencies for user modules.

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.18 3.0V and 36V AC GPIO Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode.	0	–	12.5	MHz
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	HV_{dd} = 4.5 to 5.25V, 10% - 90%.	3	–	18	ns
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	HV_{dd} = 4.5 to 5.25V, 10% - 90%.	2	–	18	ns
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	HV_{dd} = 3 to 5.25V, 10% - 90%.	10	27	–	ns
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	HV_{dd} = 3 to 5.25V, 10% - 90%.	10	22	–	ns

8.19 2.5V to 3.0V AC GPIO Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode.	0	–	3.12	MHz
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	HV_{dd} = 2.5 to 3.0V, 10% - 90%.	6	–	50	ns
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	HV_{dd} = 2.5 to 3.0V, 10% - 90%.	6	–	50	ns
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	HV_{dd} = 2.5 to 3.0V, 10% - 90%.	18	40	120	ns
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	HV_{dd} = 2.5 to 3.0V, 10% - 90%.	18	40	120	ns

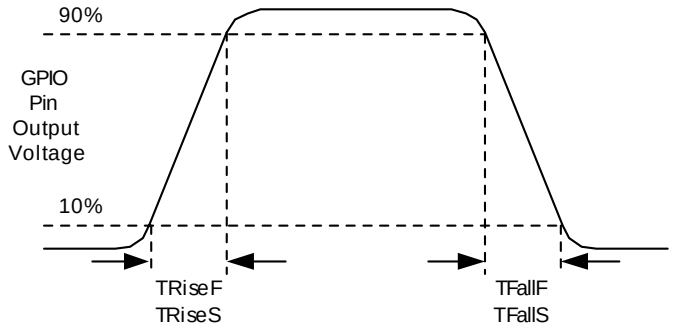


Figure 8-2. GPIO Timing Diagram

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.20 AC Comparator Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$T_{RSYNC27}$	Response Time in Synchronous Mode (50 mV Overdrive)	HV_{dd} = 2.5V to 3.0V. Output clocked at 12 MHz.	–	84	–	ns
$T_{RSYNC36}$	Response Time in Synchronous Mode (50 mV Overdrive)	HV_{dd} = 3.0V to 36V. Output clocked at 24 MHz.	–	42	–	ns
T_{R27}	Response Time (50 mV Overdrive)	HV_{dd} = 2.5V to 3.0V.	–	–	200	ns
T_{R36}	Response Time (50 mV Overdrive)	HV_{dd} = 3.0V to 36V.	–	–	100	ns
T_{RLP27}	Response Time in Low Power	HV_{dd} = 2.5V to 3.0V	–	–	400	ns
T_{RLP36}	Response Time in Low Power	HV_{dd} = 3.0V to 36V	–	–	200	ns

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.21 AC Analog-to-Digital Converter Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
	Sample Rate[a, b]	12 bits to 6 bits at 6 MHz.	1.46	–	93.75	Ksps
	8-Bit Sample Rate[b]		–	23.4	–	Ksps

a. Dependent on clock frequency and bit resolution. See individual user module data sheets.
b. For HV_{dd} = 2.5V to 3.0V, sample rates are halved. Bit BPEN in the AC0_CLK register must be set to 1.

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.22 3.0V to 36V AC Digital Block Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Timer	Capture Pulse Width		50[a]	–	–	ns
	Maximum Frequency (Capture Not Used)	4.75V < HV_{dd} < 36V.	–	–	49.9	MHz
	Maximum Frequency (With or Without Capture)	3.0V < HV_{dd} < 36V.	–	–	25.0	MHz
Counter	Enable Pulse Width		50[a]	–	–	ns
	Maximum Frequency (Enable Not Used)	4.75V < HV_{dd} < 36V.	–	–	49.9	MHz
	Maximum Frequency (With or Without Enable Input)	3.0V < HV_{dd} < 36V.	–	–	25.0	MHz

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

8.23 2.5V to 3.0V AC Digital Block Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Timer	Capture Pulse Width		100[a]	–	–	ns
	Maximum Frequency		–	–	12.5	MHz
Counter	Enable Pulse Width		100[a]	–	–	ns
	Maximum Frequency		–	–	12.5	MHz

a. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.24 4.75V to 36V AC Linear Gate Drive

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load		0.8	–	–	MHz

8.25 3.0V to 5.0V AC Linear Gate Drive

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load		0.7	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load		200	–	–	kHz

8.26 2.5V to 3.0V AC Linear Gate Drive

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load		0.6	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load		180	–	–	kHz

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.27 4.75V to 36V AC External Clock Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OSCEXT}	Frequency		0.090	–	25.0	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

8.28 3.0V to 5.0V AC External Clock Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[a]		0.090	–	12.5	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[b]		0.180	–	25.0	MHz
–	High Period with CPU Clock divide by 1		41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1		41.7	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

8.29 2.5V to 3.0V AC External Clock Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OSCEXT}	Frequency with CPU Clock divide by 1[a]		0.090	–	3.12	MHz
F_{OSCEXT}	Frequency with CPU Clock divide by 4 or greater[b]		0.180	–	12.5	MHz
–	High Period with CPU Clock divide by 1		41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1		41.7	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

a. Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 4 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.30 AC Programming Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	20	–	ms
T_{WRITE}	Flash Block Write Time		–	20	–	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	HV_{dd} > 3.6	–	–	45	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	3.0 ≤ HV_{dd} ≤ 3.6	–	–	50	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	2.5 ≤ HV_{dd} ≤ 3.0	–	–	70	ns

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.31 3.0V to 36V AC Characteristics of I2C SDA and SCL Pins

Parameter	Description	Conditions	Standard Mode		Fast Mode		Units
			Min.	Max.	Min.	Max.	
F_{SCLI2C}	SCL Clock Frequency		0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock		4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock		4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition		4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time		0	–	0	–	µs
$T_{SUDATI2C}$	Data Set-up Time		250	–	100[a]	–	ns
$T_{SUSTOI2C}$	Set-up Time for STOP Condition		4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition		4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.		–	–	0	50	ns

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 36V and -40°C ≤ T_A ≤ 85°C (referred to as 5V operation), 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C (referred to as 3.3V operation), or 2.5V to 3.0V and -40°C ≤ T_A ≤ 85°C (referred to as 2.7V operation), respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

8.32 2.5V to 3.0V AC Characteristics of I2C SDA and SCL Pins (Fast Mode not Supported)

Parameter	Description	Conditions	Standard Mode		Units
			Min.	Max.	
F_{SCLI2C}	SCL Clock Frequency		0	100	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		4.0	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock		4.7	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock		4.0	–	µs
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition		4.7	–	µs
$T_{HDDATI2C}$	Data Hold Time		0	–	µs
$T_{SUDATI2C}$	Data Set-up Time		250	–	ns
$T_{SUSTOI2C}$	Set-up Time for STOP Condition		4.0	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition		4.7	–	µs

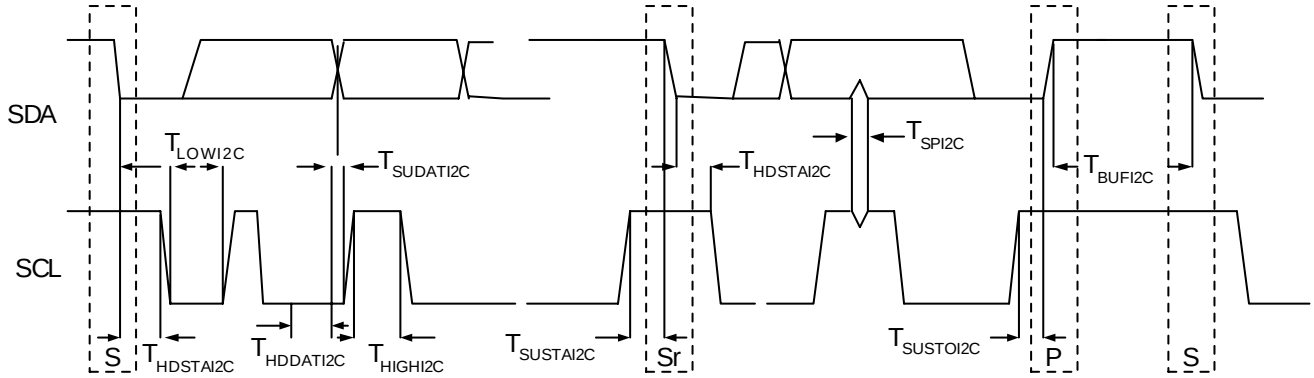


Figure 8-3. Definition for Timing for Fast/Standard Mode on the I2C Bus

9.0 Thermal Considerations

The Linear Power PSoC device can support a supply voltage up to 36V. An internal linear regulator provides the nominal 5 volts used to power the M8C processor and other internal resources. Because regulating to a lower voltage generates excess heat, care must be taken to not exceed the maximum junction temperature of the PSoC device when using higher supply voltages.

The junction temperature depends on the ambient temperature, the amount of power being dissipated in the device and the thermal resistance (θ_{JA}) of the package. In Linear Power PSoC devices, dissipated power can be broken into four sources: the PSoC core (CPU, PSoC blocks and system resources), the General Purpose Inputs/Outputs (GPIO), and the Gate Drive outputs (GD). The equation for junction temperature is shown in Equation 1, where θ_{JA} is the thermal resistance of the device package.

$$T_J = T_A + \theta_{JA} * (P_{Core} + P_{GPIO} + P_{GD})$$

Equation 1

The core power dissipated in the PSoC is the supply voltage (HV_{dd}) times the combined current of: the CPU, digital blocks, analog blocks and system resources (I_{dd}). The equation for the PSoC core power dissipation is:

$$P_{Core} = HV_{dd} * I_{dd}$$

Equation 2

The power dissipated in the PSoC due to the GPIO can be divided into two elements: current being sourced and current being sunk. Because V_{OL} is a relatively small value (less than 1V), the sinking current will not be a major contributor to heat in the Linear Power PSoC.

However, HV_{dd} - V_{OH} can be quite large and current sourced by GPIO must be looked at carefully when using HV_{dd} voltages greater than 5V. The equation for GPIO power dissipation is shown in Equation 3, where I_{Sink} is the total current being sunk by GPIO pins, and I_{Source} is the total current being sourced by GPIO pins.

$$P_{GPIO} = V_{OL} * I_{Sink} + (HV_{dd} - V_{OH}) * I_{Source}$$

Equation 3

The power dissipated by the high voltage Gate Drives (GD0 and GD1) is divided into a current sink and current source element. With the GD pins, the (HV_{dd} - V_{OHGD}) component is relatively small and the V_{OLGD} component can be large (approximately HV_{dd} - 5V). Therefore, with the GD pins, care must be taken to consider the effects of sinking currents. The equation for GD power dissipation is shown in Equation 4, where I_{SinkGD} is the total current sunk by the GD pins, and $I_{SourceGD}$ is the total current sourced by the GD pins.

$$P_{GD} = V_{OLGD} * I_{SinkGD} + (HV_{dd} - V_{OHGD}) * I_{SourceGD}$$

Equation 4

The following figures show the effects of supply voltage and current on the temperature of the PSoC. *Figure 9-1a* shows the maximum current with a varied supply voltage at an ambient temperature of 70°C and *Figure 9-1b* shows the maximum current with a varied supply voltage at an ambient temperature of 85°C. The PSoC model used assumes I_{dd} = 5mA and all other current is sourced by GPIO.

Each curve in the figures shows the maximum I_{Source} that can be tolerated (T_J remains below the maximum limit) at various supply voltages between 2.5V and 36V, for a specific package. The maximum current is clipped at 85 mA due to drive limitations on the GPIO pins. The package types available with Linear Power PSoC devices are shown. Thermal resistance (θ_{JA}) for the packages can be found in Section 9.1 on page 32.

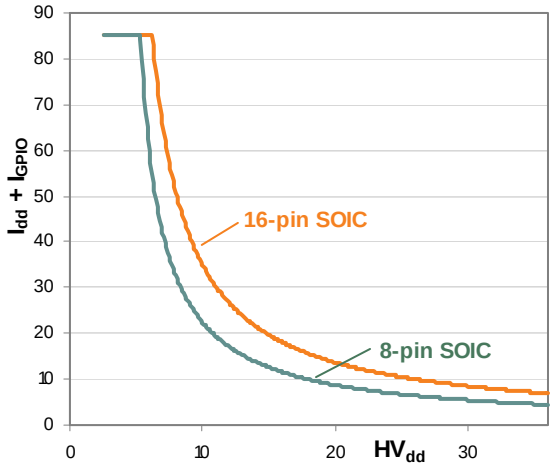


Figure 9-1a. Maximum Current vs. Supply Voltage by Package (70° Ambient)

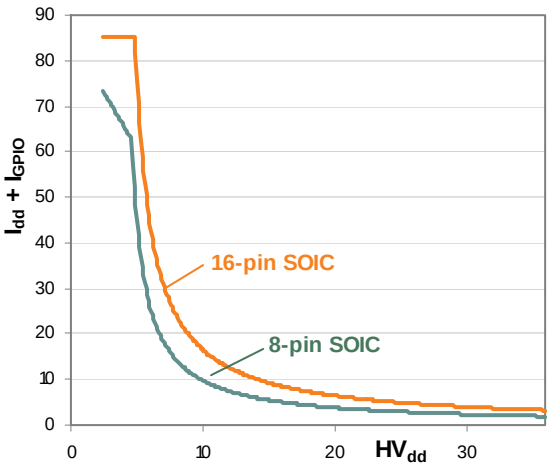


Figure 9-1b. Maximum Current vs. Supply Voltage by Package (85° Ambient)

9.1 Thermal Impedances per Package

Package	Typical θ_{JA} *
8 SOIC	186°C/W
16 SOIC	124°C/W
32 QFN	22°C/W

* Thermal resistance from silicon junction to ambient ($T_J = T_A$ + POWER x θ_{JA}).

9.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature*	Maximum Peak Temperature
8 SOIC	240°C	260°C
16 SOIC	240°C	260°C
32 QFN	240°C	260°C

* Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5°C with Sn-Pb or 245+/-5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

10.0 CY8C41x23 PSoC Device Key Features and Ordering Information

The following table lists the CY8C41x23 Power PSoC device's key package features and ordering codes .

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Power Blocks	Digital Blocks	Analog Channel	Digital IO Pins	HV GPO	XRES Pin
8-Pin SOIC	CY8C41123-24SXI	4K	256	-40°C to +85°C	2	4	2	4	0	No
8-Pin SOIC Tape and Reel	CY8C41123-24SXIT	4K	256	-40°C to +85°C	2	4	2	4	0	No
16-Pin SOIC	CY8C41223-24SXI	4K	256	-40°C to +85°C	2	4	2	10	0	No
16-Pin SOIC Tape and Reel	CY8C41223-24SXIT	4K	256	-40°C to +85°C	2	4	2	10	0	No
32-Pin OCD QFN*	CY8C41000-24LFXI*	4K	256	-40°C to +85°C	2	4	2	10	0	Yes

* This part is only used for in-circuit debugging. It is NOT available for production.

11.0 Package Diagrams

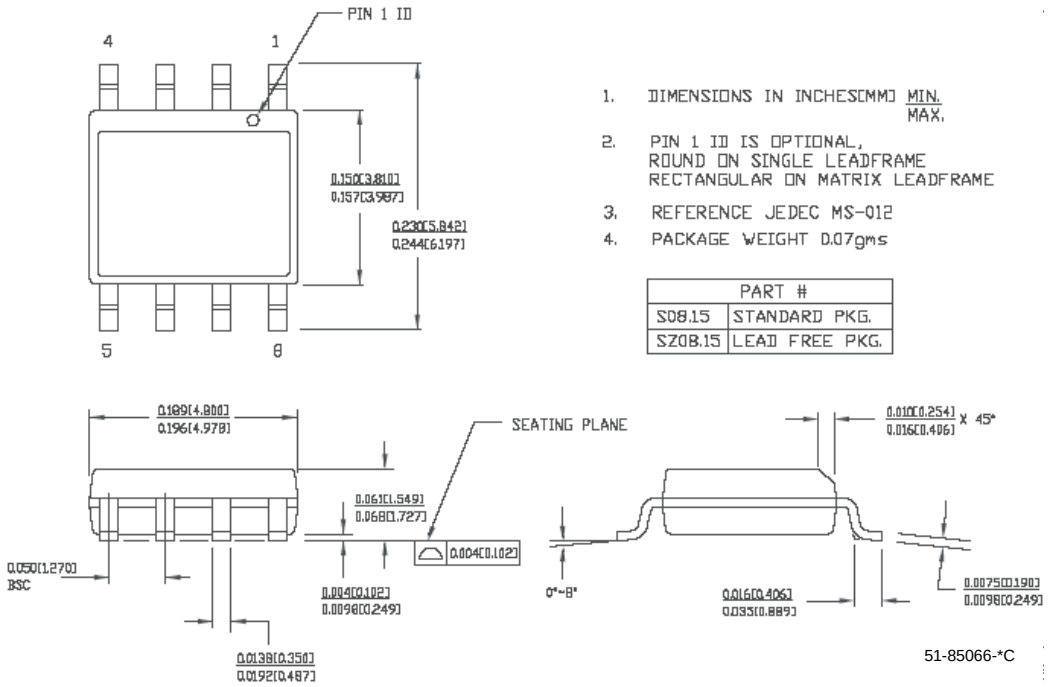


Figure 11-1. 8-Lead (150) SOIC

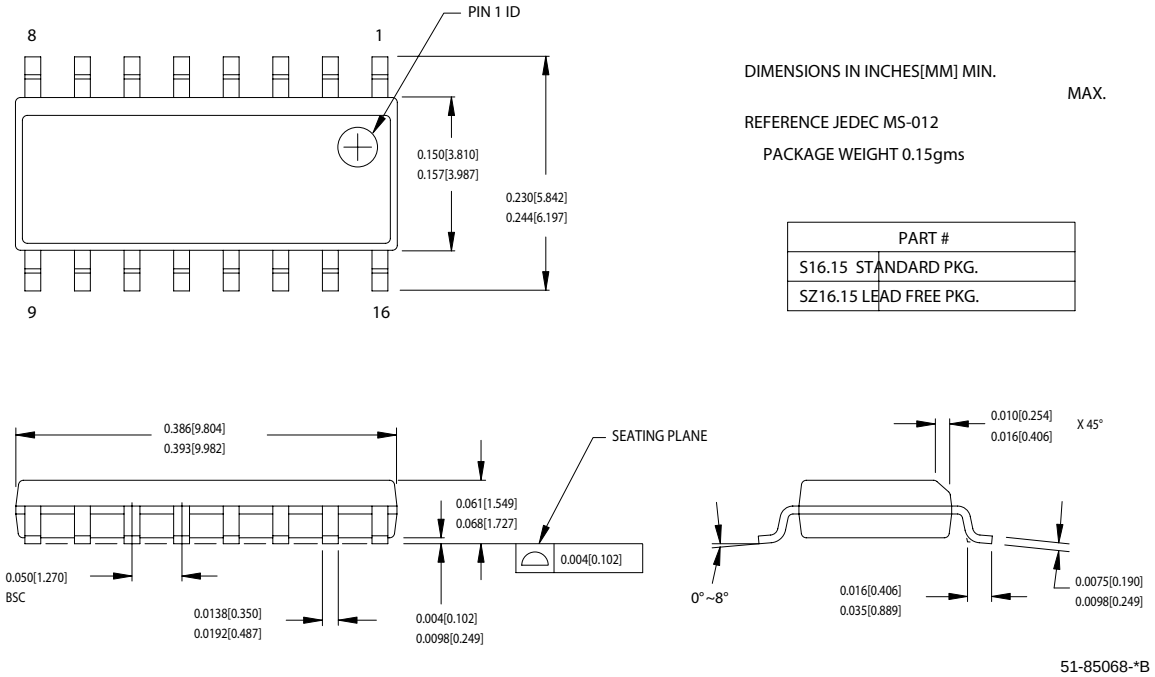
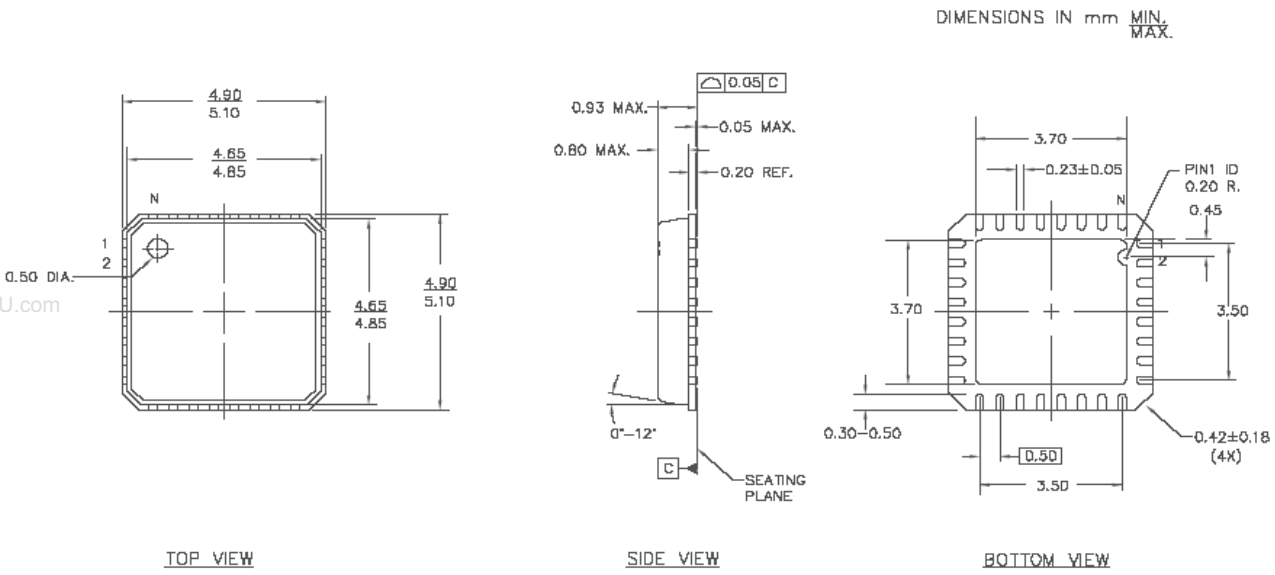


Figure 11-2. 16-Lead (150) SOIC



E-PAD X, Y for this product is 3.71 mm, 3.71 mm (+/-0.08 mm)

JEDEC # MO–220
Package Weight: 0.054 grams

51-85188 *A

Figure 11-3. 32-Lead (5x5 mm) QFN

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

To obtain information about Cypress Semiconductor or PSoC sales and technical support, reference the following information.

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Phone: 408.943.2600

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

Flash Code Protection Note the following details of the Flash code protection features on Cypress Semiconductor PSoC devices.

Cypress Semiconductor products meet the specifications contained in their particular data sheets. Cypress Semiconductor believes that its PSoC family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress Semiconductor, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress Semiconductor nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress Semiconductor is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress Semiconductor are committed to continuously improving the code protection features of our products.

Document History Page

Description Title: CY8C41123 and CY8C41223 Linear Power PSoC™ Devices Document Number: 001-00360				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	391186	See ECN	HMT	New data sheet. Preliminary for PR3.
*A	406572	See ECN	HMT	Add R_{ATTEN} to the DC Linear Control Specifications table. Add CY corporate address on Information page. Implement CY standard QFN package terminology.