

### REVISION HISTORY

| <u>Revision</u> | <u>Description</u>   | <u>Issue Date</u> |
|-----------------|--|-------------------|
| Rev. 1.0        | Initial Issued   | 2012/2/21         |
| Rev. 1.1        | 1. "CE# $\geq V_{CC} - 0.2V$ " revised as "CE# $\leq 0.2$ " for TEST CONDITION of Average Operating Power supply Current Icc1 on page3<br>2. Revised <b>ORDERING INFORMATION</b> Page11  | July.19. 2012     |
| Rev. 1.2        | 1. Revise "TEST CONDITION" for VOH, VOL on page 4<br>I <sub>OH</sub> = -8mA revised as -4mA<br>I <sub>OL</sub> =4mA revised as 8mA<br>2. Revise VIH(max) & VIL(min) note on page 4<br>VIH(max) = VCC + 2.0V for pulse width less than 6ns.<br>VIL(min) = VSS - 2.0V for pulse width less than 6ns. | June. 04. 2013    |
| Rev. 1.3        | Revised the address pin sequence of TSOP-II pin configuration on page 3 in order to be compatible with industry convention. (No function specifications and applications have been changed and all the characteristics are kept all the same as Rev 1.2 )  | Oct. 30. 2013     |

### FEATURES

- Fast access time : 8/10/12ns
  - **Very low power consumption:**  
 Operating current:  
   90/80/70mA(TYP. 8/10/12ns)  
 Standby current(Normal version):  
   3mA(TYP.)
  - Single 3.3V power supply
  - All inputs and outputs TTL compatible
  - Fully static operation
  - Tri-state output
  - Data retention voltage : 1.5V (MIN.)
  - **Green package available**
- Package : 44-pin 400 mil TSOP-II  
 48-ball 6mmx8mm TFBGA

### GENERAL DESCRIPTION

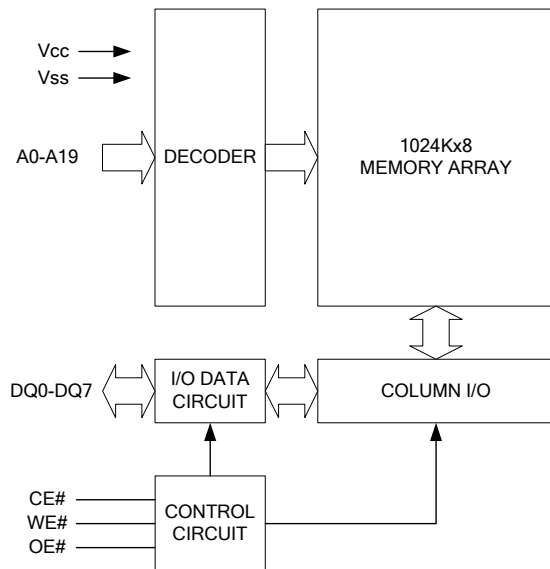
The LY61L10248A is a 8M-bit high speed CMOS static random access memory organized as 1,024K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY61L10248A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range  | Speed     | Power Dissipation               |                                   |
|----------------|-----------------------|------------|-----------|---------------------------------|-----------------------------------|
|                |                       |            |           | Standby(I <sub>SB1</sub> ,TYP.) | Operating(I <sub>CC1</sub> ,TYP.) |
| LY61L10248A    | 0 ~ 70°C              | 3.0 ~ 3.6V | 8/10/12ns | 3mA                             | 90/80/70mA                        |
| LY61L10248A(I) | -40 ~ 85°C            | 3.0 ~ 3.6V | 8/10/12ns | 3mA                             | 90/80/70mA                        |
| LY61L10248A    | 0 ~ 70°C              | 2.7 ~ 3.6V | 10/12ns   | 3mA                             | 80/70mA                           |
| LY61L10248A(I) | -40 ~ 85°C            | 2.7 ~ 3.6V | 10/12ns   | 3mA                             | 80/70mA                           |

### FUNCTIONAL BLOCK DIAGRAM

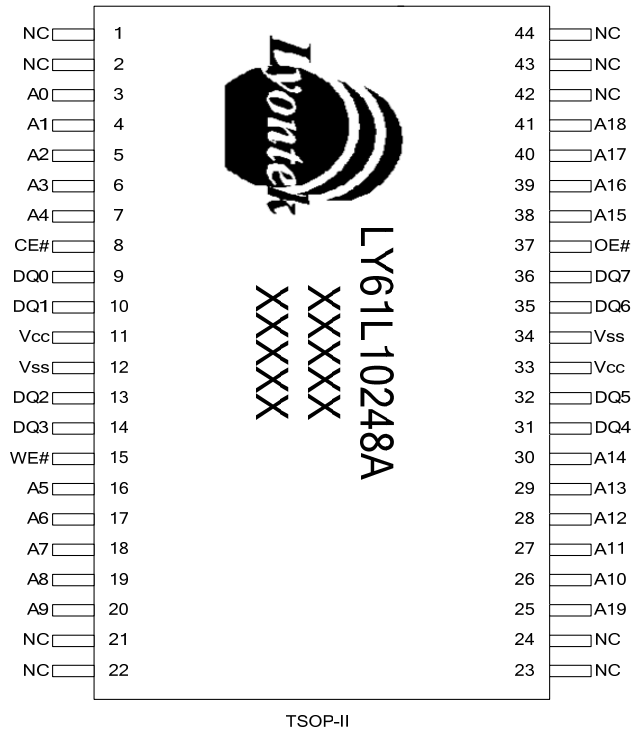


### PIN DESCRIPTION

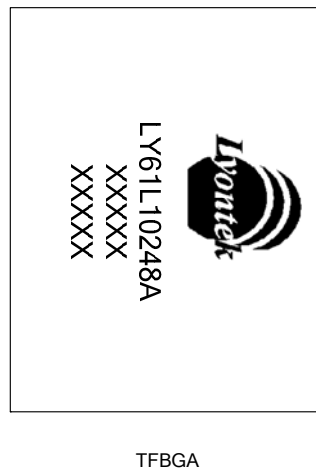
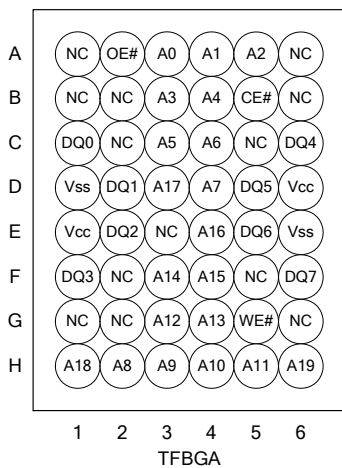
| SYMBOL    | DESCRIPTION         |
|-----------|---------------------|
| A0 - A19  | Address Inputs      |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE#       | Chip Enable Inputs  |
| WE#       | Write Enable Input  |
| OE#       | Output Enable Input |
| Vcc       | Power Supply        |
| Vss       | Ground              |
| NC        | No Connection       |

**PIN CONFIGURATION**

**44-pin TSOP(Type II)**



**48-ball 6mmx8mm TFBGA**



**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                | SYMBOL           | RATING                       | UNIT |
|--|------------------|------------------------------|------|
| Voltage on Vcc relative to Vss           | V <sub>T1</sub>  | -0.5 to 4.6                  | V    |
| Voltage on any other pin relative to Vss | V <sub>T2</sub>  | -0.5 to V <sub>CC</sub> +0.5 | V    |
| Operating Temperature                    | T <sub>A</sub>   | 0 to 70(C grade)             | °C   |
|  |                  | -40 to 85(I grade)           |      |
| Storage Temperature                      | T <sub>STG</sub> | -65 to 150                   | °C   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

| MODE           | CE# | OE# | WE# | I/O OPERATION    | SUPPLY CURRENT   |
|----------------|-----|-----|-----|------------------|------------------|
| Standby        | H   | X   | X   | High-Z           | I <sub>SB1</sub> |
| Output Disable | L   | H   | H   | High-Z           | I <sub>CC</sub>  |
| Read           | L   | L   | H   | D <sub>OUT</sub> | I <sub>CC</sub>  |
| Write          | L   | X   | L   | D <sub>IN</sub>  | I <sub>CC</sub>  |

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

| PARAMETER                              | SYMBOL                       | TEST CONDITION  | MIN.   | TYP. <sup>4</sup> | MAX.                 | UNIT |    |
|--|------------------------------|---|--------|-------------------|----------------------|------|----|
| Supply Voltage                         | V <sub>CC</sub>              |   | -8     | 3.0               | 3.3                  | 3.6  | V  |
|  |                              |   | -10/12 | 2.7               | 3.3                  | 3.6  | V  |
| Input High Voltage                     | V <sub>IH</sub> <sup>1</sup> |   | 2.2    | -                 | V <sub>CC</sub> +0.3 | V    |    |
| Input Low Voltage                      | V <sub>IL</sub> <sup>2</sup> |   | -0.3   | -                 | 0.8                  | V    |    |
| Input Leakage Current                  | I <sub>LI</sub>              | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>   | -1     | -                 | 1                    | μA   |    |
| Output Leakage Current                 | I <sub>LO</sub>              | V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> ,<br>Output Disabled                   | -1     | -                 | 1                    | μA   |    |
| Output High Voltage                    | V <sub>OH</sub>              | I <sub>OH</sub> = -4mA  | 2.4    | -                 | -                    | V    |    |
| Output Low Voltage                     | V <sub>OL</sub>              | I <sub>OL</sub> = 8mA   | -      | -                 | 0.4                  | V    |    |
| Average Operating Power supply Current | I <sub>CC</sub>              | CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA<br>;f=max                                    | -8     | -                 | 110                  | 140  | mA |
|  |                              |   | -10    | -                 | 100                  | 130  | mA |
|  |                              |   | -12    | -                 | 90                   | 120  | mA |
|  | I <sub>CC1</sub>             | CE# ≤ 0.2, Other pin is<br>at 0.2V or V <sub>CC</sub> -0.2V<br>I <sub>I/O</sub> = 0mA;f=max | -8     | -                 | 90                   | 120  | mA |
|  |                              |   | -10    | -                 | 80                   | 110  | mA |
|  |                              |   | -12    | -                 | 70                   | 100  | mA |
| Standby Power Supply Current           | I <sub>SB</sub>              | CE# ≥ V <sub>IH</sub><br>Other pin is at V <sub>IL</sub> or V <sub>IH</sub>                 | -      | -                 | 40                   | mA   |    |
| Standby Power Supply Current           | I <sub>SB1</sub>             | CE# ≥ V <sub>CC</sub> - 0.2V;<br>Other pin is at 0.2V or V <sub>CC</sub> -0.2V              | -      | 3                 | 25                   | mA   |    |

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 2.0V for pulse width less than 6ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

| PARAMETER                | SYMBOL           | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance        | C <sub>IN</sub>  | -    | 8   | pF   |
| Input/Output Capacitance | C <sub>I/O</sub> | -    | 10  | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

|  |  |
|--|--|
| speed                                    | 8ns/10/12ns  |
| Input Pulse Levels                       | 0.2V to V <sub>CC</sub> -0.2V  |
| Input Rise and Fall Times                | 3ns  |
| Input and Output Timing Reference Levels | 1.5V   |
| Output Load                              | C <sub>L</sub> = 30pF + 1TTL,<br>I <sub>OH</sub> /I <sub>OL</sub> = -4mA/8mA |

**AC ELECTRICAL CHARACTERISTICS**
**(1) READ CYCLE**

| PARAMETER                          | SYM.               | LY61L10248A<br>-8 |      | LY61L10248A<br>-10 |      | LY61L10248A<br>-12 |      | UNIT |
|------------------------------------|--------------------|-------------------|------|--------------------|------|--------------------|------|------|
|                                    |                    | MIN.              | MAX. | MIN.               | MAX. | MIN.               | MAX. |      |
| Read Cycle Time                    | t <sub>RC</sub>    | 8                 | -    | 10                 | -    | 12                 | -    | ns   |
| Address Access Time                | t <sub>AA</sub>    | -                 | 8    | -                  | 10   | -                  | 12   | ns   |
| Chip Enable Access Time            | t <sub>ACE</sub>   | -                 | 8    | -                  | 10   | -                  | 12   | ns   |
| Output Enable Access Time          | t <sub>OE</sub>    | -                 | 4.5  | -                  | 4.5  | -                  | 5    | ns   |
| Chip Enable to Output in Low-Z     | t <sub>CLZ</sub> * | 2                 | -    | 2                  | -    | 3                  | -    | ns   |
| Output Enable to Output in Low-Z   | t <sub>OLZ</sub> * | 0                 | -    | 0                  | -    | 0                  | -    | ns   |
| Chip Disable to Output in High-Z   | t <sub>CHZ</sub> * | -                 | 3    | -                  | 4    | -                  | 5    | ns   |
| Output Disable to Output in High-Z | t <sub>OHZ</sub> * | -                 | 3    | -                  | 4    | -                  | 5    | ns   |
| Output Hold from Address Change    | t <sub>OH</sub>    | 2                 | -    | 2                  | -    | 2                  | -    | ns   |

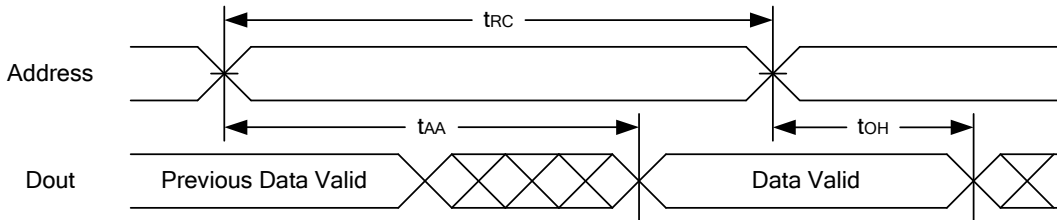
**(2) WRITE CYCLE**

| PARAMETER                        | SYM.               | LY61L10248A<br>-8 |      | LY61L10248A<br>-10 |      | LY61L10248A<br>-12 |      | UNIT |
|----------------------------------|--------------------|-------------------|------|--------------------|------|--------------------|------|------|
|                                  |                    | MIN.              | MAX. | MIN.               | MAX. | MIN.               | MAX. |      |
| Write Cycle Time                 | t <sub>WC</sub>    | 8                 | -    | 10                 | -    | 12                 | -    | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>    | 6.5               | -    | 8                  | -    | 10                 | -    | ns   |
| Chip Enable to End of Write      | t <sub>CW</sub>    | 6.5               | -    | 8                  | -    | 10                 | -    | ns   |
| Address Set-up Time              | t <sub>AS</sub>    | 0                 | -    | 0                  | -    | 0                  | -    | ns   |
| Write Pulse Width                | t <sub>WP</sub>    | 6.5               | -    | 8                  | -    | 10                 | -    | ns   |
| Write Recovery Time              | t <sub>WR</sub>    | 0                 | -    | 0                  | -    | 0                  | -    | ns   |
| Data to Write Time Overlap       | t <sub>DW</sub>    | 5                 | -    | 6                  | -    | 7                  | -    | ns   |
| Data Hold from End of Write Time | t <sub>DH</sub>    | 0                 | -    | 0                  | -    | 0                  | -    | ns   |
| Output Active from End of Write  | t <sub>OW</sub> *  | 2                 | -    | 2                  | -    | 2                  | -    | ns   |
| Write to Output in High-Z        | t <sub>WHZ</sub> * | -                 | 3    | -                  | 4    | -                  | 5    | ns   |

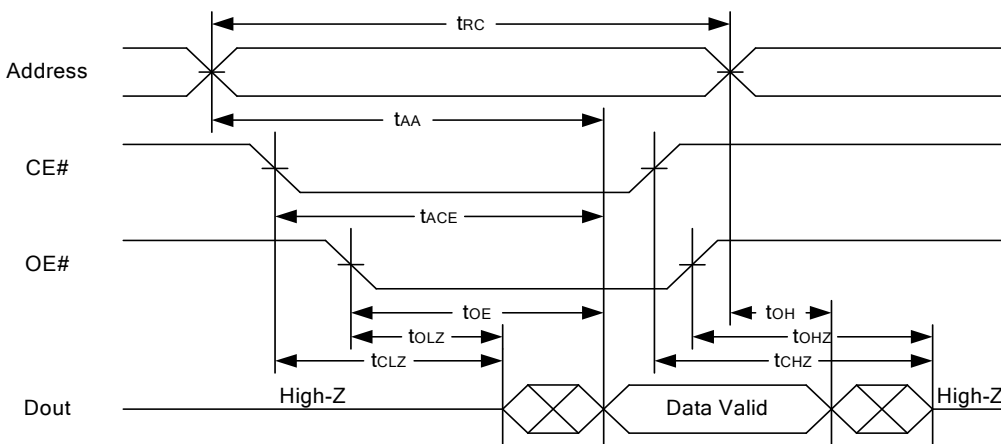
\*These parameters are guaranteed by device characterization, but not production tested.

**TIMING WAVEFORMS**

**READ CYCLE 1 (Address Controlled) (1,2)**



**READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, toLZ, tCHZ and toHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, toHZ is less than toLZ.



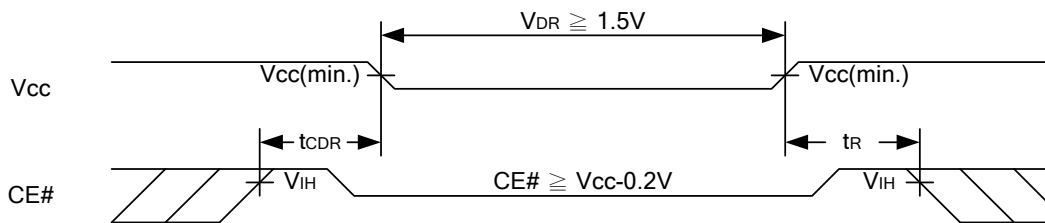


**DATA RETENTION CHARACTERISTICS**

| PARAMETER                           | SYMBOL           | TEST CONDITION   | MIN.              | TYP. | MAX. | UNIT |
|-------------------------------------|------------------|--|-------------------|------|------|------|
| V <sub>CC</sub> for Data Retention  | V <sub>DR</sub>  | CE# ≥ V <sub>CC</sub> - 0.2V   | 1.5               | -    | 3.6  | V    |
| Data Retention Current              | I <sub>DR</sub>  | V <sub>CC</sub> = 1.5V<br>CE# ≥ V <sub>CC</sub> - 0.2V;<br>Other pin is at 0.2V or V <sub>CC</sub> -0.2V | -                 | 3    | 25   | mA   |
| Chip Disable to Data Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)   | 0                 | -    | -    | ns   |
| Recovery Time                       | t <sub>R</sub>   |  | t <sub>RC</sub> * | -    | -    | ns   |

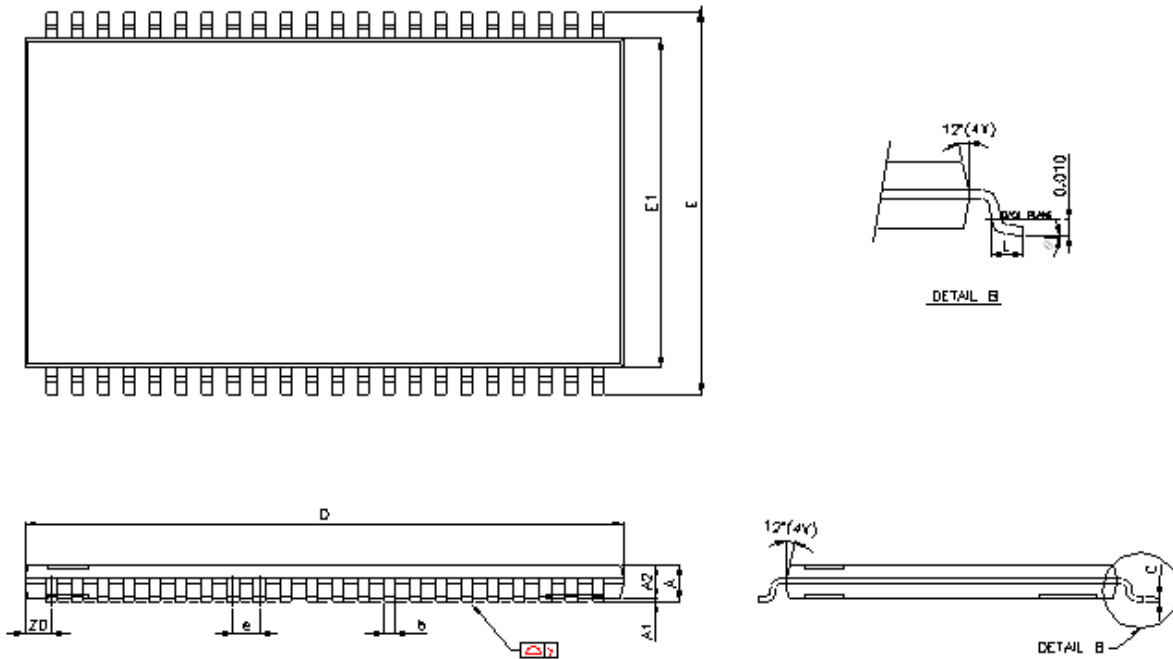
t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**



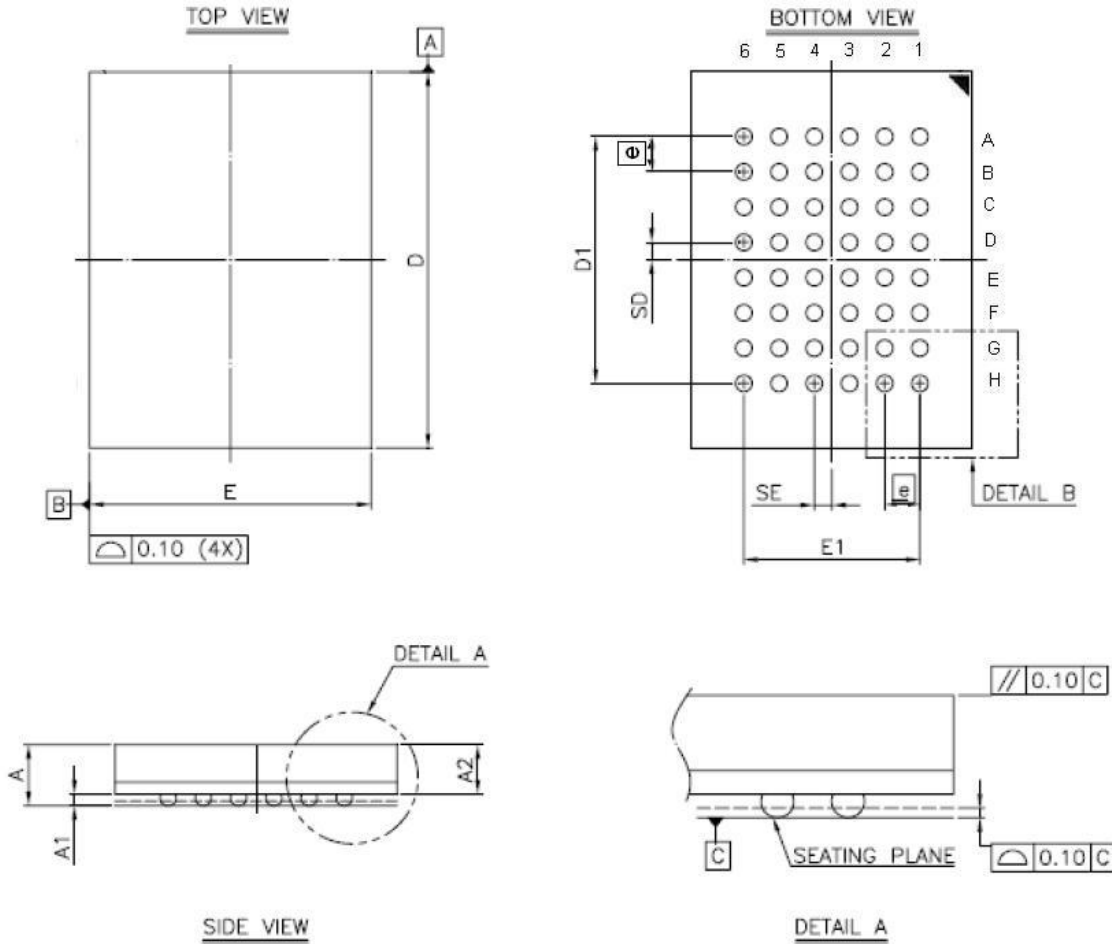
**PACKAGE OUTLINE DIMENSION**

44-pin 400mil TSOP-II Package Outline Dimension

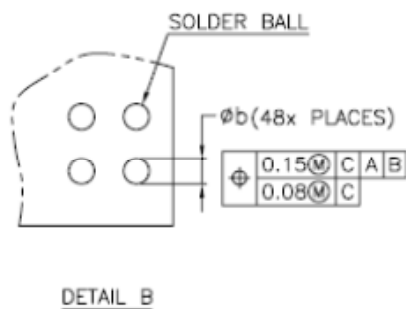


| SYMBOLS | DIMENSIONS IN MILLMETERS |        |        | DIMENSIONS IN MILS |      |      |
|---------|--------------------------|--------|--------|--------------------|------|------|
|         | MIN.                     | NOM.   | MAX.   | MIN.               | NOM. | MAX. |
| A       | -                        | -      | 1.20   | -                  | -    | 47.2 |
| A1      | 0.05                     | 0.10   | 0.15   | 2.0                | 3.9  | 5.9  |
| A2      | 0.95                     | 1.00   | 1.05   | 37.4               | 39.4 | 41.3 |
| b       | 0.30                     | -      | 0.45   | 11.8               | -    | 17.7 |
| c       | 0.12                     | -      | 0.21   | 4.7                | -    | 8.3  |
| D       | 18.212                   | 18.415 | 18.618 | 717                | 725  | 733  |
| E       | 11.506                   | 11.760 | 12.014 | 453                | 463  | 473  |
| E1      | 9.957                    | 10.160 | 10.363 | 392                | 400  | 408  |
| e       | -                        | 0.800  | -      | -                  | 31.5 | -    |
| L       | 0.40                     | 0.50   | 0.60   | 15.7               | 19.7 | 23.6 |
| ZD      | -                        | 0.805  | -      | -                  | 31.7 | -    |
| y       | -                        | -      | 0.076  | -                  | -    | 3    |
| θ       | 0°                       | 3°     | 6°     | 0°                 | 3°   | 6°   |

### 48-ball 6mm x 8mm TFBGA Package Outline Dimension



| SYM.      | DIMENSION (mm) |      |      | DIMENSION (inch) |       |       |
|-----------|----------------|------|------|------------------|-------|-------|
|           | MIN.           | NOM. | MAX. | MIN.             | NOM.  | MAX.  |
| A         | —              | —    | 1.40 | —                | —     | 0.055 |
| A1        | 0.20           | 0.25 | 0.30 | 0.008            | 0.010 | 0.012 |
| A2        | —              | —    | 1.05 | —                | —     | 0.041 |
| b         | 0.30           | 0.35 | 0.40 | 0.012            | 0.014 | 0.016 |
| D         | 7.95           | 8.00 | 8.05 | 0.313            | 0.315 | 0.317 |
| D1        | 5.25 BSC       |      |      | 0.207 BSC        |       |       |
| E         | 5.95           | 6.00 | 6.05 | 0.234            | 0.236 | 0.238 |
| E1        | 3.75 BSC       |      |      | 0.148 BSC        |       |       |
| SE        | 0.375 TYP      |      |      | 0.015 TYP        |       |       |
| SD        | 0.375 TYP      |      |      | 0.015 TYP        |       |       |
| $\square$ | 0.75 BSC       |      |      | 0.030 BSC        |       |       |


**NOTE:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

**ORDERING INFORMATION**

| Package Type              | Access Time (Speed)(ns) | Temperature Range(°C) | Packing Type | Lyontek Item No.   |
|---------------------------|-------------------------|-----------------------|--------------|--------------------|
| 44Pin(400mil)<br>TSOP-II  | 8                       | 0°C~70°C              | Tray         | LY61L10248AML-8    |
|                           |                         |                       | Tape Reel    | LY61L10248AML-8T   |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AML-8I   |
|                           |                         |                       | Tape Reel    | LY61L10248AML-8IT  |
|                           | 10                      | 0°C~70°C              | Tray         | LY61L10248AML-10   |
|                           |                         |                       | Tape Reel    | LY61L10248AML-10T  |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AML-10I  |
|                           |                         |                       | Tape Reel    | LY61L10248AML-10IT |
|                           | 12                      | 0°C~70°C              | Tray         | LY61L10248AML-12   |
|                           |                         |                       | Tape Reel    | LY61L10248AML-12T  |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AML-12I  |
|                           |                         |                       | Tape Reel    | LY61L10248AML-12IT |
| 48-ball(6mmx8mm)<br>TFBGA | 8                       | 0°C~70°C              | Tray         | LY61L10248AGL-8    |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-8T   |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AGL-8I   |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-8IT  |
|                           | 10                      | 0°C~70°C              | Tray         | LY61L10248AGL-10   |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-10T  |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AGL-10I  |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-10IT |
|                           | 12                      | 0°C~70°C              | Tray         | LY61L10248AGL-12   |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-12T  |
|                           |                         | -40°C~85°C            | Tray         | LY61L10248AGL-12I  |
|                           |                         |                       | Tape Reel    | LY61L10248AGL-12IT |

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