Four-Channel, Four-Quadrant Analog Multiplier

MLT04

FEATURES

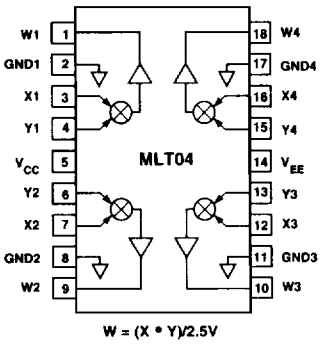
Four Independent Channels
Voltage IN, Voltage OUT
No External Parts Required
8 MHz Bandwidth
Four-Quadrant Multiplication
Voltage Output; W = (X × Y)/2.5 V
0.2% Typical Linearity Error on X or Y Inputs
Excellent Temperature Stability: 0.005%
±2.5 V Analog Input Range
Operates from ±5 V Supplies
Low Power Dissipation: 150 mW typ
Spice Model Available

APPLICATIONS

Geometry Correction in High-Resolution CRT Displays
Waveform Modulation & Generation
Voltage Controlled Amplifiers
Automatic Gain Control
Modulation and Demodulation

FUNCTIONAL BLOCK DIAGRAM

18-Lead Epoxy DIP (P Suffix)
18-Lead Wide Body SOIC (S Suffix)



GENERAL DESCRIPTION

The MLT04 is a complete, four-channel, voltage output analog multiplier packaged in an 18-pin DIP or SOIC-18. These complete multipliers are ideal for general purpose applications such as voltage controlled amplifiers, variable active filters, "zipper" noise free audio level adjustment, and automatic gain control. Other applications include cost-effective multiple-channel power calculations (I × V), polynomial correction generation, and low frequency modulation. The MLT04 multiplier is ideally suited for generating complex, high-order waveforms especially suitable for geometry correction in high-resolution CRT display systems.

Fabricated in a complementary bipolar process, the MLT04 includes four 4-quadrant multiplying cells which have been laser-trimmed for accuracy. A precision internal bandgap reference normalizes signal computation to a 0.4 scale factor. Drift over temperature is under 0.005%/°C. Spot noise voltage of 0.3 $\mu V/\sqrt{Hz}$ results in a THD + Noise performance of 0.02% (LPF = 22 kHz) for the lower distortion Y channel. The four 8 MHz channels consume a total of 150 mW of quiescent power.

The MLT04 is available in 18-pin plastic DIP, and SOIC-18 surface mount packages. All parts are offered in the extended industrial temperature range (–40°C to +85°C).

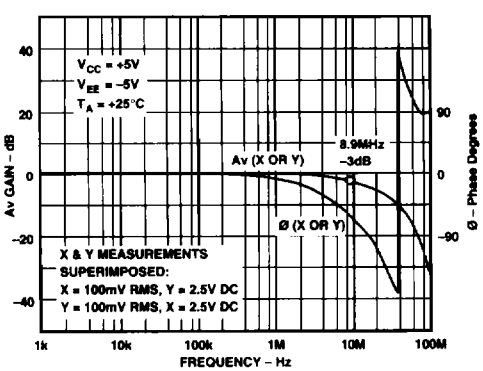


Figure 1. Gain & Phase vs. Frequency Response

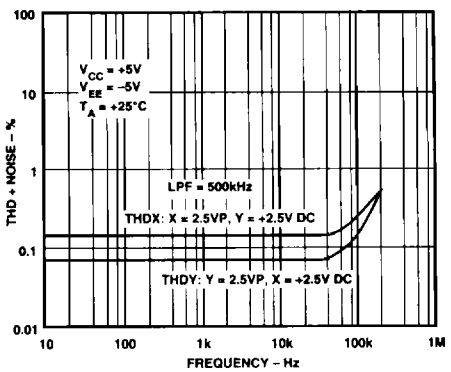


Figure 2. THD + Noise vs. Frequency

MLT04—SPECIFICATIONS (V_{CC} = +5 V, V_{EE} = −5 V, V_{IN} = ±2.5 V_P, R_L = 2 kΩ, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MULTIPLIER PERFORMANCE[1]						
Total Error[2] X	E_X	−2.5 V < X < +2.5 V, Y = +2.5 V	5	+2	5	% FS
Total Error[2] Y	E_Y	−2.5 V < Y < +2.5 V, X = +2.5 V	5	±2	5	% FS
Linearity Error[2] X	LE_X	−2.5 V < X < +2.5 V, Y = +2.5 V	1	±0.2	+1	% FS
Linearity Error[2] Y	LE_Y	−2.5 V < Y < +2.5 V, X = +2.5 V	1	±0.2	+1	% FS
Total Error Drift	TCE_X	X = −2.5 V, Y = 2.5 V, T_A = −40°C to +85°C		0.005		%/°C
Total Error Drift	TCE_Y	Y = −2.5 V, X = 2.5 V, T_A = −40°C to +85°C		0.005		%/°C
Scale Factor[3]	K	X = +2.5 V, Y = ±2.5 V, T_A = −40°C to +85°C	0.38	0.40	0.42	1/V
Output Offset Voltage	Z_{OS}	X = 0 V, Y = 0 V, T_A = −40°C to +85°C	50	±10	50	mV
Output Offset Drift	TCZ_{OS}	X = 0 V, Y = 0 V, T_A = −40°C to +85°C		50		µV/°C
Offset Voltage, X	X_{OS}	X = 0 V, Y = ±2.5 V, T_A = −40°C to +85°C	50	±10.5	50	mV
Offset Voltage, Y	Y_{OS}	Y = 0 V, X = ±2.5 V, T_A = −40°C to +85°C	50	±10.5	50	mV
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	BW	V_{OUT} = 0.1 V rms		8		MHz
Slew Rate	SR	V_{OUT} = ±2.5 V	30	53		V/µs
Settling Time	t_S	V_{OUT} = Δ2.5 V to 1% Error Band		1		µs
AC Feedthrough	FT_{AC}	X = 0 V, Y = 1 V rms @ f = 100 kHz		65		dB
Crosstalk @ 100 kHz	CT_{AC}	X = Y = 1 V rms Applied to Adjacent Channel		90		dB
OUTPUTS						
Audio Band Noise	E_N	f = 10 Hz to 50 kHz		76		µV rms
Wide Band Noise	E_N	Noise BW = 1.9 MHz		380		µV rms
Spot Noise Voltage	e_N	f = 1 kHz		0.3		µV/√Hz
Total Harmonic Distortion	THD_X	f = 1 kHz, LPF = 22 kHz, Y = 2.5 V		0.1		%
	THD_Y	f = 1 kHz, LPF = 22 kHz, X = 2.5 V		0.02		%
Open Loop Output Resistance	R_{OUT}			40		Ω
Voltage Swing	V_{PK}	V_{CC} = +5 V, V_{EE} = −5 V	±3.0	±3.3		V_P
Short Circuit Current	I_{SC}			30		mA
INPUTS						
Analog Input Range	IVR	GND = 0 V	2.5		+2.5	V
Bias Current	I_B	X = Y = 0 V		2.3	10	µA
Resistance	R_{IN}			1		MΩ
Capacitance	C_{IN}			3		pF
SQUARE PERFORMANCE						
Total Square Error	E_{SQ}	X = Y = 1		5		% FS
POWER SUPPLIES						
Positive Current	I_{CC}	V_{CC} = 5.25 V, V_{EE} = −5.25 V		15	20	mA
Negative Current	I_{EE}	V_{CC} = 5.25 V, V_{EE} = −5.25 V		15	20	mA
Power Dissipation	P_{DISS}	Calculated = 5 V × I_{CC} + 5 V × I_{EE}		150	200	mW
Supply Sensitivity	PSSR	X = Y = 0 V, V_{CC} = Δ5% or V_{EE} = Δ5%			10	mV/V
Supply Voltage Range	V_{RANGE}	For V_{CC} & V_{EE}	±4.75		±5.25	V

NOTES
[1]Specifications apply to all four multipliers.
[2]Error is measured as a percent of the ±2.5 V full scale, i.e., 1% FS = 25 mV.
[3]Scale Factor K is an internally set constant in the multipher transfer equation W = K × X × Y.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages V_{CC}, V_{EE} to GND ..... ±7 V
Inputs X_I, Y_I ..... V_{CC}, V_{EE}
Outputs W_I ..... V_{CC}, V_{EE}
Operating Temperature Range ..... −40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
PDIP-18 (N-18) ..... 74°C/W
SOIC-18 (SOL-18) ..... 89°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification are not implied.

ORDERING INFORMATION[1]

Model	Temperature Range	Package Description	Package Option[2]
MLT04GP	−40°C to +85°C	18-Pin P-DIP	N-18
MLT04GS	−40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GS-REEL	−40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GBC	+25°C	Die	

NOTES
[1]For die specifications contact your local Analog sales office. The MLT04 contains 211 transistors.
[2]For outline information see Package Information section.