MP1492

2A, 4.2V-16V Input, Fast Transient Synchronous Step-down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1492 is a fully integrated, high–efficiency 2A synchronous rectified step-down converter. The MP1492 operates at high efficiency over a wide output current load range. Adaptive Constant-On-Time (COT) control mode provides fast transient response, eases loop stabilization, and operates with a low-cost electrolytic capacitor.

The MP1492 requires a minimum number of readily available standard external components and is available in an 8-pin SOIC ROHS compliant package.

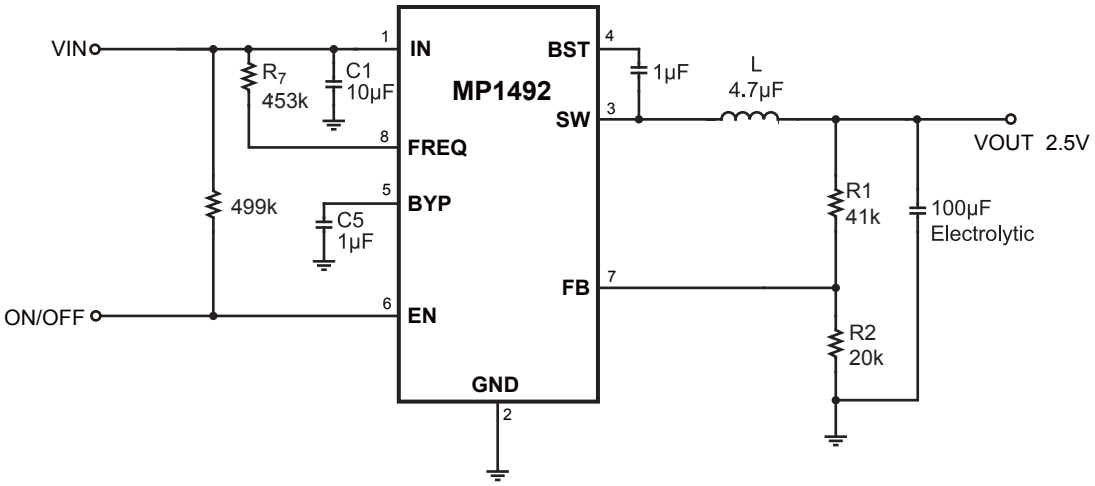
FEATURES

- Wide 4.2V to 16V Operating Input Range
- 2A Output Current
- Adaptive COT for Fast Transient Response
- Low R_{DS} (ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Programmable Switching Frequency
- OCP, SCP, OVP, UVP Protection and Thermal Shutdown
- Output Adjustable from 0.805V to 13V

APPLICATIONS

- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION

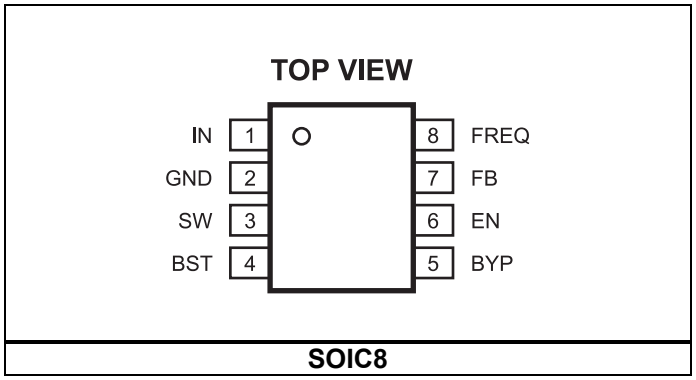


ORDERING INFORMATION

Part Number	OCP Protection	Package	Top Marking	Free Air Temperature (T_A)
MP1492DS*	Latch-off Mode	SOIC8	MP1492	-40°C to +85°C
MP1492DS-A**	Hiccup Mode		MP1492-A	

* For Tape & Reel, add suffix –Z (e.g. MP1492DS–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP1492DS–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP1492DS-A–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP1492DS-A–LF–Z)

PACKAGE REFERENCE



SOIC8

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 19V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8 ..... 1.39W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.2V to 16V
Output Voltage V_{OUT} ..... 0.805V to 13V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8	90	45	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN}=0V		5		μA
Supply Current (Quiescent, Not Switching)	I_{IN}	V_{EN}=2V, V_{FB}=0.9V		1		mA
HS Switch On Resistance	HS_{RDS-ON}			120		mΩ
LS Switch On Resistance	LS_{RDS-ON}			70		mΩ
Switch Leakage	SW_{LKG}	V_{EN}=0V [V_{SW}=0V or 12V]		0	10	μA
Current Limit (5)	I_{LIMIT}	After Soft-Start Time-out	3.0			A
One-Shot On Time	T_{ON}	R_7=300kΩ,V_{OUT}=1.2V		250		ns
Minimum Off Time	T_{OFF}			130	150	ns
Fold-back Off Time	T_{FB}	I_{LIM}=1		1.25		μs
OCP hold-off time	T_{OC}	I_{LIM}=1		50		μs
Feedback Voltage	V_{FB}		789	805	821	mV
Feedback Current	I_{FB}	V_{FB}=800mV		10	50	nA
Soft Start Time	T_{SS}			1		ms
EN Rising Threshold	VIL_{EN}		1.05	1.35	1.6	V
EN Threshold Hysteresis	VIL_{EN}			500		mV
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0		
VIN Under Voltage Lockout Threshold Rising	INUVVth				3.1	V
VIN Under Voltage Lockout Threshold Hysteresis	INUVHYS			300		mV
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

Note:

5) Guaranteed by design and characterization..

PIN FUNCTIONS

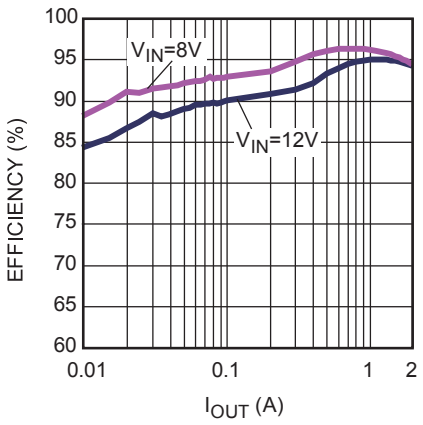
SOIC8 Pin #	Name	Description
1	IN	Supply Voltage. The MP1492 operates from a +4.2V to +16V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
3	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
4	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
5	BYP	Internal LDO output. Decouple with a 1μF ceramic capacitor. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	EN	EN=1 to enable the MP1492. For automatic start-up, connect EN pin to VIN with a pull-up resistor.
7	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
8	FREQ	Frequency. Setting Pin. Sets the full-load switching frequency driving CCM operation.. Connect a resistor R_7 to IN to set the switching frequency. An optional 1nF decoupling capacitor can be added to improve any switching frequency jitter that may be present.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=+25°C, unless otherwise noted.

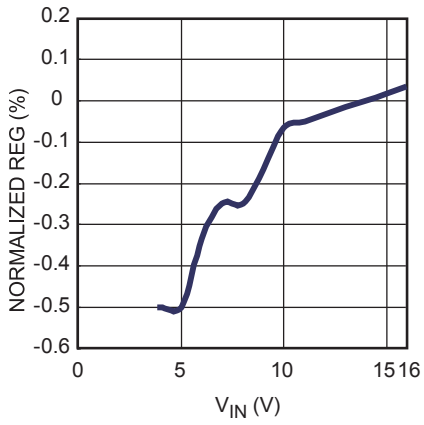
Efficiency

V_{OUT}=5V, f_s=600kHz, L=6.2µH

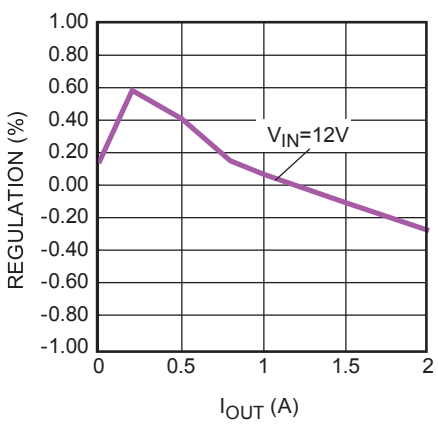


Line Regulation

I_{OUT}=2A

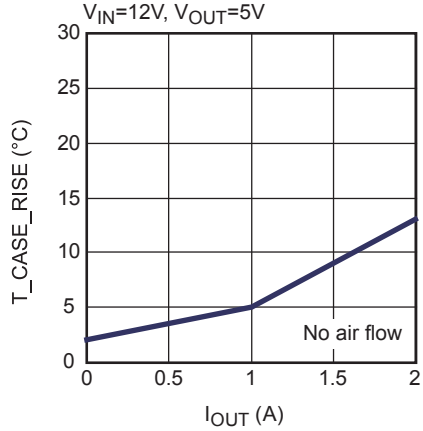


Load Regulation

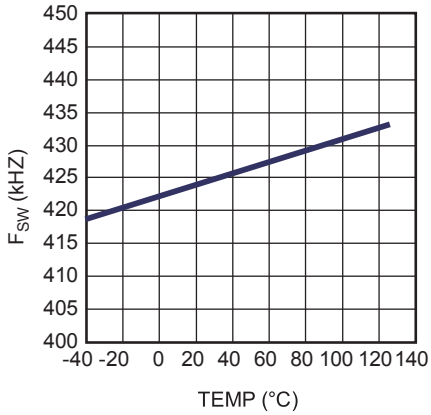


Case Temprature Rise vs. Load Current

V_{IN}=12V, V_{OUT}=5V

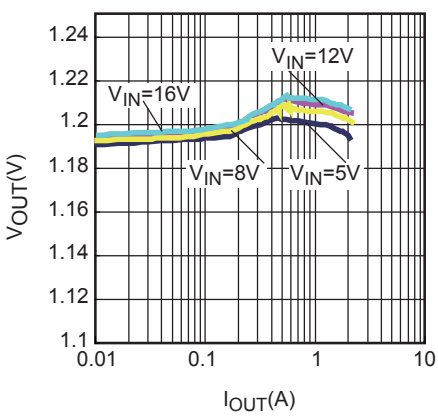


Frequency vs. Temperature



V_{OUT} VS. I_{OUT}

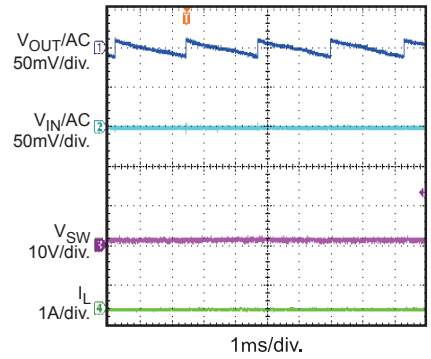
V_{OUT}=1.2V, Freq=500kHz



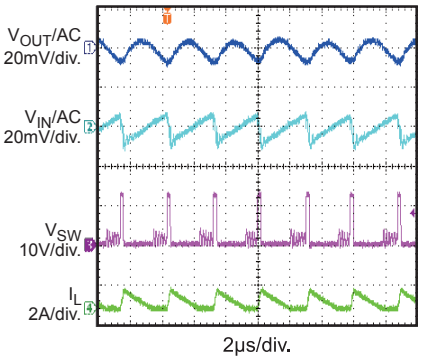
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=+25°C, unless otherwise noted.

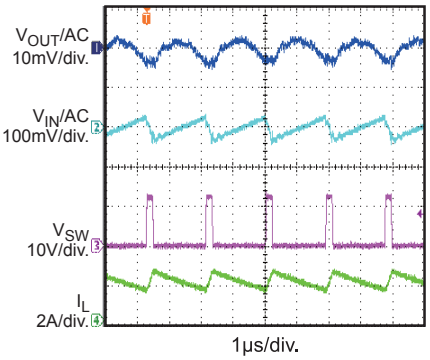
Input/Output Voltage Ripple
I_{OUT} = 0A



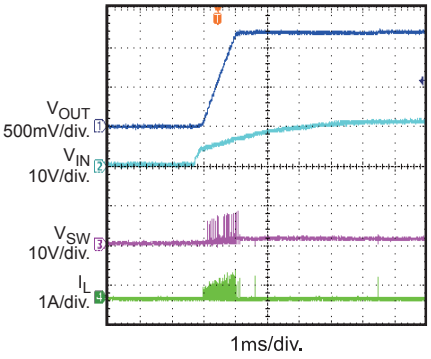
Input/Output Voltage Ripple
I_{OUT} = 0.3A



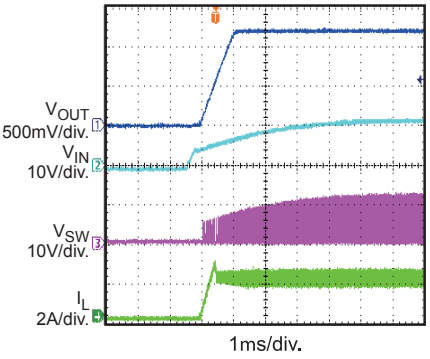
Input/Output Voltage Ripple
I_{OUT} = 2A



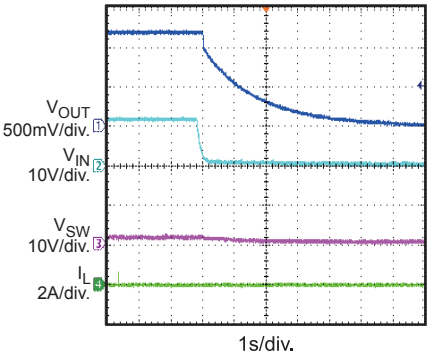
Start Up Through VIN
I_{OUT} = 0A



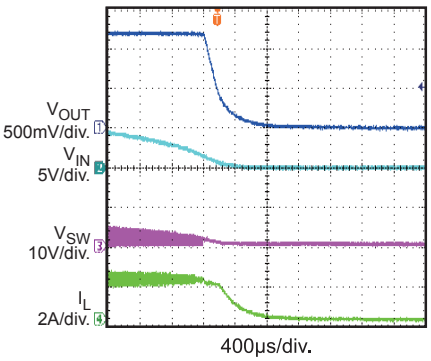
Start Up Through VIN
I_{OUT} = 2A



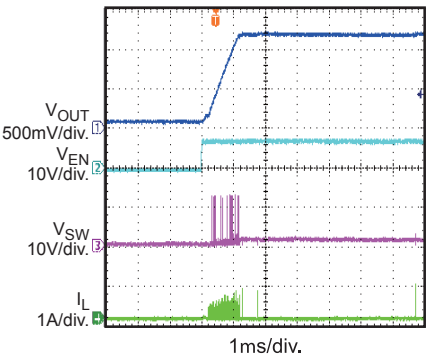
Shut Down Through VIN
I_{OUT} = 0A



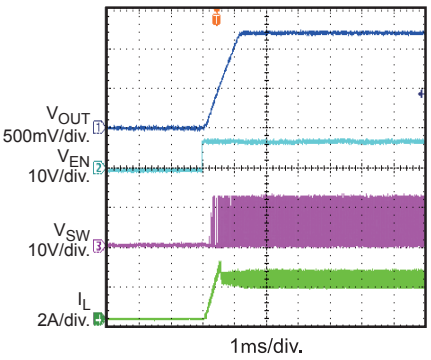
Shut Down Through VIN
I_{OUT} =2A



Start Up Through EN
I_{OUT} =0A



Start Up Through EN
I_{OUT} = 2A

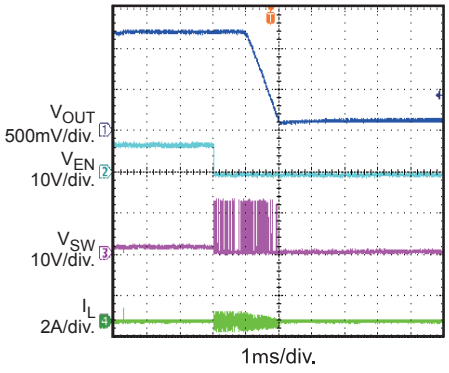


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=1.2V, L=2.2µH, T_A=+25°C, unless otherwise noted.

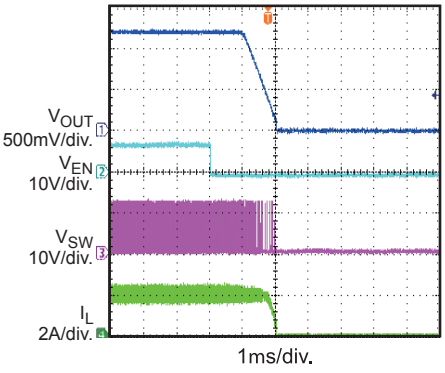
Shut Down Through EN

I_{OUT} = 0A



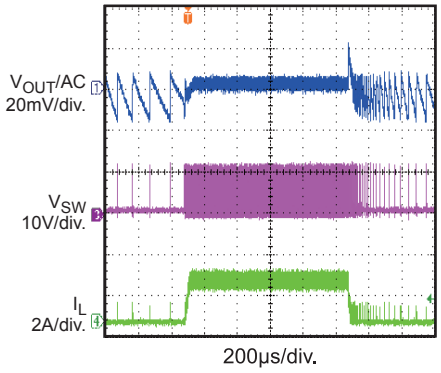
Shut Down Through EN

I_{OUT} = 2A



Transient Response

I_{OUT} = 0A~2A@2.5A/µs
f_{SW} = 500kHz, C_{OUT} = 2*22µH



BLOCK DIAGRAM

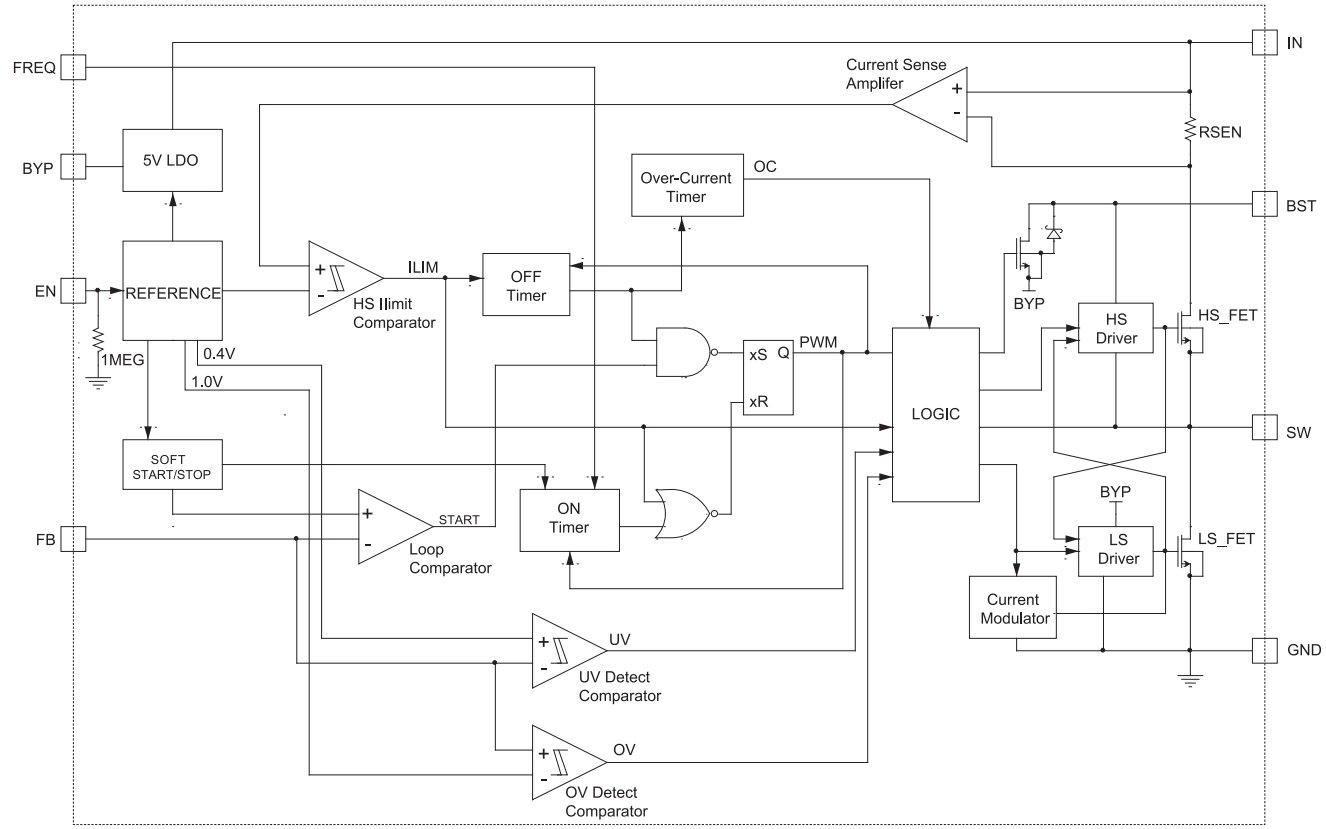


Figure 1—Function Block Diagram

OPERATION

PWM Operation

The MP1492 is a fully integrated synchronous rectified step-down switch converter. Adaptive constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (FB) is below the reference voltage (REF) which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$T_{ON}(ns) = \frac{9.3 \times R_7(k\Omega)}{V_{IN}(V) - 0.4} + 40ns \quad (1)$$

After the ON period elapses, the HS-FET is turned off. It is turned ON again when FB drops below REF. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on.

When the output current is high, the HS-FET and LS-FET repeat on/off as described above. In this operation, the inductor current will never go to zero. It's called continuous-conduction-mode (CCM) operation. In CCM operation, the switching frequency (Fs) is fairly constant.

Light-Load Operation

When the load current decreases, MP1492 reduces the switching frequency automatically to maintain high efficiency. As the output current reduces from heavy-load condition, the inductor current decreases as well, and eventually comes close to zero current. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero level. The current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, efficiency at light-load condition is optimized.

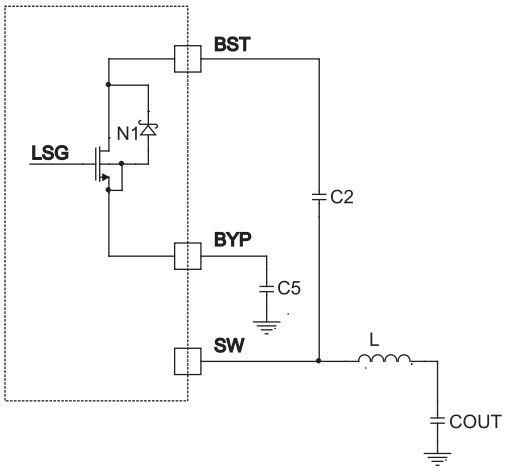


Figure 2

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is charged from VCC through N1 (Figure 3). N1 turns on when LS switches turns on and turns off when LS switch turns off.

Switching Frequency

Adaptive constant-on-time (COT) control is used in MP1492 and there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R_7. The duty ratio is kept as V_{OUT}/V_{IN}. Hence the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_S(kHz) = \frac{10^6}{\frac{9.3 \times R_7(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (2)$$

Where TDELAY is the comparator delay, it's about 40ns.

MP1492 is optimized to operate at high switching frequency but with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Figure 3 and Figure 4 show jitter occurring in both PWM mode and skip mode. When there is noise in the V_{FB} downward slope, the ON time of

HS-FET deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't directly affect the noise immunity directly.

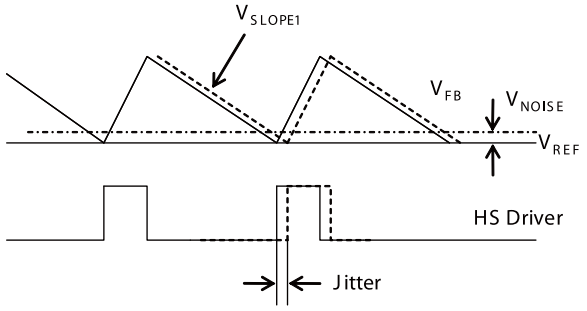


Figure 3—Jitter in PWM Mode

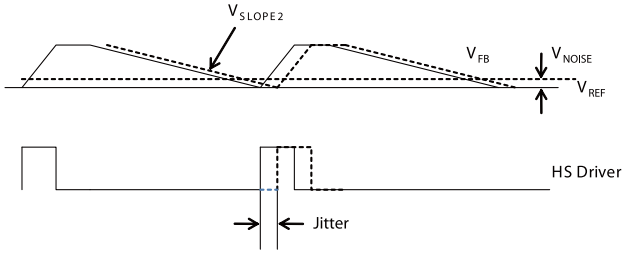


Figure 4—Jitter in Skip Mode

Ramp with Large ESR Cap

In the case of POSCAP or other types of capacitor with larger ESR is applied as output capacitor. The ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 5 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR caps.

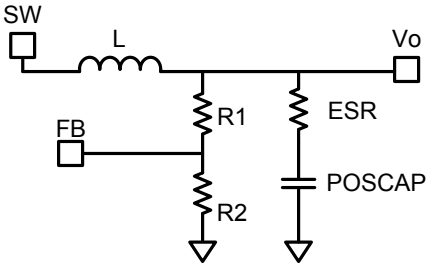


Figure 5—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability when no external ramp is used, usually the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (3)$$

T_{SW} is the switching period.

Ramp with small ESR Cap

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.

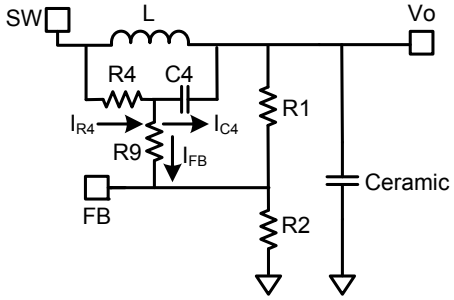


Figure 6—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 6. The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} + R_9 \right) \quad (4)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

And the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN} - V_O}{R_4 \times C_4} \times T_{ON} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (6)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (7)$$

As can be seen from equation 7, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 4, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 8.

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} C_{OUT}}{2 \times L \times C_{OUT}} V_{OUT} + \frac{Io \times 10^{-3}}{T_{SW} - T_{on}} \quad (8)$$

Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is almost the same whether the external ramp is used or not. Figure 7 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

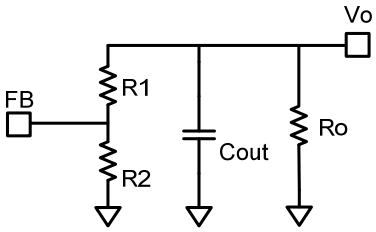


Figure 7—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1 + R_2) // Ro) \times C_{OUT}} \quad (9)$$

Where Ro is the equivalent load resistor.
As described in Figure 4, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during ultra light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the ultra light load efficiency.

Soft Start/Stop

MP1492 employs soft start/stop (SS) mechanism to ensure smooth output during power up and power shut-down. When the EN pin becomes high, an internal SS voltage ramps up slowly. The SS voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once SS voltage reaches the same level of the REF voltage, it keeps ramping up, while REF takes over the PWM comparator. At this point, the soft start finishes, it enters steady state operation. The SS time is about 1ms.

When the EN pin becomes low, the internal SS voltage is discharged through an internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator. The output voltage will decrease smoothly with SS voltage until zero level.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP1492 has cycle-by-cycle over-current limiting control. The inductor current is monitored during the ON state. And it has two optional OCP/SCP protection modes: latch-off mode and hiccup mode.

For MP1492DS, once it detects that the inductor current is higher than the current limit, the HS-FET is turned off. At the same time, the OCP timer is started. The OCP timer is set as 50μs. If in the following 50μs, the current limit is hit for every cycle, then it'll trigger OCP. The converter needs power cycle to restart after it triggers OCP.

When the current limit is hit and the FB voltage is lower than 50% of the REF voltage, MP1492DS considers this as a dead short on the output. It'll trigger OCP immediately. This is short-circuit protection (SCP).

For MP1492DS-A, enters hiccup mode that periodically restarts the part when the inductor current peak value exceeds the current limit and V_{FB} drops below the under-ltage (UV) threshold. Typically, the UV threshold is 50% below the REF voltage, In OCP/SCP, MP1492DS-A will disable the output voltage power, discharge internal soft-start cap, and then automatically try to soft –start again. If the over-current circuit condition still holds after soft-start ends, it repeats this operation cycle until the over-current circuit condition disappears, and output rises back to regulation level.

Over/Under-voltage Protection (OVP/UVP)

MP1492 monitors the output voltage through a resistor divided feedback (FB) voltage to detect

over and under voltage on the output. When the FB voltage is higher than 125% of the REF voltage, it'll trigger OVP. Once it triggers OVP, the LS-FET is always on, while the HS-FET is off. It needs power cycle to power up again. When the FB voltage is below 50% of the REF voltage (0.805V), UVP will be triggered. Usually UVP comes with current limit is hit, hence it results in SCP.

UVLO protection

MP1492 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP1492 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

Thermal shutdown is employed in MP1492. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops around 125ºC, it initiates a SS.

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APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As figure 8 shows.

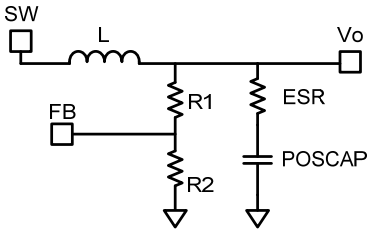


Figure 8—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low,etc.,1.05V, and a smaller R2 when Vo is high. Then R1 is determined as follow with the output ripple considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} R_2 \quad (10)$$

ΔV_{OUT} is the output ripple determined by equation 19.

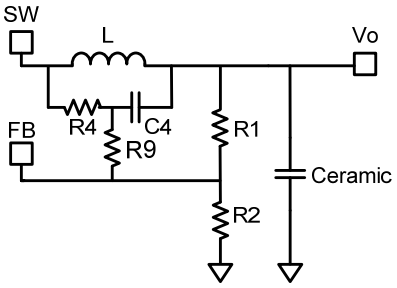


Figure 9—Simplified Circuit of Ceramic Capacitor

Setting the Output Voltage-Small ESR Caps

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp voltage V_{RAMP} besides R divider. The V_{RAMP} can be calculated as shown in equation 6, R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc.,1.05V, and a smaller R2 when Vo is high. And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT} - V_{FB(AVG)})} - \frac{R_2}{R_4 + R_9}} \quad (11)$$

The $V_{FB(AVG)}$ is the average value on the FB, $V_{FB(AVG)}$ varies with the Vin, Vo, and load condition, etc., its value on the skip mode would be lower than that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$,if one wants to gets a better load or line regulation, a lower Vramp is suggested once it meets equation 8.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from equation 12.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (12)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 13 for a better noise immunity. It should also set to be 5 timers smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 \le \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (13)$$

Using equation 11 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 11, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 10 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 14 for PWM mode operation.

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2} V_{RAMP})}{V_{REF} + \frac{1}{2} V_{RAMP}} R_2 \quad (14)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and

should also not larger than 0.47μF considering start up performance. In case one wants to use a larger Cdc for a better FB noise immunity, combined with reducing R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

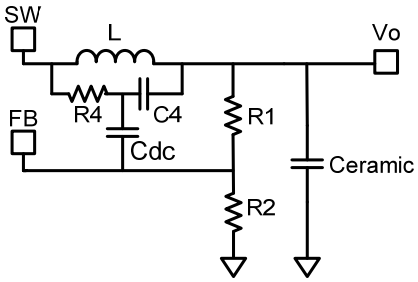


Figure10—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitor as close as possible to the VIN pin.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (15)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (16)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose the input capacitor that meets the specification.The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_S \times C_{IN}} \quad (18)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (19)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_S^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 4, 7 and 8.

In the case of POSCAP or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. So the external ramp is not recommended. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (21)$$

Maximum output capacitor limitation should be also considered in design application. MP1492 has an around 1ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (22)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule of thumb for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (24)$$

Application Recommendation

As Figure 8 shows, when output cap is electrolytic POSCAP, etc with large ESR, no external ramp is needed. Recommended parameters are listed below in Table 1 to Table 3

Table 1—300kHz Recommended Parameters without External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	3.3	12.1	26.1	402
2.5	3.3	30	14.3	820
3.3	3.3	40.2	13.3	1000

Table 2—500kHz Recommended Parameters without External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	3.3	12.1	26.1	240
2.5	3.3	30	14.3	510
3.3	3.3	40.2	13.3	649

Table 3—700kHz Recommended Parameters without External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.2	2.2	12.1	26.1	174
2.5	2.2	30	14.3	348
3.3	2.2	40.2	13.3	475

When output cap is ceramic caps with lower ESR, external ramp is needed as shown in Fig.9. Recommended parameters are as listed in Table 4 to Table 6 with R9=0Ω.

Table 4—300kHz Recommended Parameters with External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	3.3	12.1	26.1	330	220	402
2.5	3.3	30	14.3	698	220	820
3.3	3.3	40.2	12.7	698	220	1000

Table 5—500kHz Recommended Parameters with External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	3.3	12.1	26.1	402	220	240
2.5	3.3	30	14.3	549	220	510
3.3	3.3	40.2	12.7	698	220	649

Table 6—700kHz Recommended Parameters with External Ramp Compensation
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.2	2.2	12.1	26.1	330	220	174
2.5	2.2	30	14.3	549	220	348
3.3	2.2	40.2	12.7	698	220	475

According to equation (22) and some design abundance are reserved, recommended maximum output capacitor value is shown in Table 7.

Table 7—Recommended Maximum Output Capacitor Value (F_S=500 kHz)
Recommended Conditions: V_{IN}=12V, I_{OUT}=2A

V_{OUT} (V)	1.2	1.8	2.5	3.3	5
C_{O_MAX} (μF)	680	570	390	330	220

The detailed application schematic is shown in Figure 11, 12 and Figure 13. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

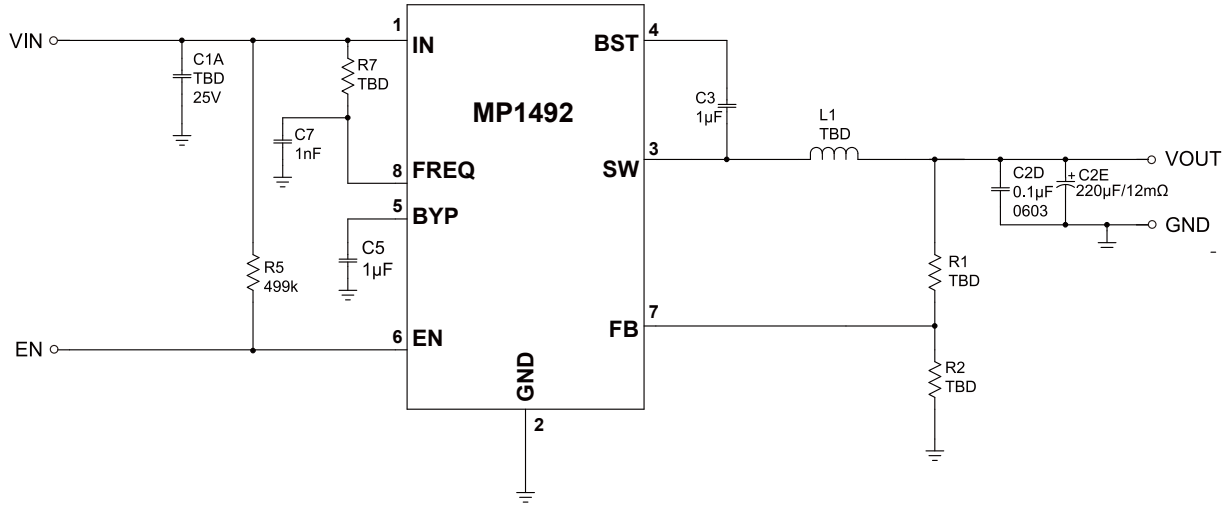


Figure 11—Typical Application Schematic with No External Ramp

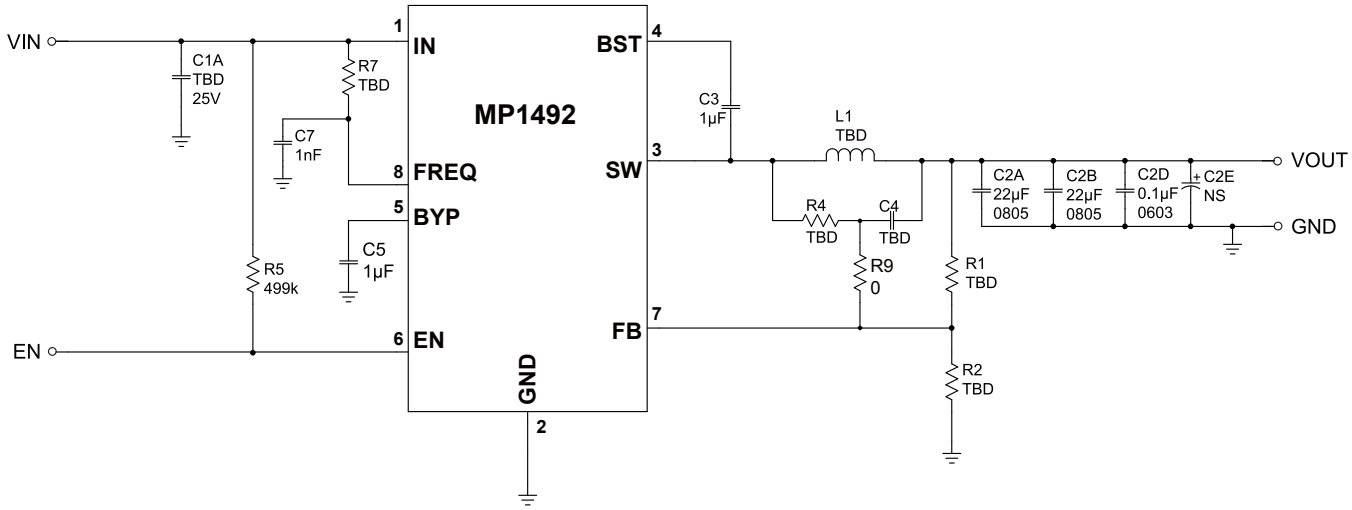


Figure 12—Typical Application Schematic with Low ESR Ceramic Capacitor

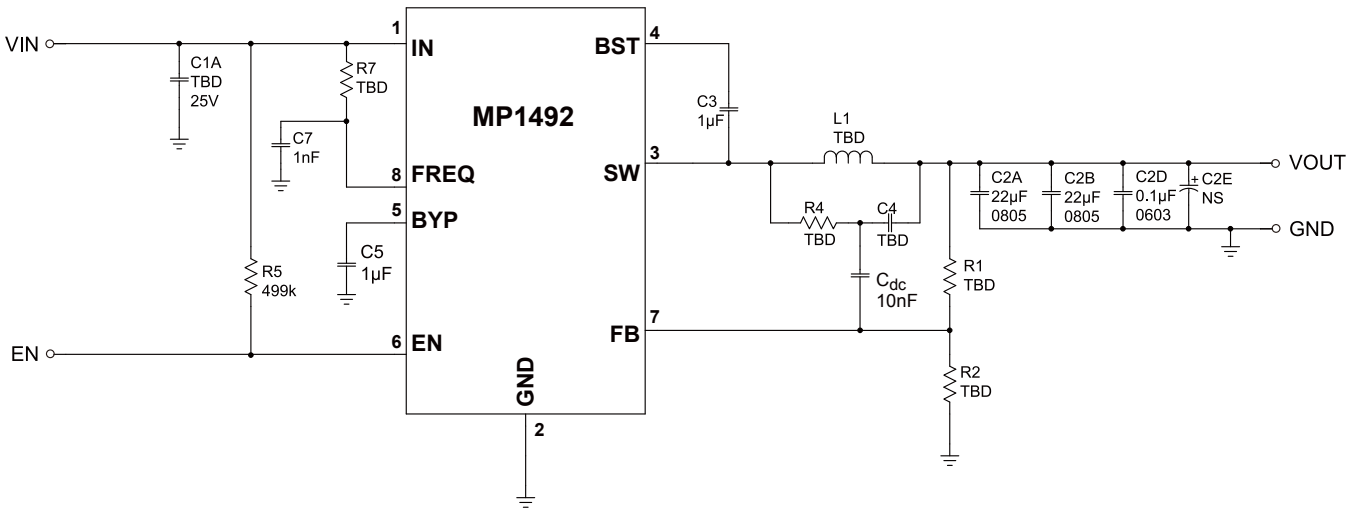


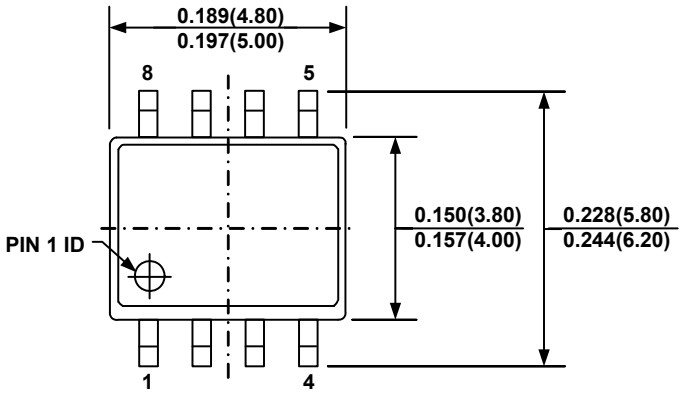
Figure 13—Typical Application Schematic with Low ESR Ceramic Capacitor and DC Blocking Capacitor.

Layout Recommendation

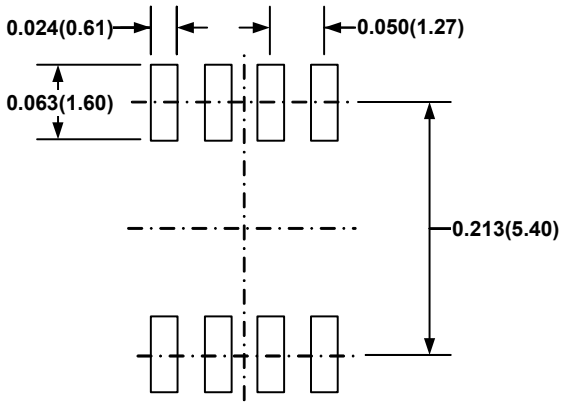
1) Put the input capacitors as close as possible to the IN pin.
2) Put the decoupling capacitor as close as possible to the V_{CC} pin.
3) Put the inductor as close as possible to SW pin. Make the SW pad as large as possible to minimize the switching noise interference.
4) The FB pin is directly connected to the PWM comparator. It should be routed away from the noisy SW node.

PACKAGE INFORMATION

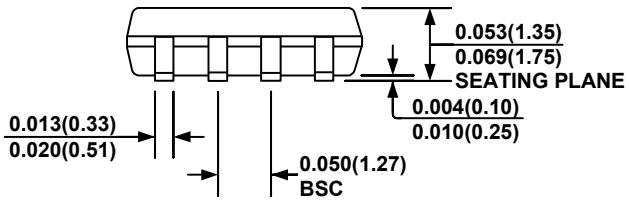
SOIC8



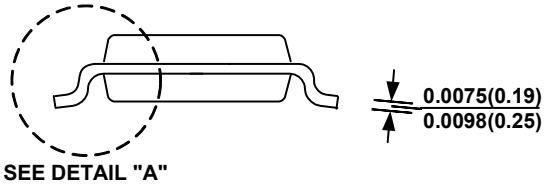
TOP VIEW



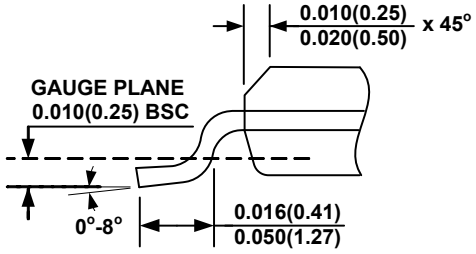
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.