RAiO

RA8808

128x64 Driver

for Dot Matrix LCD

Specification

Version 1.0

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RAiO Technology Inc.

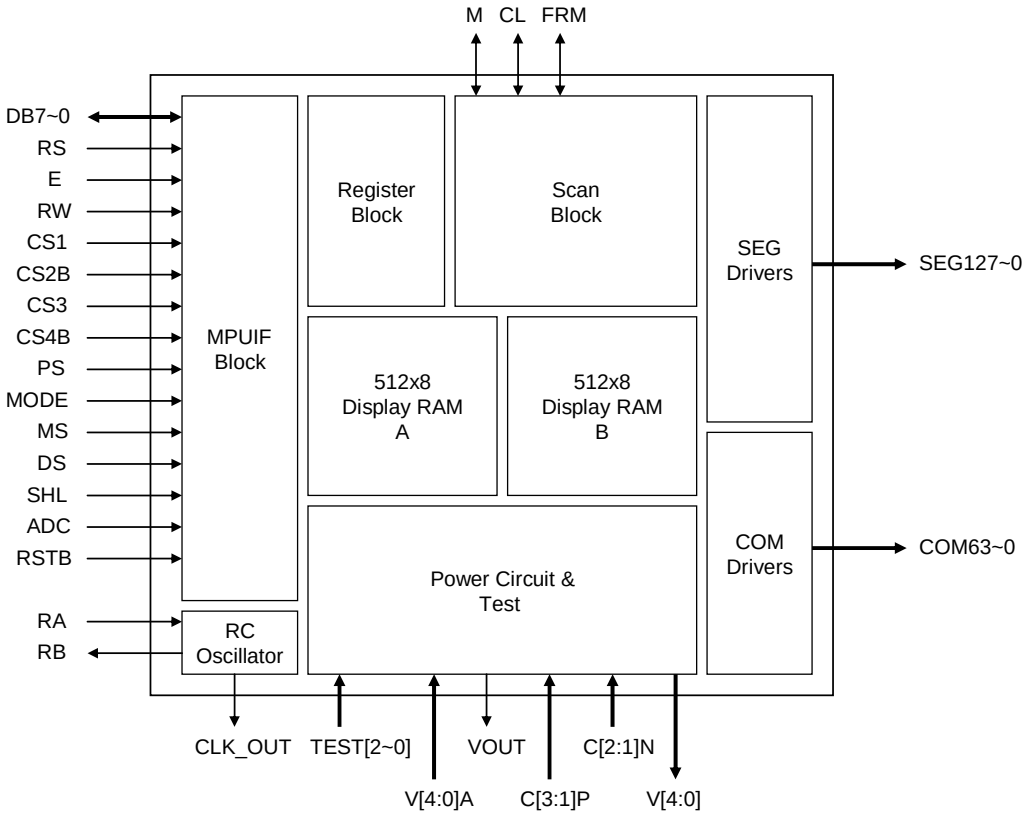
1. General Description

The RA8808 is a LCD driver LSI with 128(Segment) x 64(Common) driver output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM,128-bit segment drivers, 64-bit common drivers and decoder logic. It has the internal display RAM for storing the display data transferred from an 8-bit 8080/6800 micro controller or 3-wire-SPI/IIC controller and generates the dot matrix liquid crystal driving signals corresponding to stored data.

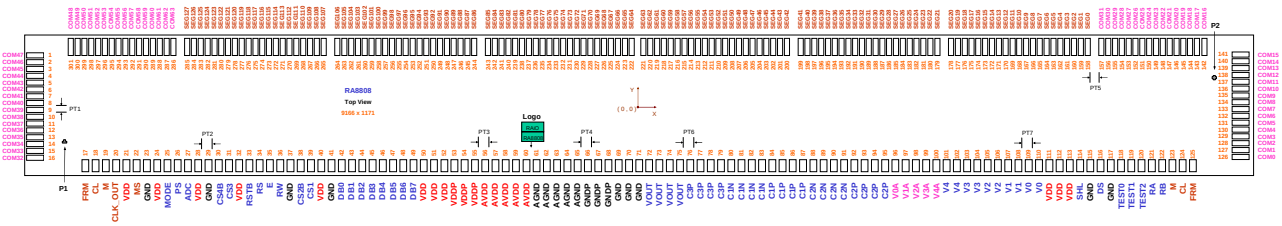
2. Features

- Dot matrix LCD segment driver with 128 channel output, and common driver with 64 channel output.
- Internal timing generator circuit for dynamic display.
- Selection of master/slave mode for combine two RA8808 controller to support 256x64 dot Matrix.
- Applicable LCD common duty: 1/48, 1/64.
- Support 6800/8080 8-bit parallel MPU interface.
- Support 3-wires SPI and IIC serial MPU interface.
- Two 512 bytes (4096-bits) Display RAM
- LCD driving voltage: 8V ~17V
- Built-in 2X~4X Voltage Booster and Voltage Follower
- Power supply voltage: +2.7V ~ 5.5V
- High voltage CMOS process
- Bare gold bump chip available

3. Block Diagram



4. Pad Diagram



5. Pin Description

5-1 MPU Interface

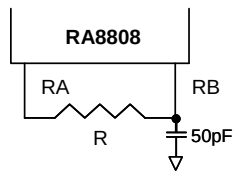
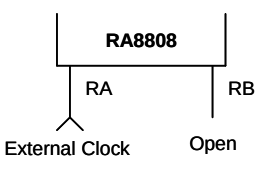
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>DB0~DB7</td><td>I/O</td><td>
In Parallel Mode :
Data Bus
These are data bus for data transfer between MPU(6800/8080) and RA8808.
In Serial Mode :
<table>
<tr><th>Pin</th><th>Description</th></tr>
<tr><td>DB7</td><td rowspan="2">These pins are not used and must be connected to low.</td></tr>
<tr><td>DB6</td></tr>
<tr><td>DB5</td><td rowspan="3">In IIC Interface :
These pins are used as the IIC device address input. (SA[2:0])
In SPI Interface :
These pins are not used and must be connected to high or low.</td></tr>
<tr><td>DB4</td></tr>
<tr><td>DB3</td></tr>
<tr><td>DB2</td><td>In IIC Interface :
This pin is not used and must be connected to low.
In SPI Interface :
This pin is used as Chip selection, active low. (ZCS)</td></tr>
<tr><td>DB1</td><td>In IIC Interface :
This pin is used as Bi-direction serial Data.(SDA)
In SPI Interface :
This pin is used as Bi-direction serial Data.(SDA)</td></tr>
<tr><td>DB0</td><td>In IIC Interface :
This pin is used as serial clock.(SCL)
In SPI Interface :
This pin is used as serial clock.(SCK)</td></tr>
</table>
</td></tr>
<tr><td>E</td><td>I</td><td>
In Parallel Mode :
Enable or Read Control
When use 6800 series interface, this pin is used as Enable, active high.
When use 8080 series interface, this pin is used as data read, active low.
In Serial Mode :
This pin is not used and must be connected to low.
</td></tr>
</table>

<table>
<tr><td>RW</td><td>I</td><td>In Parallel Mode :
Read-Write Control or Write Control
When use 6800 series interface, this pin is used as data read/write control. Active high for read and active low for write.
When use 8080 series interface, this pin is used as data write, active low.
In Serial Mode :
This pin is not used and must be connected to low.</td></tr>
<tr><td>RS</td><td>I</td><td>In Parallel Mode :
Data or Instruction
RS = H ➔ DB0~DB7 : Display RAM data
RS = L ➔ DB0~DB7 : Instruction data
In Serial Mode :
This pin is not used and must be connected to low.</td></tr>
<tr><td>CS1
CS2B</td><td>I</td><td>In Parallel Mode :
Chip selection for left side (Note 1)
In order to interface left side data for input or output, the terminals have to be CS1 = H, CS2B = L.
In Serial Mode :
These pins are not used and must be connected to high or low.</td></tr>
<tr><td>CS3
CS4B</td><td>I</td><td>In Parallel Mode :
Chip selection for right side (Note 1)
In order to interface right side data for input or output, the terminals have to be
CS3 = H, CS4B = L.
In Serial Mode :
These pins are not used and must be connected to to high or low.</td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset Signal
When RSTB = L,
_ON/OFF register becomes set by 0. (display off)
_Display start line register becomes set by 0.(Z-address 0 set, display from line 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial MPU Interface Selection
<table>
<tr><th>PS</th><th>Parallel/Serial</th></tr>
<tr><td>H</td><td>Parallel</td></tr>
<tr><td>L</td><td>Serial</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>I</td><td>MPU Interface Selection(Combine with PS)
<table>
<tr><th>PS</th><th>MODE</th><th>MPU Interface</th></tr>
<tr><td>H</td><td>H</td><td>6800 series</td></tr>
<tr><td>H</td><td>L</td><td>8080 series</td></tr>
<tr><td>L</td><td>H</td><td>3-wire SPI</td></tr>
<tr><td>L</td><td>L</td><td>IIC</td></tr>
</table></td></tr>
</table>

5-2 LCD Panel Interface

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0~
SEG127</td><td>O</td><td>LCD Segment Driver Output
Display RAM data 1 : On, Display RAM data 0 : Off
Relation of display RAM & M :
<table>
<tr><th>M</th><th>Data</th><th>Output Level</th></tr>
<tr><td>L</td><td>L</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>V3</td></tr>
<tr><td>H</td><td>H</td><td>GND</td></tr>
</table></td></tr>
<tr><td>COM0~
COM63</td><td>O</td><td>Common Signal Output for LCD Driving
Relation of common signal & M :
<table>
<tr><th>M</th><th>Common Signal</th><th>Output Level</th></tr>
<tr><td>L</td><td>L</td><td>V1</td></tr>
<tr><td>L</td><td>H</td><td>GND</td></tr>
<tr><td>H</td><td>L</td><td>V4</td></tr>
<tr><td>H</td><td>H</td><td>V0</td></tr>
</table></td></tr>
<tr><td>M</td><td>I/O</td><td>Alternating Signal Input for LCD Driving.
The input/output selection is determined by MS.</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display Synchronous Signal
Display data is latched at rising time of the CL signal and increments the Z-address counter at CL falling time. The input/output selection is determined by MS.</td></tr>
<tr><td>FRM</td><td>I/O</td><td>Synchronous Control Signal
Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high. The input/output selection is determined by MS.</td></tr>
<tr><td>MS</td><td>I</td><td>Master/Slave Mode Selection
<table>
<tr><th>MS</th><th>Master/Slave Mode</th></tr>
<tr><td>H</td><td>Master</td></tr>
<tr><td>L</td><td>Slave</td></tr>
</table>
When in Master mode, M, CL, FRM are output pins.
When in Slave mode, M, CL, FRM are input pins.</td></tr>
</table>

5-3 Clock

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RA</td><td>I</td><td>In internal clock mode, this pin connects to external resistor for RC circuit.
In external clock mode, this pin is an input of external clock.
<table>
<tr><th>Internal Clock Mode</th><th>External Clock Mode</th></tr>
<tr><td> 
</td><td> 
</td></tr>
</table></td></tr>
<tr><td>RB</td><td>O</td><td>In internal clock mode, this pin connects to external resistor for RC circuit.
In external clock mode, this pin must keep floating.</td></tr>
<tr><td>CLK_OUT</td><td>O</td><td>Internal system clock output for cascade application or others for user.</td></tr>
</table>

5-4 Power

Pin Name	I/O	Description
VOUT	O	**Regulator Voltage Output**
VDD VDDP	P	**Digital Power**
GND GNDP	P	**Digital Ground**
AVDD	P	**Analog Power**
AGND	P	**Analog Ground**
C1N C1P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C2N C2P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C3P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
V0A~V4A	I	**Voltage Input**
V0~V4	O	**Voltage Source of LCD Driver** The relationship of the power is V0 > V1 > V2 > V3 > V4 > GND.

5-5 MISC

Pin Name	I/O	Description
ADC	I	**Selection of Segment Data Direction** ADC: H → SEG0 → SEG1 … →SEG127; L → SEG127 → SEG126 … → SEG0
SHL	I	**Selection of Common Data Shift Direction** SHL: H → COM0 → COM1 … →COM63; L → COM63 → COM62 … → COM0
DS	I	**Selection of Display Duty** DS: H → 1/64; L → 1/48
TEST0 TEST1 TEST2	I	These pins must contact to GND in normal mode.

6. LCD Panel Interface Application Circuit