2.8W Mono Class D Audio Power Amplifier with AGC

Features

- **Operating Voltage: 2.4V-5.5V**
- **High Efficiency up to 90%**
- **Supply Current**
  - **I_{DD}=3mA at V_{DD}=5V**
  - **I_{DD}=2.5mA at V_{DD}=3.6V**
- **Low Shutdown Current**
  - **I_{DD}=1μA at V_{DD}=5V**
- **Output Power**
  at 1% THD+N
  - **1.3W, at V_{DD}=5V, R_L=8Ω**
  - **0.6W, at V_{DD}=3.6V, R_L=8Ω**
  - **2.0W, at V_{DD}=5V, R_L=4Ω**
  - **1.0W, at V_{DD}=3.6V, R_L=4Ω**

  at 10% THD+N
  - **1.6W, at V_{DD}=5V, R_L=8Ω**
  - **0.8W, at V_{DD}=3.6V, R_L=8Ω**
  - **2.8W, at V_{DD}=5V, R_L=4Ω (WLCSP-9)**
  - **2.4W, at V_{DD}=5V, R_L=4Ω**
  - **1.2W, at V_{DD}=3.6V, R_L=4Ω**
- **APA2011 Dynamic Range Control (DRC) Provide Maximum 15dB Control (2:1 Compression Ratio)**
- **APA2011A Non-Clip Function can Provide Maximum 15dB Control (Gain Decreasing)**
- **Less External Components Required**
- **Fast Start-up Time (4ms)**
- **High PSRR: 70dB at 217Hz**
- **Thermal and Over-Current Protections**
- **Space Saving Packages**
  WLCSP1.5x1.5-9 Bump, TDFN3x3-8
- **Lead Free and Green Devices Available**
  (RoHS Compliant)

Applications

- **Mobil Phones**
- **Handset**
- **PDAs**
- **Portable Multimedia Device**

General Description

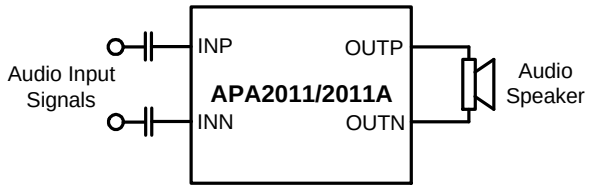
The APA2011/2011A is a mono, filter-free Class-D audio amplifier available in WLCSP1.5x1.5-9 or TDFN3x3-8 package.

The default gains without the external input resistor is 27dB. Besides, the gain can be low down by external input resistance. APA2011 provides an Dynamic-Range-Control (DRC) function, and this function can low down the dynamic range for large input signal. APA2011 can provide maximun 15dB gain control. APA2011A can provide maximum 15dB gain decrease for non-clipping function, and this function can avoid output signal clipping. High PSRR and differential architecture provide increased immunity to noise and RF rectification. In addition to these features, a fast start-up time and small package size make the APA2011/2011A an ideal choice for portable devices.

The APA2011/2011A is capable of driving 1.6W at 5V or 0.8W at 3.6V into 8Ω. It is also capable of driving 4Ω. The APA2011/2011A is designed with a Class-D architecture and operating with highly efficiency compared with Class-AB amplifier. It's suitable for power sensitive application, such as battery-powered devices. The filter-free architecture eliminates the output filter, reduces the external component count, board area, and system costs, and simplifies the design.

Moreover, the APA2011/2011A provides thermal and short circuit protection.

Simplified Application Circuit

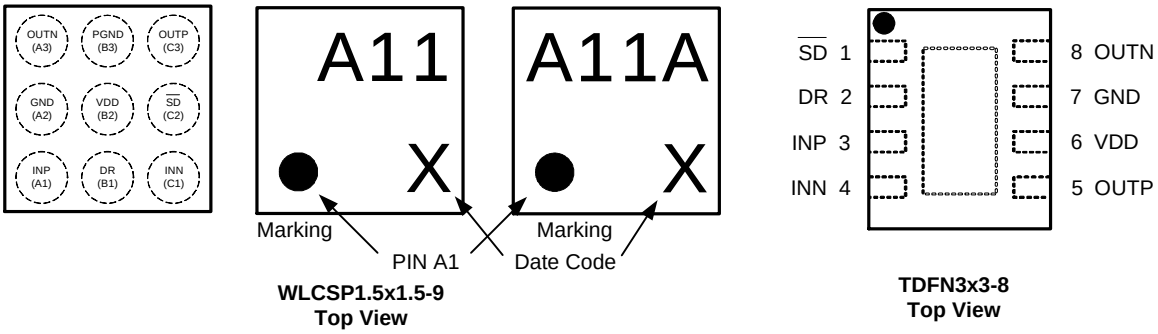


Ordering and Marking Information

APA2011/2011A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code HA : WLCSP1.5x1.5-9 QB : TDFN3x3-8 Operating Ambient Temperature Range I : - 40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2011 HA : A11 / X	X - Date Code
APA2011A HA : A11A / X	X - Date Code
APA2011 QB : APA / 2011 / • XXXXX	XXXXX - Date Code
APA2011A QB : APA / 2011A / • XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



WLCSP1.5x1.5-9
Top View

TDFN3x3-8
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PGND_GND}	PGND to GND	-0.3 to +0.3	V
V_{DD}	Supply Voltage (VDD to PGND, VDD to GND)	-0.3 to 6	
V_{IN}	Input Voltage (INN, INP to GND)	-0.3 to V_{DD}+0.3	
$V_{\overline{SD}}$, V_{DR}	Input Voltage ($\overline{SD}$, DR to GND)	-0.3 to V_{DD}+0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) WLCSP1.5x1.5-9 TDFN3x3-8	 165 50	°C/W
θ_{JC}	Thermal Resistance -Junction to Case (Note 3) TDFN3x3-8	 10	°C/W

Note 2: Please refer to " Layout Recommendation", the Thermal Pad on the bottom of the IC should soldered directly to the PCB's Thermal Pad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness**.**

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TDFN3x3-8 package.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		2.4	5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$	1	-	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$	-	0.4	
V_{IC}	Common Mode Input Voltage		-	V_{DD}-1	
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	
R_L	Speaker Resistance		2.8	-	Ω

Electrical Characteristics

V_{DD}=5V, GND=0V, A_V=15dB, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2011/2011A			Unit
				Min.	Typ.	Max.	
I_{DD}	Supply Current			-	3	6	mA
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V		-	1	5	μA
I_I	Input Current	$\overline{SD}$		-	0.1	1	
F_{OSC}	Oscillator Frequency			400	500	600	kHz
$t_{wake-up}$	Recovery Time from Shutdown			-	4	8	ms
R_i	Input Resistor	INN, INP		23.75	25	26.25	kΩ
R_{DR}	DR Pin Pull-high Resistor			9.5	10	10.5	
$R_{DS(ON)}$	Static Drain-Source On-State Resistance (PMOSFET+NMOSFET)	V_{DD}=5V, I_L=0.8A	WLCSP1.5x1.5-9	-	780	-	mΩ

Electrical Characteristics (Cont.)

V_{DD}=5V, GND=0V, A_V=15dB, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2011/2011A			Unit
				Min.	Typ.	Max.	
$R_{DS(ON)}$	Static Drain-Source On-State Resistance (PMOSFET+NMOSFET)	V_{DD}=3.6V, I_L=0.6A	WLCSP1.5x1.5-9	-	900	-	mΩ
		V_{DD}=2.4V, I_L=0.4A	WLCSP1.5x1.5-9	-	1000	-	
η	Efficiency	P_O=1.2W, R_L=8Ω+33μH	WLCSP1.5x1.5-9	-	90	-	%
		P_O=2W, R_L=4Ω+33μH	WLCSP1.5x1.5-9	-	82	-	
V_{DD}=5V							
P_O	Output Power	THD+N=1%, f_{in}=1kHz	R_L=3Ω	-	2.45	-	W
			R_L=4Ω, WLCSP1.5x1.5-9	-	2.2	-	
			R_L=4Ω	-	2.0	-	
			R_L=8Ω	1	1.3	-	
		THD+N=10%, f_{in}=1kHz	R_L=3Ω	-	3.0	-	
			R_L=4Ω, WLCSP1.5x1.5-9	-	2.8	-	
			R_L=4Ω	-	2.4	-	
			R_L=8Ω	-	1.6	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω P_O=1.4W	-	0.05	0.1	%
			R_L=8Ω P_O=0.9W	-	0.04	0.1	
			R_L=8Ω P_O=1.5W, V_{DR}=V_{DD}	-	3	5	
V_{OS}	Output Offset Voltage	R_L=8Ω		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter, R_L=8Ω		-	100	200	μVrms
S/N	Signal to Noise Ratio	With A-weighting Filter, P_O=0.9W, R_L=8Ω		82	89	-	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω, f_{in}=217Hz,V_{rr}=0.5V_{pp}		-	-70	-60	
CMRR	Common Mode Rejection Ratio	f_{in}=1kHz, R_L=8Ω, V_{in}=0.1V_{pp}		-	-60	-50	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{pp}		-	-100	-90	
V_{DD}=3.6V							
P_O	Output Power	THD+N=1%, f_{in}=1kHz	R_L=4Ω	-	1.0	-	W
			R_L=8Ω	-	0.6	-	
		THD+N=10%, f_{in}=1kHz	R_L=4Ω	-	1.2	-	
			R_L=8Ω	-	0.8	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω P_O=0.7W	-	0.07	0.15	%
			R_L=8Ω P_O=0.4W	-	0.05	0.1	
V_{OS}	Output Offset Voltage	R_L=8Ω		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter, R_L=8Ω		-	100	200	μVrms

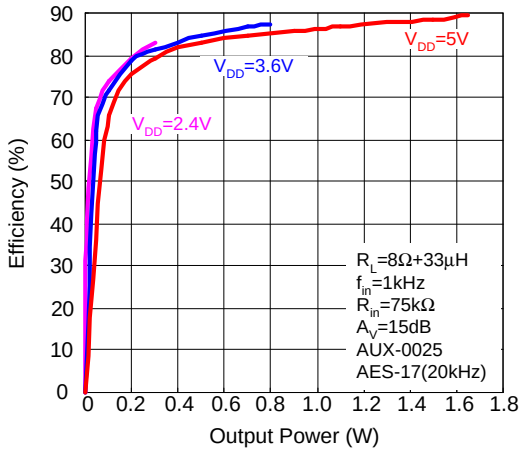
Electrical Characteristics (Cont.)

V_{DD}=5V, GND=0V, A_V=15dB, T_A= 25°C (unless otherwise noted)

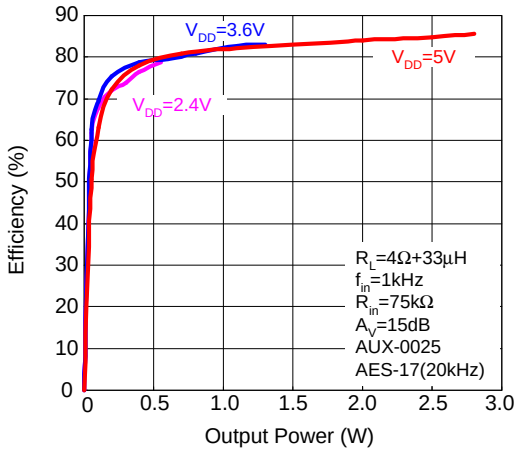
Symbol	Parameter	Test Conditions		APA2011/2011A			Unit
				Min.	Typ.	Max.	
V_{DD}=3.6V (CONT.)							
S/N	Signal to Noise Ratio	With A-weighting Filter, P_O=0.4W, R_L=8Ω		79	85	-	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω, f_{in}=217Hz,V_{rr}=0.2V_{pp}		-	-70	-60	
CMRR	Common Mode Rejection Ratio	f_{in}=1kHz, R_L=8Ω, V_{in}=0.1V_{pp}		-	-60	-50	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{pp}		-	-100	-90	
V_{DD}=2.4V							
P_O	Output Power	THD+N=1%, f_{in}=1kHz	R_L=4Ω	-	0.45	-	W
			R_L=8Ω	-	0.3	-	
		THD+N=10%, f_{in}=1kHz	R_L=4Ω	-	0.55	-	
			R_L=8Ω	-	0.35	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω P_O=0.32W	-	0.2	0.5	%
			R_L=8Ω P_O=0.2W	-	0.1	0.3	
V_{os}	Output Offset Voltage	R_L=8Ω		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter, R_L=8Ω		-	110	220	μVrms
S/N	Signal to Noise Ratio	With A-weighting Filter, P_O=0.2W, R_L=8Ω		75	81	-	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω, f_{in}=217Hz,V_{rr}=0.1V_{pp}		-	-65	-60	
CMRR	Common Mode Rejection Ratio	f_{in}=1kHz, R_L=8Ω, V_{in}=0.1V_{pp}		-	-60	-50	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{pp}		-	-100	-90	

Typical Operating Characteristics

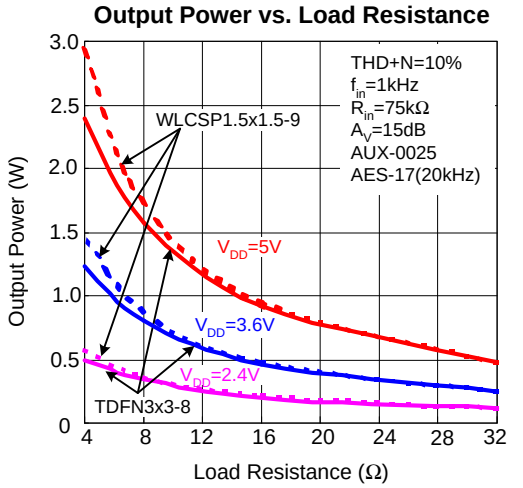
Efficiency vs. Output Power (8W)



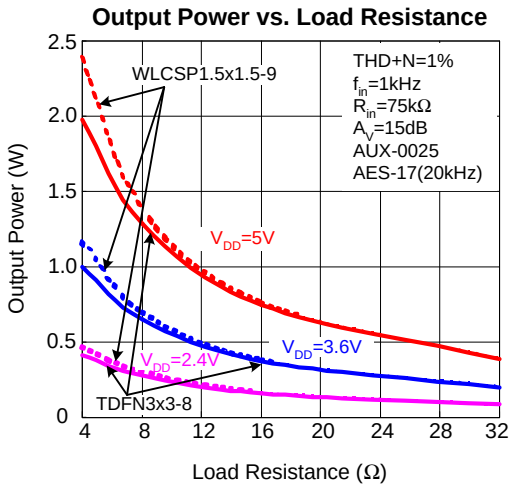
Efficiency vs. Output Power (4W)



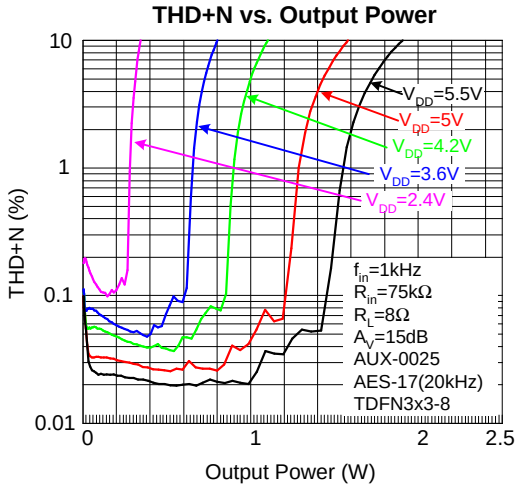
Output Power vs. Load Resistance



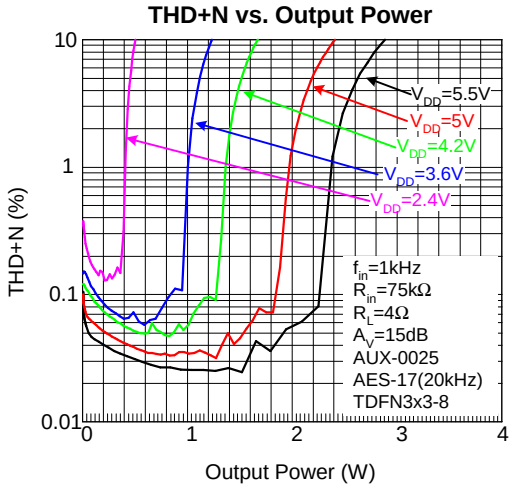
Output Power vs. Load Resistance



THD+N vs. Output Power

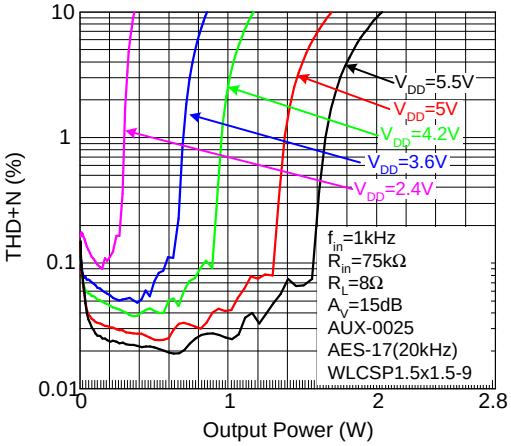


THD+N vs. Output Power

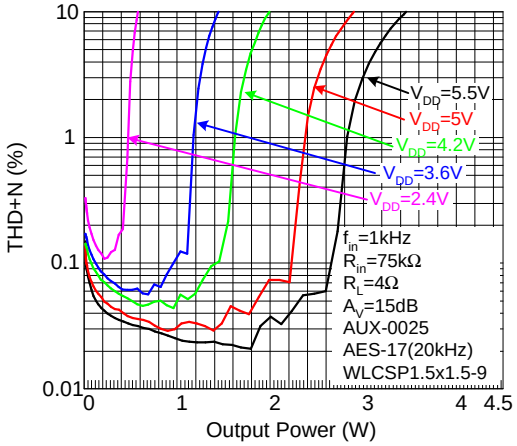


Typical Operating Characteristics (Cont.)

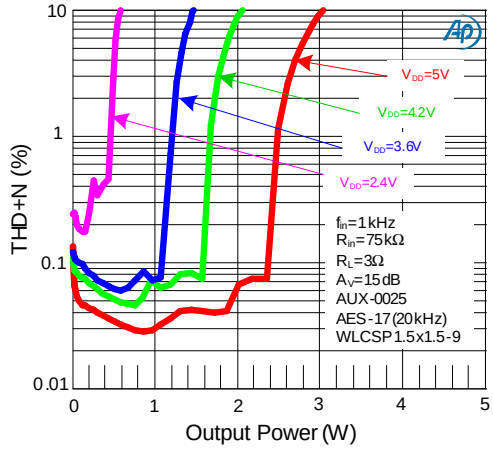
THD+N vs. Output Power



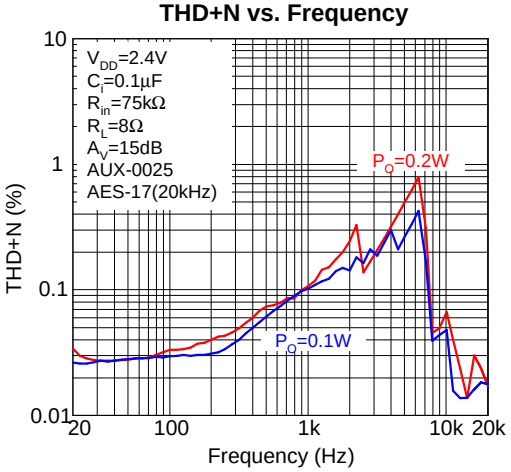
THD+N vs. Output Power



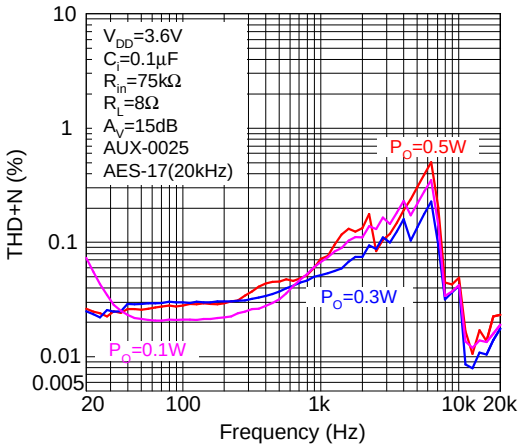
THD+N vs. Output Power



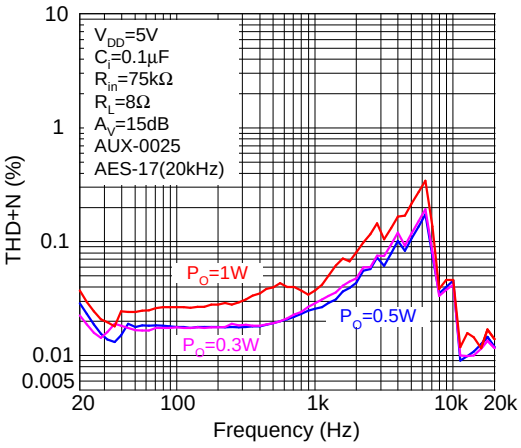
THD+N vs. Frequency



THD+N vs. Frequency

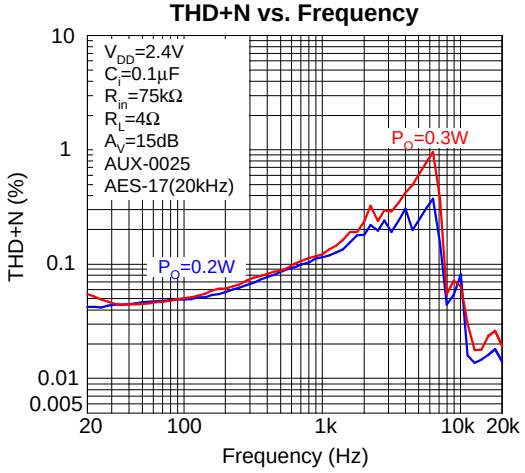


THD+N vs. Frequency

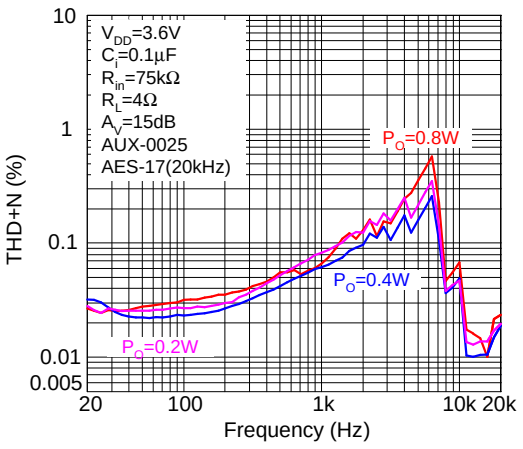


Typical Operating Characteristics (Cont.)

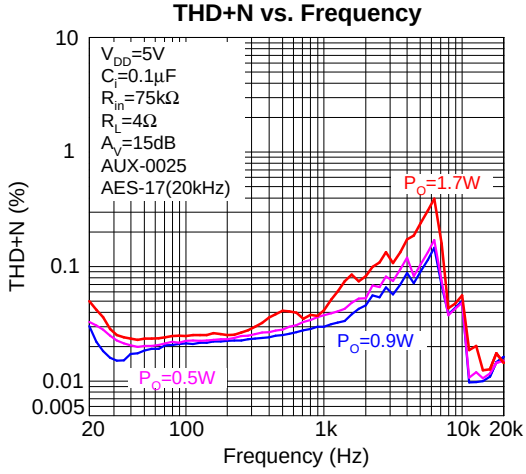
THD+N vs. Frequency



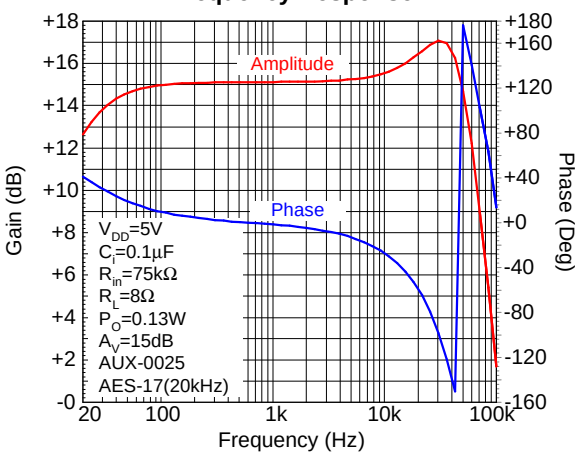
THD+N vs. Frequency



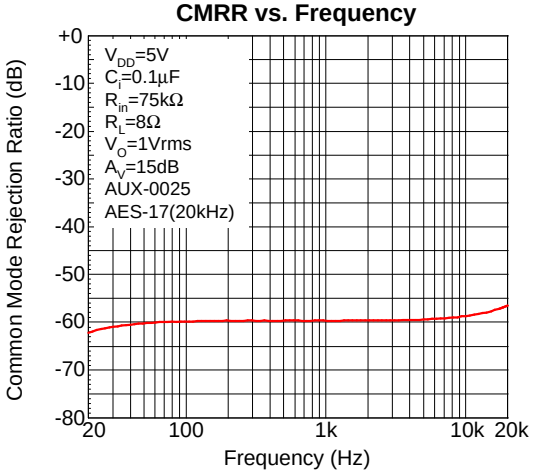
THD+N vs. Frequency



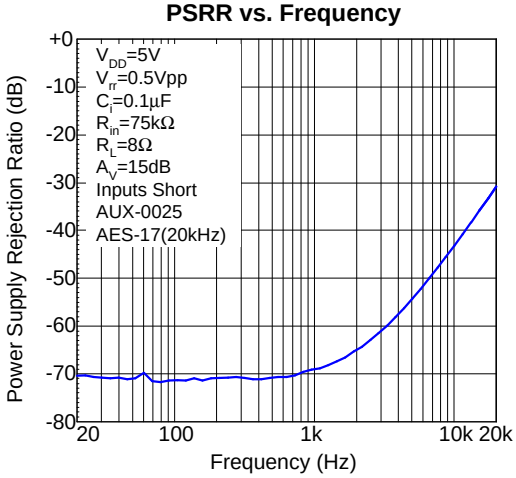
Frequency Response



CMRR vs. Frequency

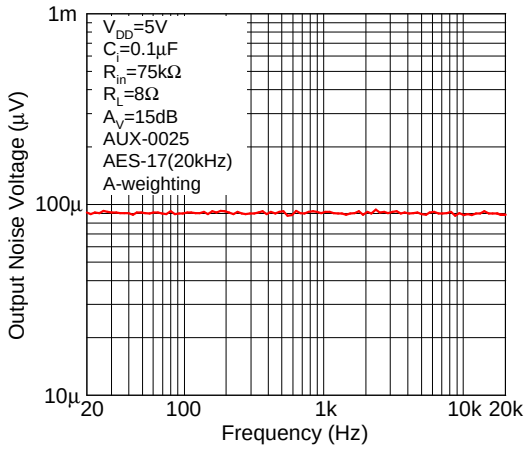


PSRR vs. Frequency

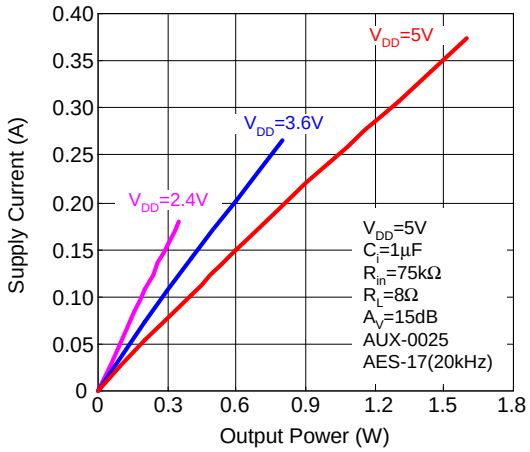


Typical Operating Characteristics (Cont.)

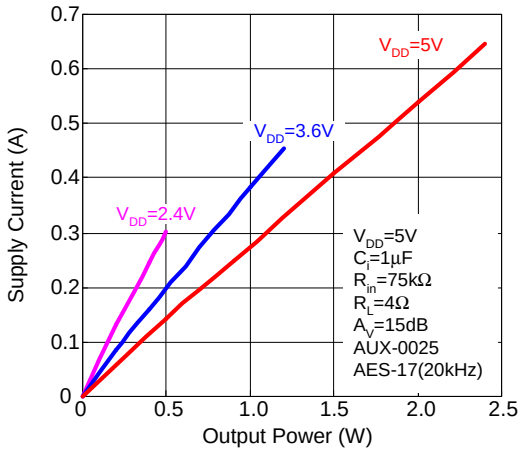
Noise vs. Frequency



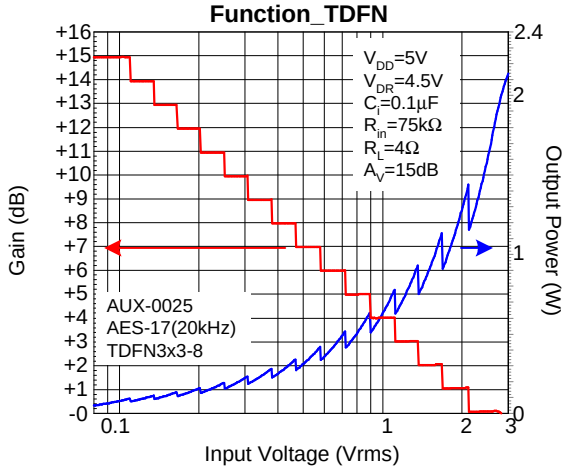
Supply Current vs. Output Power



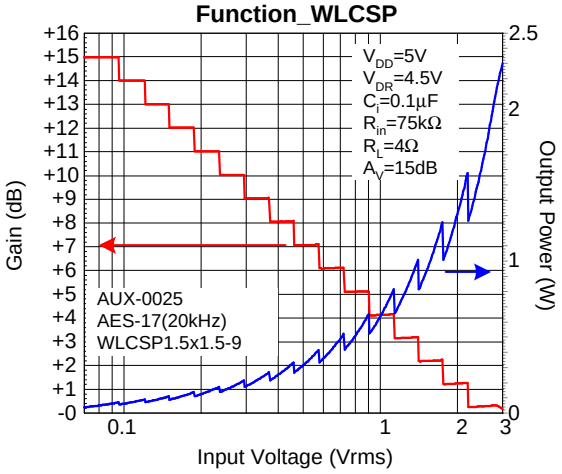
Supply Current vs. Output Power



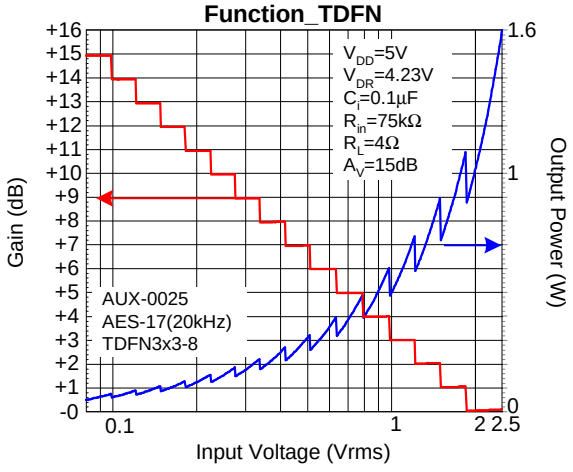
APA2011 Dynamic Range Control Function_TDFN



APA2011 Dynamic Range Control Function_WLCSP

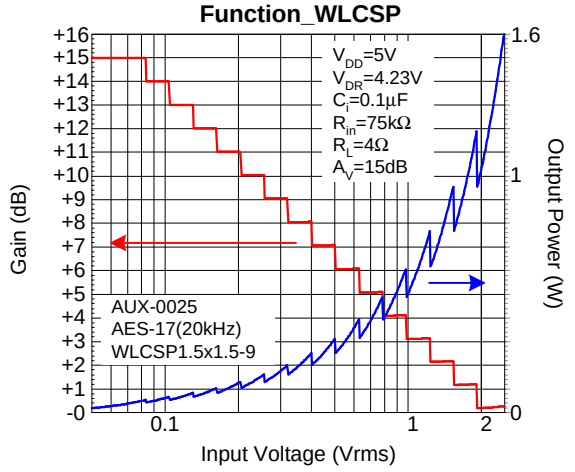


APA2011 Dynamic Range Control Function_TDFN

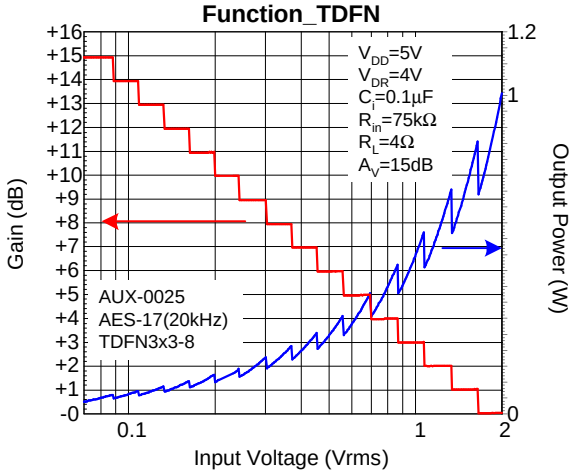


Typical Operating Characteristics (Cont.)

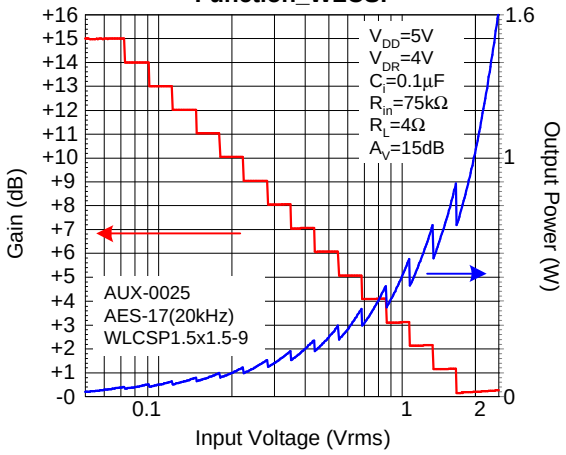
APA2011 Dynamic Range Control Function_WLCSP



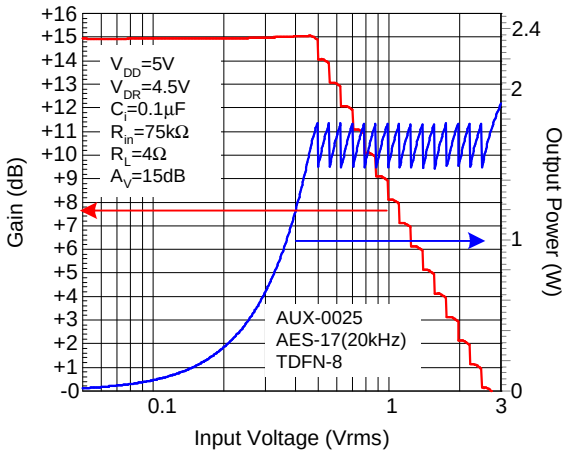
APA2011 Dynamic Range Control Function_TDFN



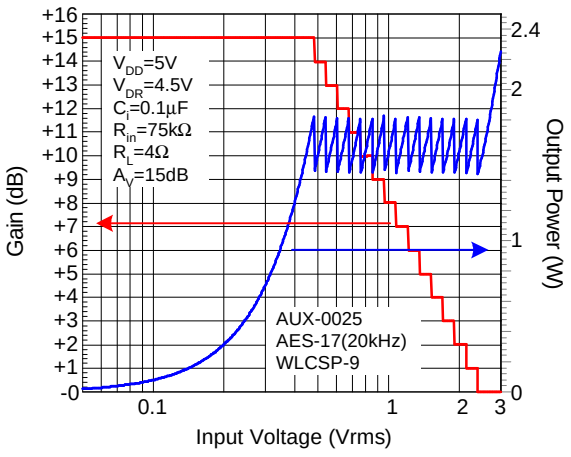
APA2011 Dynamic Range Control Function_WLCSP



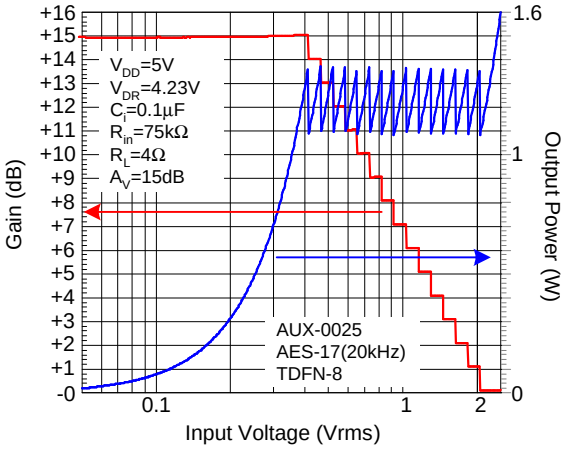
APA2011A Non-Clipping Function_TDFN



APA2011A Non-Clipping Function_WLCSP

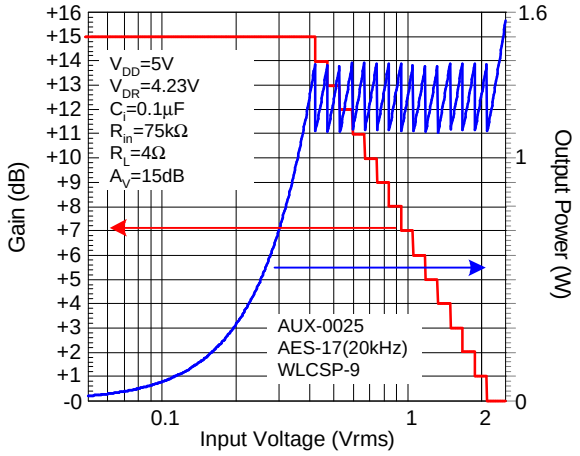


APA2011A Non-Clipping Function_TDFN



Typical Operating Characteristics (Cont.)

APA2011A Non-Clipping Function_WLCSP



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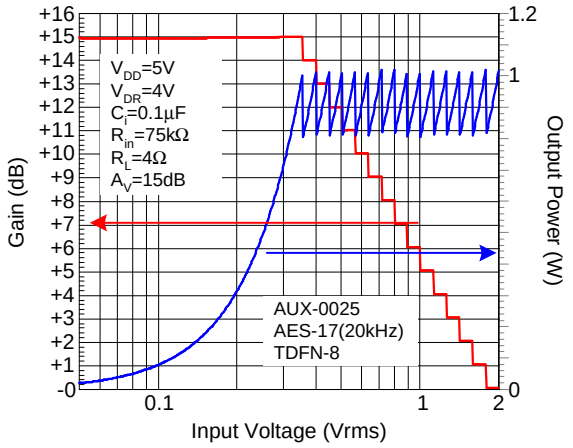
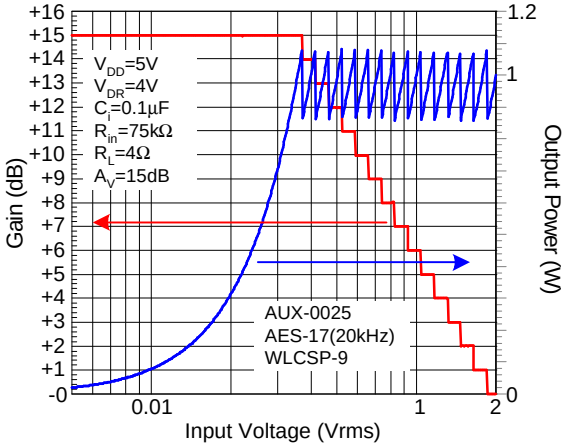
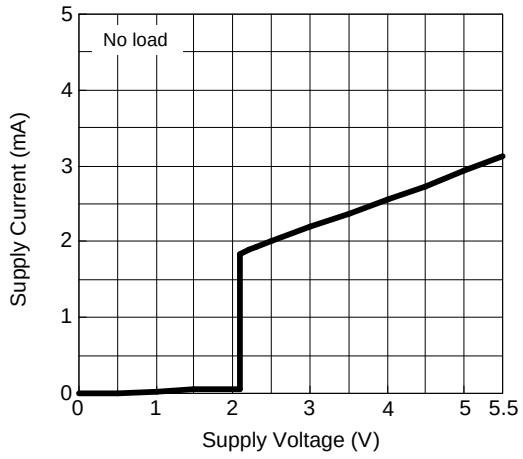


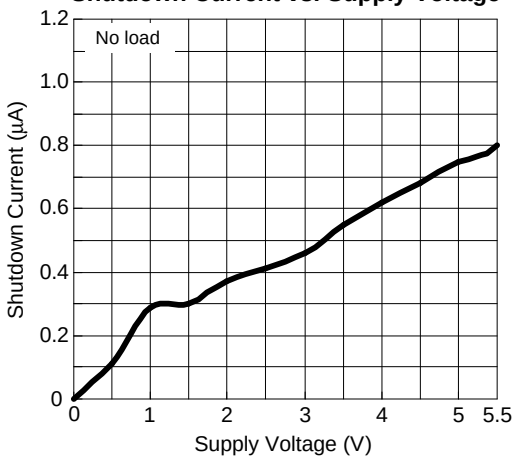
APA2011A Non-Clipping Function_WLCSP



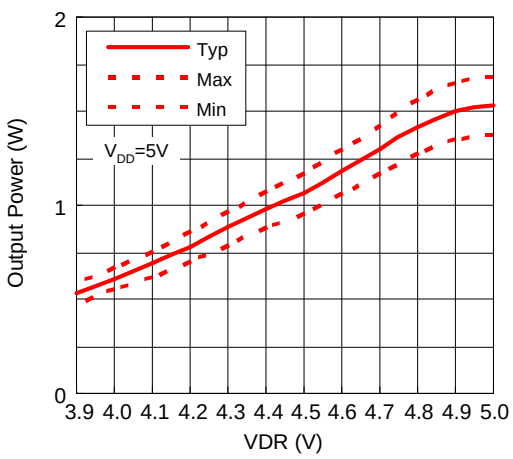
Supply Current vs. Supply Voltage



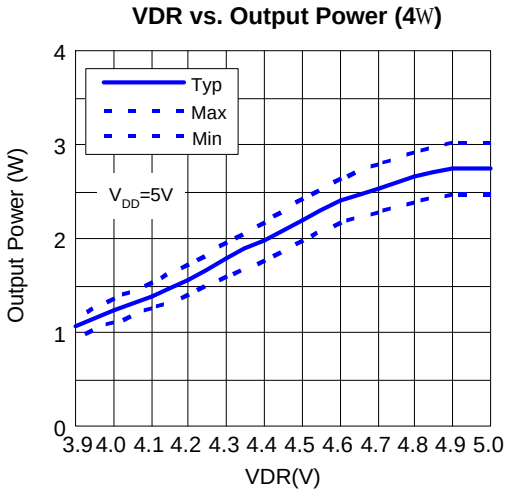
Shutdown Current vs. Supply Voltage



VDR vs. Output Power (8W)

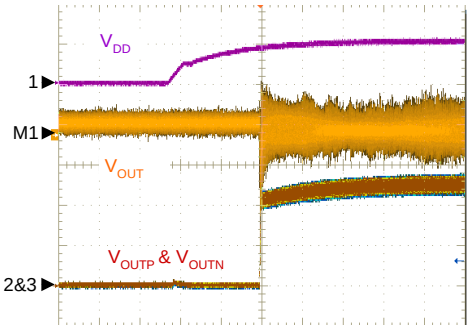


Typical Operating Characteristics (Cont.)



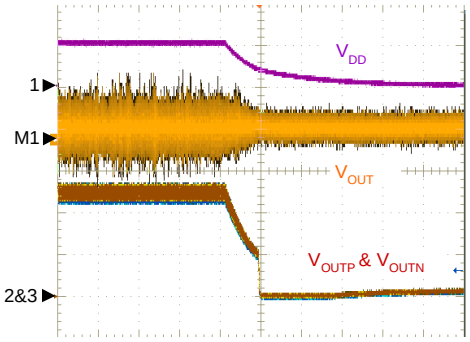
Operating Waveforms

Power On



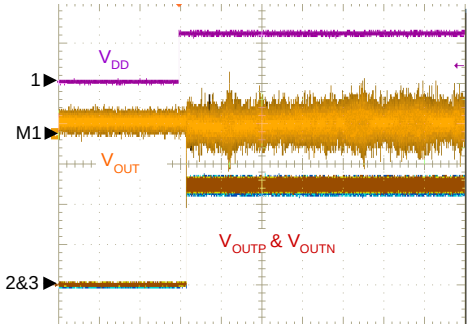
CH1: V_{DD}, 5V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUTN}, 1V/Div, DC
CHM1: V_{OUT}(CH2-CH3), 100mV/Div, DC
TIME: 2ms/Div

Power Off



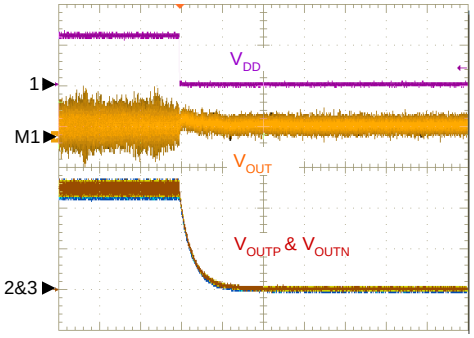
CH1: V_{DD}, 5V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUTN}, 1V/Div, DC
CHM1: V_{OUT}(CH2-CH3), 100mV/Div, DC
TIME: 40ms/Div

Shutdown Release



CH1: V_{SD}, 5V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUTN}, 1V/Div, DC
CHM1: V_{OUT}(CH2-CH3), 100mV/Div, DC
TIME: 20ms/Div

Shutdown

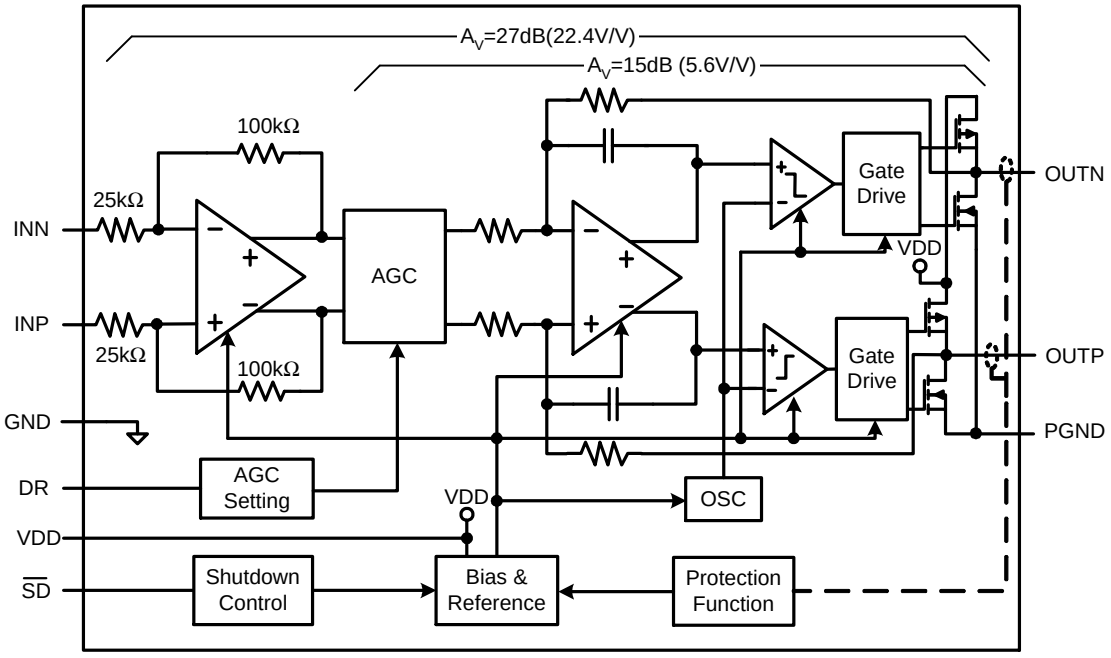


CH1: V_{SD}, 5V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUTN}, 1V/Div, DC
CHM1: V_{OUT}(CH2-CH3), 100mV/Div, DC
TIME: 1ms/Div

Pin Description

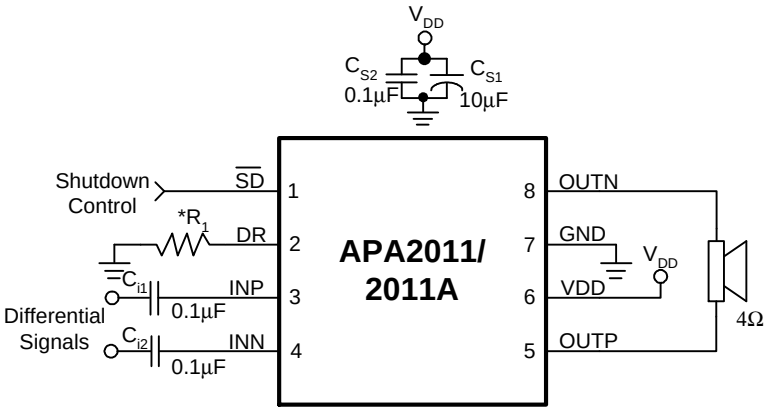
PIN			I/O/P	FUNCTION
NO.		NAME		
WLCSP1.5x1.5-9	TDFN3x3-8			
A1	3	INP	I	Positive Input of Power Amplifier.
A2	7	GND	P	Ground Connection for Circuitry.
A3	8	OUTN	O	Negative Output of Power Amplifier.
B1	2	DR	I	Setting the Maximum Output Power; Disable the DRC/Non-clipping, when $V_{DR}<0.2V_{DD}$, and if the $0.2V_{DD}<V_{DR}<0.55V_{DD}$, the V_{DR} is set to $0.55V_{DD}$ by internal, this is maximum power limit (Minimum the output power). $V_{DR}=\frac{R_1}{R_1+10k\Omega}\times V_{DD}$ $*P_O=\frac{2(V_{DR}-0.5V_{DD})^2}{R_{SPK}}$ R_{SPK}: Speaker Resistor Note: The setting value has 15% variation by IC process and this equation only for WLCSP1.5x1.5-9 package, the TDFN3x3-8 package's output power will less than the calculation.
B2	6	VDD	P	Supply Voltage Input Pin.
B3	-	PGND	P	Ground Connection for Power Stage
C1	4	INN	I	Negative Input of Power Amplifier.
C2	1	$\overline{SD}$	I	Shutdown Mode Control Input, Place entire IC in shutdown mode when held low.
C3	5	OUTP	O	Positive Output of Power Amplifier.

Block Diagram



Typical Application Circuit

Differential input mode (TDFN3x3-8)



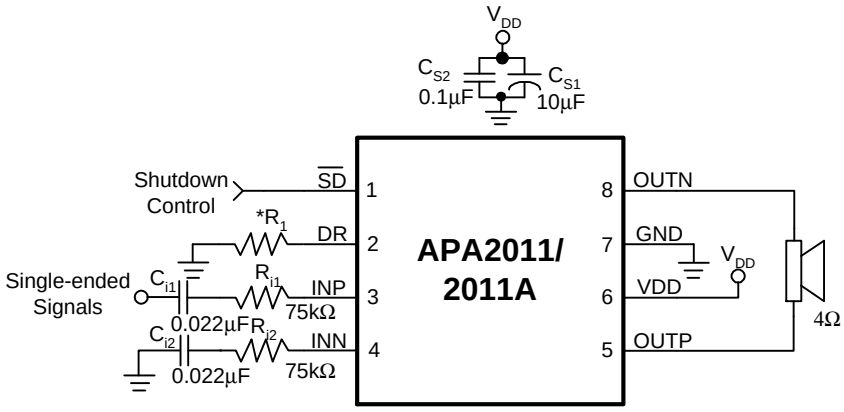
*R_1: Setting the Maximum Output Power

$$V_{DR}=\frac{R_1}{R_1+10k\Omega}\times V_{DD} \quad *P_O=\frac{2(V_{DR}-0.5V_{DD})^2}{R_{SPK}}$$

R_{SPK}: Speaker Resistor

Note : *The setting value has 15% variation by IC process and this equation only for WLCSP1.5x1.5-9 package, the TDFN3x3-8 package's output power will less than the calculation.

Single-Ended input mode (TDFN3x3-8) and A_V=15dB



*R_1: Setting the Maximum Output Power

$$V_{DR}=\frac{R_1}{R_1+10k\Omega}\times V_{DD} \quad *P_O=\frac{2(V_{DR}-0.5V_{DD})^2}{R_{SPK}}$$

R_{SPK}: Speaker Resistor

$$A_V=\frac{100k\Omega}{75k\Omega\,(R_{i1}\,\&\,R_{i2})+25k\Omega}\times 5.6=5.6(V/V),\ A_V=20Log5.6=15dB$$

Note : *The setting value has 15% variation by IC process and this equation only for WLCSP1.5x1.5-9 package, the TDFN3x3-8 package's output power will less than the calculation.

Function Description

Fully Differential Amplifier

The APA2011/2011A is a fully differential amplifier with differential inputs and outputs. The fully differential has some advantages versus traditional amplifier. First, don't need the input coupling capacitors because the common-mode feedback will compensate the input bias. The inputs can biased from 0.5V to V_{DD}-0.5V, and the outputs still be biased at mid-supply of APA2011/2011A. If the inputs are biased out of the input range, the coupling capacitors are required. Second, don't need the mid-supply capacitor (C_B) because any shift of the mid-supply of APA2011/2011A will have the same affect for both positive & negative channel, and will cancel at the differential outputs. Third, the fully differential amplifier will cancel the GSM RF transmitter's signal (217Hz).

Class D Operation

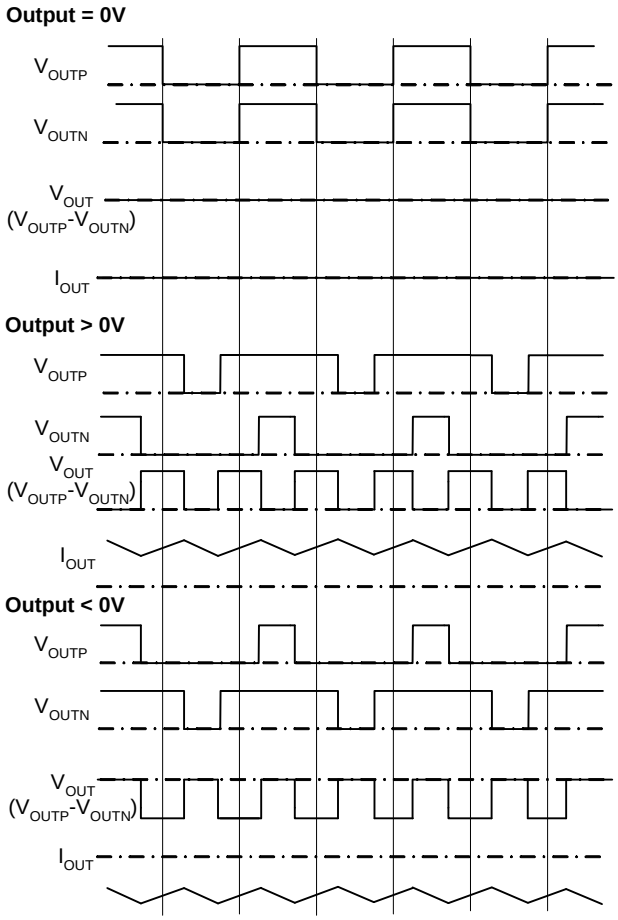


Figure 1. APA2011/2011 Output Waveform (Voltage & Current)

The APA2011/2011A modulation scheme is shown in figure 1. The outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output > 0V, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when output <0V, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load and reduces the I^2R losses in the load that improves the amplifier's efficiency. This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Non-Clipping Function (APA2011A)

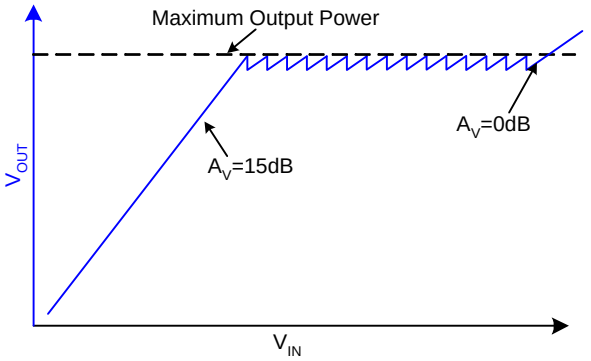


Figure 2. APA2011A Non-Clipping Control Function

The APA2011A provides the 15 steps Non-Clipping Control, and the range is from 15dB to 0dB, 1dB/step. When the output reaches the maximum power setting value, the internal Programmable Gain Amplifier (PGA) will decrease the gain for prevent the output waveform clipping. This feature prevents speaker damage from occurring clipping.

Using the DR pin to set the non-clipping function and limit the output power. Disable the AGC, when V_{DR}<0.2V_{DD}, and if the 0.2V_{DD}<V_{DR}<0.55V_{DD}, the V_{DR} is set to 0.55V_{DD} by internal, this is maximum power limit (Minimum the output power).

$$V_{DR} = \frac{R_1}{R_1 + 10k\Omega} \times V_{DD} \quad (1)$$

$$*P_O = \frac{2(V_{DR} - 0.5V_{DD})^2}{R_{SPK}} \quad R_{SPK}\text{: Speaker Resistor} \quad (2)$$

Function Description (Cont.)

Non-Clipping Function (APA2011A) (Cont.)

Note: *The setting value has 15% variation by IC process and this equation only for WLCSP1.5x1.5-9 package, the TDFN3x3-8 package's output power will less than the calculation.

Dynamic Range Control Function

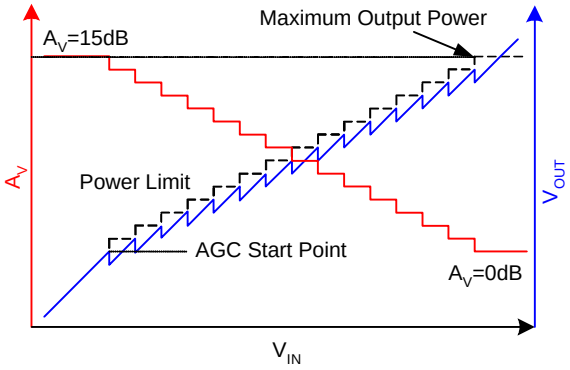
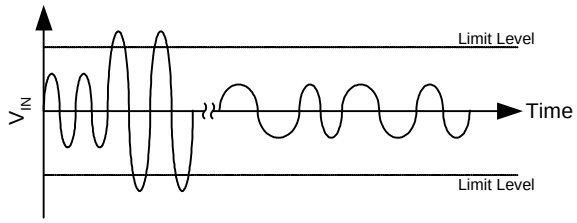


Figure 3. APA2011 Auto Gain Control Function

The APA2011 provides the 15 steps Dynamic Range Control (DRC), and the range is from 15dB to 0dB, 1dB/step. DRC provides continuous automatic gain adjustment to the amplifier through an internal Programmable Gain Amplifier (PGA). This feature enhances the perceived audio loudness and prevents speaker damage from occurring clipping at the same time.

The equations 1 & 2 are the method that set the maximum output power. If the R_1=40kΩ, the V_{DR} is 4V. Therefore, the maximum output power is 1.125W (R_L=4Ω), and the output voltage swing is limited at 3Vpp (1.5Vp) [The limited voltage can be calculated by 4V(V_{DR})-2.5V(Internal Bypass Voltage)=1.5V]. The AGC start point is 0.536V_{PP} (1.5Vp/5.6(A_V)=0.268V_P) at output, it means when the output power excesses 0.036W, the AGC will start work and decrease the gain by 1dB. If the input signal increase un-limit, the gain will be decreased until the maximum gain attenuation (15dB).



Attack Time and Release Time

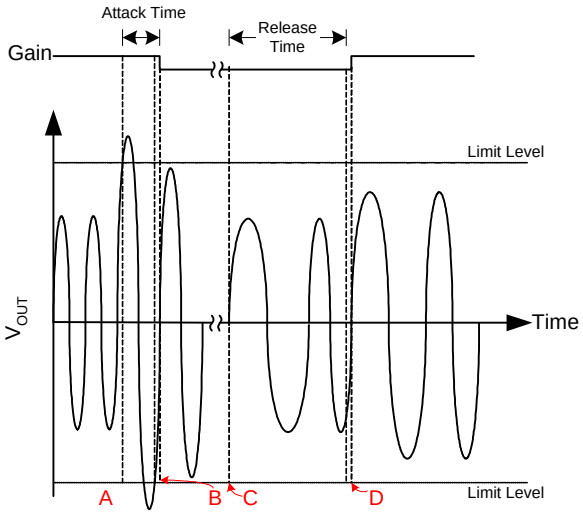


Figure 4. APA2011 Output Signal vs. Time

A. The output level excesses the AGC start point.
B. A to B is the attack time (32ms), but the Gain needs to change at output signal zero crossing.
C. The output level is under the limit level.
D. D to E is release time (512ms), but the Gain needs to change at output signal zero crossing..

When the APA2011/2011A senses the input signal excesses the start point of DRC/Non-clipping, it needs 32ms to decrease the gain, this calls "Attack Time". And if the input signal is small than the threshold about 512ms, the gain will be recovery, this time calls " release time".

The APA2011's compress ratio is 2:1, it means when the input signal has the 2dB change, the output signal will change 1dB. Because most small form speakers have only small dynamic range, the compress allows input signal with large dynamic range to fit into a small speaker with small dynamic rage.

And the APA2011A is just decrease the gain to avoid the output signal clipping, and the maximum control is 15dB gain.

Shutdown Operation

In order to reduce power consumption while not in use, the APA2011/2011A contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2011/2011A. The trigger point between

Function Description (Cont.)

Shutdown Operation (Cont.)

a logic high and logic low level is typically 1.4V. It is best to switch between the ground and the supply voltage VDD to provide maximum device performance. By switching the $\overline{SD}$ pin to a low level, the amplifier enters a low-consumption- current state, I_{DD} for APA2011/2011A is in shutdown mode. On normal operating, APA2011/2011A's $\overline{SD}$ pin should pull to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Over-Current Protection

The APA2011/2011A monitors the output current. When the current exceeds the current-limit threshold, the APA2011/2011A turns off the output stage to prevent the output device from damages in over-current or short-circuit condition. The IC will turn on the output buffer after 1ms, but if the over-current or short-circuits condition still remains, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has be removed.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA2011/2011A. When the junction temperature exceeds T_J = +150 °C, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about 125 °C. The thermal protection is designed with a 25 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Application Information

Square Wave Into The Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jump out the air gap and deface the voice coil. However, this depends on the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 500kHz switching frequency, this is not issued for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor, R_i

The APA2011/2011A's input resistor is fixed and the value is 25kΩ. The input resistance has wide variation (+/-5%) is caused by manufacture. The gain also can be set by the external resistors (Riexr).

$$A_V = \frac{100k\Omega}{R_i + R_{iexr}} \times 5.6 = \frac{100k\Omega}{25k\Omega + Riexr(R_{i1} \& R_{i2})} \times 5.6 \quad (3)$$

For fully differential operating, the R_{iexr} (R_{i1}& R_{i2}) match is very important for CMRR, PSRR, and harmonic distortion performance. It's recommended to use 1% tolerance resistor or better. Keep the input trace as short as possible to limit the noise injection. The gain is recommended to set 5.6V/V or lower for optimal the APA2011/2011A's performance.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (4)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 25kΩ (minimum) and the specification calls for a flat bass response down to 100Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (5)$$

When the input resistance variation is considered, the C_i is 0.064μF, so a value in the range of 0.1μF to 0.22μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifier input is held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Ferrite Bead Selection

If the traces form APA2011/2011A to speaker is short, the ferrite bead filters can reduce the high frequency radiated to meet the FCC & CE required.
A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output Low-Pass Filter

If the traces form APA2011/2011A to speaker are short, it don't require output filter for FCC & CE standard.
A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The figure 5 is the sample for added ferrite bead; the ferrite show choosing high impedance in high frequency.

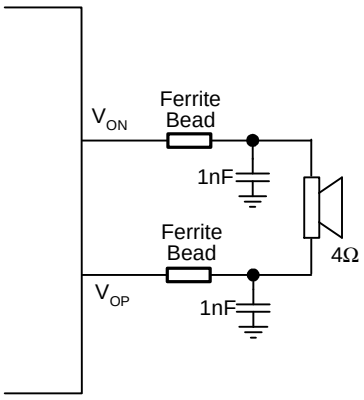


Figure 5. Ferrite Bead Output Filter

Figure 6 and 7 and are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace form amplifier to speaker is too long, and needs to eliminate the radiated emission or EMI.

Application Information (Cont.)

Output Low-Pass Filter (Cont.)

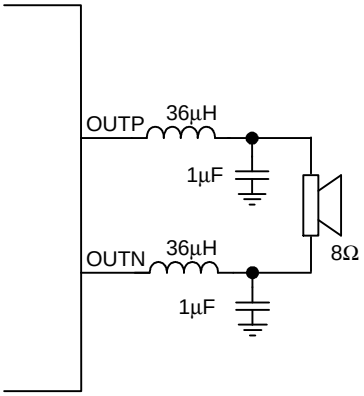


Figure 6. LC output filter for 8Ω speaker

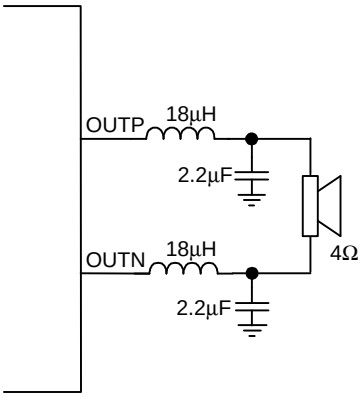


Figure 7. LC Output Filter for 4Ω Speaker

Figure 6 and 7's low pass filter cut-off frequency are 25kHz (F_C).

$$f_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (6)$$

Power-Supply Decoupling Capacitor, C_s

The APA2011/2011A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that targets on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device VDD pin for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

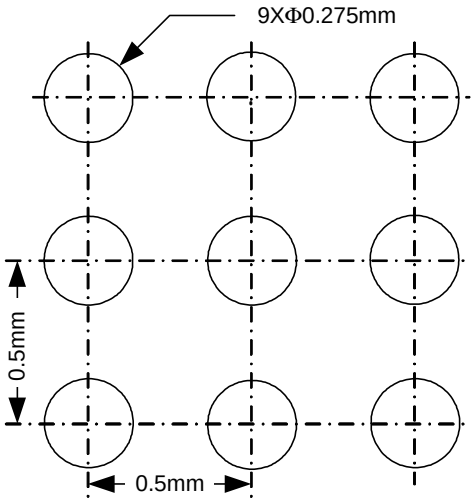


Figure 8. WLCSP1.5x1.5-9 Land Pattern Recommendation

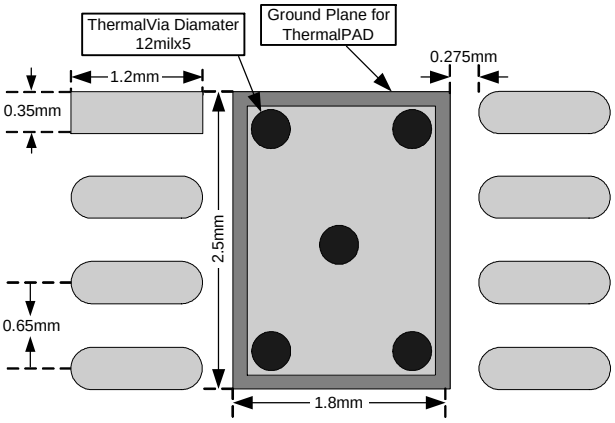


Figure 9. TDFN3x3-8 Land Pattern Recommendation

1. All components should be placed close to the APA2011/2011A. For example, the input capacitor (C_i) should be close to APA2011/2011A's input pins to avoid causing noise coupling to APA2011/2011A's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2011's power pin to decouple the power rail noise.

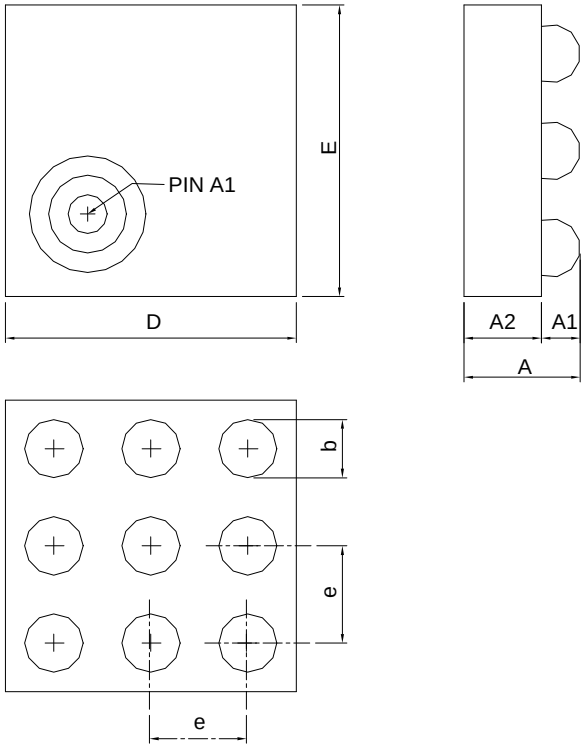
Application Information (Cont.)

Layout Recommendation (Cont.)

2. The output traces should be short, wide (>50mil) and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The TDFN3x3-8 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

Package Information

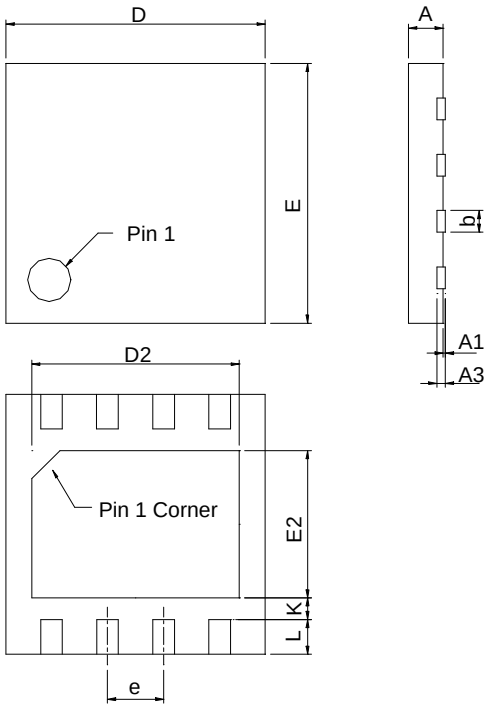
WLCSP1.5x1.5-9



SYMBOL	WLCSP1.5x1.5-9			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.53	0.67	0.021	0.026
A1	0.20	0.24	0.008	0.009
A2	0.33	0.43	0.013	0.017
b	0.29	0.31	0.011	0.012
D	1.47	1.53	0.058	0.060
E	1.47	1.53	0.058	0.060
e	0.50 BSC		0.020 BSC	

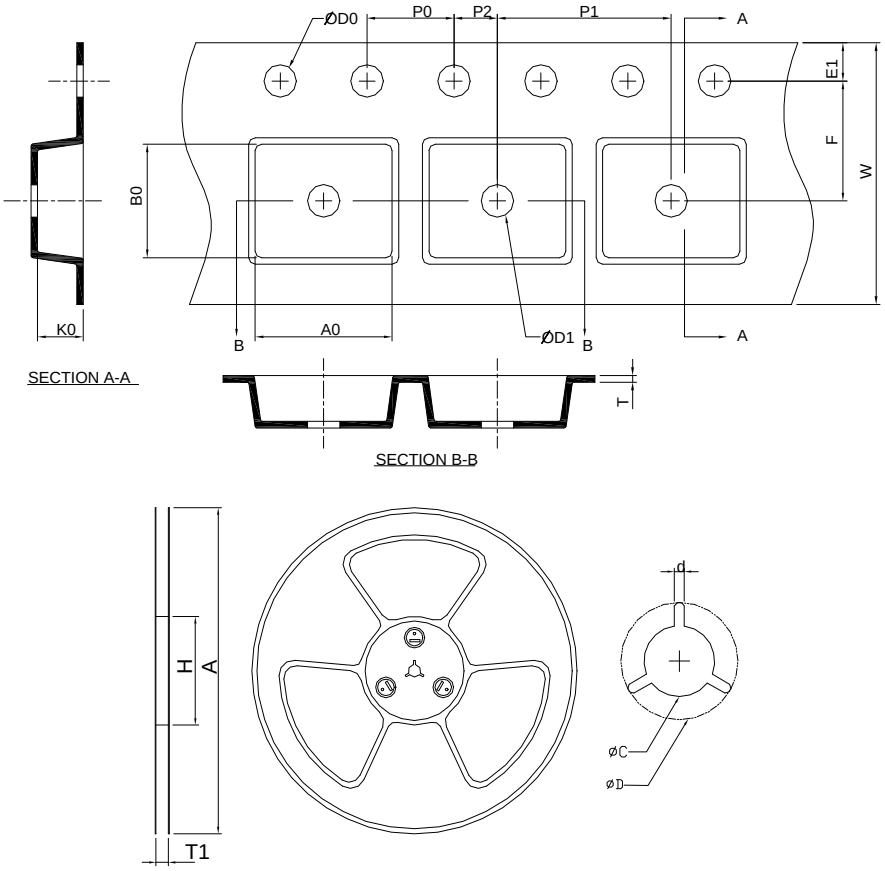
Package Information

TDFN3x3-8



SYMBOL	TDFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	2.90	3.10	0.114	0.122
D2	1.90	2.40	0.075	0.094
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.5x1.5-9	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.70±0.20	1.70±0.20	0.90±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-8	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

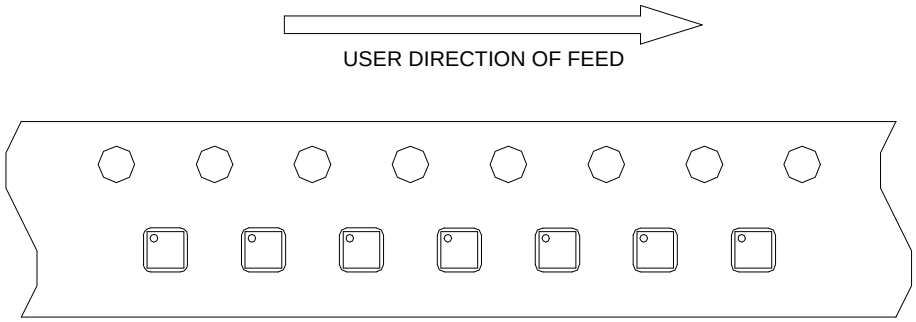
(mm)

Devices Per Unit

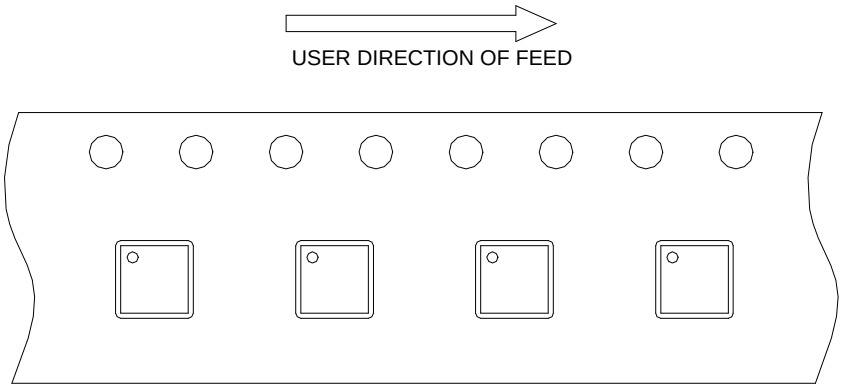
Package Type	Unit	Quantity
WLCSP1.5x1.5-9	Tape & Reel	3000
TDFN3x3-8	Tape & Reel	3000

Taping Direction Information

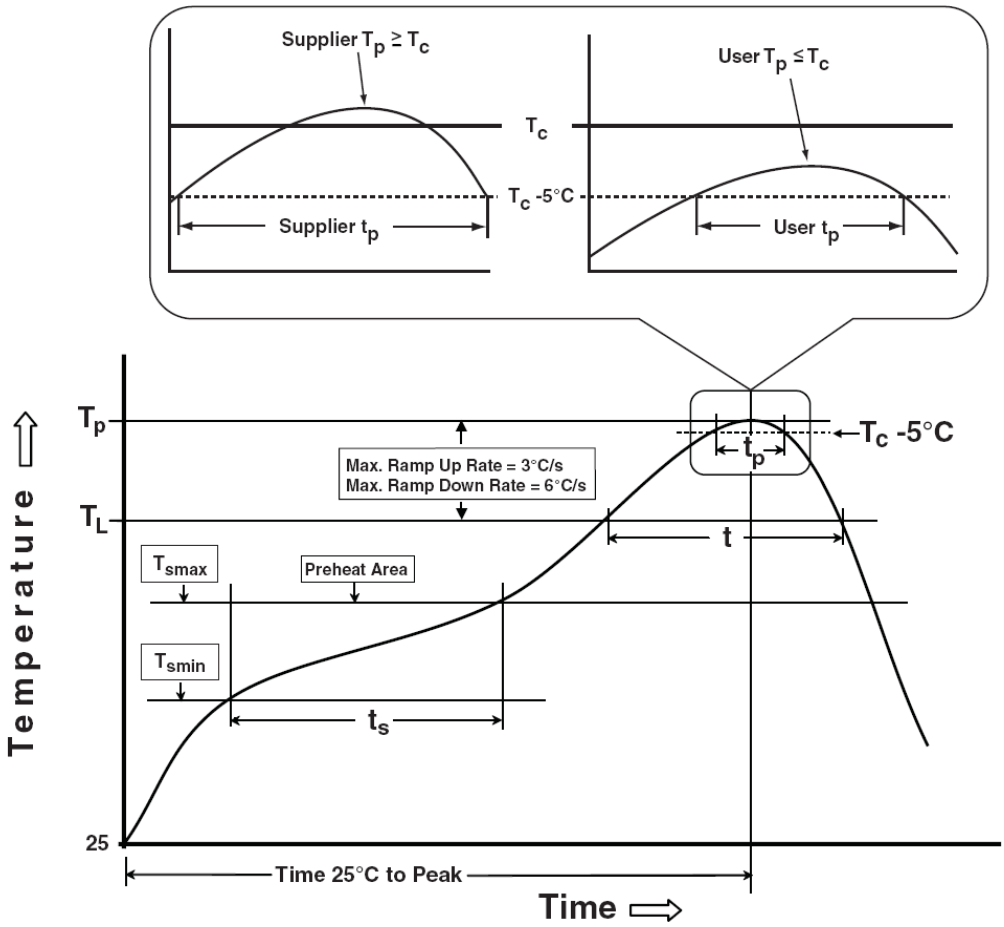
WLCSP1.5x1.5-9



TDFN3x3-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838