

## Description

The μPD27C4001 is a 4,194,304-bit ultraviolet erasable EPROM fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 524,288 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C4001 has a single-location programming feature, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage ( $V_{PP}$ ) of 12.5 volts and is available in a 32-pin cerdip with quartz window.

## Features

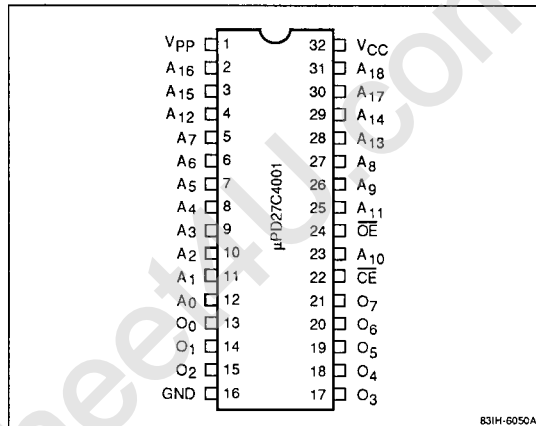
- 524,288-word by 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed programming
- Low power dissipation
  - 30 mA (active)
  - 100 μA (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging with a quartz window
- JEDEC-compatible pinout

## Ordering Information

Part Number	Access Time (max)	Package
μPD27C4001DZ-15	150 ns	32-pin cerdip with quartz window
DZ-17	170 ns	
DZ-20	200 ns	

## Pin Configuration

### 32-Pin Cerdip



## Pin Identification

Symbol	Function
$A_0 - A_{18}$	Address inputs
$O_0 - O_7$	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
GND	Ground
$V_{CC}$	+5-volt power supply
$V_{PP}$	Program voltage

**Absolute Maximum Ratings**

Power supply voltage, $V_{CC}$	-0.6 to +7.0 V
Input voltage, $V_{IN}$	-0.6 to $V_{CC} + 0.3$ V
Input voltage, $A_9$	-0.6 to +13.5 V
Output voltage, $V_{OUT}$	-0.6 to +7.0 V
Operating temperature, $T_{OPR}$	-10 to +80°C
Storage temperature, $T_{STG}$	-65 to +125°C
Program voltage, $V_{PP}$	-0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Capacitance**

$T_A = 25^\circ\text{C}$ ;  $f = 1$  MHz;  $V_{IN}$  and  $V_{OUT} = 0$  V

Parameter	Symbol	Max	Typ	Unit
Input capacitance	$C_{IN}$	14		pF
Output capacitance	$C_{OUT}$	16		pF

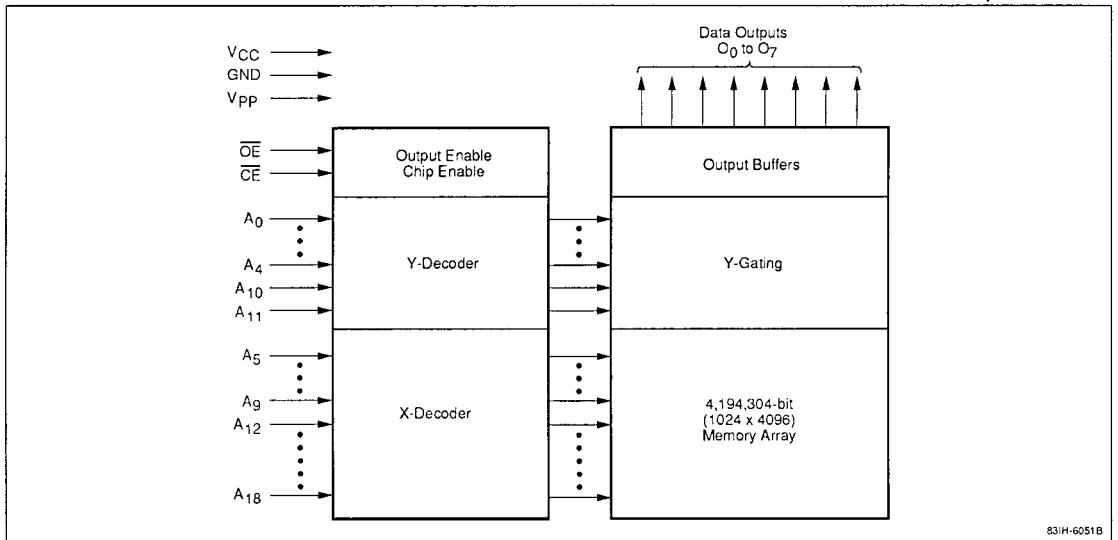
**Truth Table**

Function	$\overline{CE}$	$\overline{OE}$	$V_{PP}$	$V_{CC}$	Outputs
Read	$V_{IL}$	$V_{IL}$	+5.0 V	+5.0 V	$D_{OUT}$
Output disable	$V_{IL}$	$V_{IH}$	+5.0 V	+5.0 V	High-Z
Standby	$V_{IH}$	X	+5.0 V	+5.0 V	High-Z
Program verify	X	$V_{IL}$	+12.5 V	+6.5 V	$D_{OUT}$
Program	$V_{IL}$	$V_{IH}$	+12.5 V	+6.5 V	$D_{IN}$
Program inhibit	$V_{IH}$	$V_{IH}$	+12.5 V	+6.5 V	High-Z

**Notes:**

- (1) "X" can be either  $V_{IL}$  or  $V_{IH}$ .

**Block Diagram**



## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
<b>Read Operation or Standby</b>					
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{PP}$	$V_{CC} - 0.6$	$V_{CC}$	$V_{CC} + 0.6$	V
Input voltage, high	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	0		70	°C
<b>Programming Operation</b>					
Supply voltage	$V_{CC}$	6.25	6.5	6.75	V
	$V_{PP}$	12.2	12.5	12.8	V
Input voltage, high	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	20	25	30	°C

## DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{V} \pm 10\%$ ;  $V_{PP} = V_{CC} \pm 0.6\text{V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Read Operation, Output Disabled, and Standby</b>						
Output voltage, high	$V_{OH1}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
	$V_{OH2}$	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu\text{A}$
Output voltage, low	$V_{OL}$		0.45		V	$I_{OL} = 2.1\ \text{mA}$
Output leakage current	$I_{LO}$	-10		10	$\mu\text{A}$	$\overline{OE} = V_{IH}$ ; $V_{OUT} = 0\ \text{V to } V_{CC}$
Input leakage current	$I_{LI}$	-10		10	$\mu\text{A}$	$V_{IN} = 0\ \text{V to } V_{CC}$
Operating supply current	$I_{CCA1}$			30	mA	$\overline{CE} = V_{IL}$ ; $V_{IN} = V_{IH}$
	$I_{CCA2}$			30	mA	$f = 6.7\ \text{MHz}$ ; $I_{OUT} = 0\ \text{mA}$
Standby supply current	$I_{CCS1}$			1	mA	$\overline{CE} = V_{IH}\ \text{min}$
	$I_{CCS2}$		1	100	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2\ \text{V}$ ; $V_{IN} = 0\ \text{V to } V_{CC}$
Program voltage current	$I_{PP}$		1	100	$\mu\text{A}$	$V_{PP} = V_{CC}$

## DC Characteristics (cont)

$T_A = +25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5\text{V} \pm 0.25$ ;  $V_{PP} = +12.5\text{V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Programming Operation</b>						
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
Output voltage, low	$V_{OL}$		0.45		V	$I_{OL} = 2.1\ \text{mA}$
Input leakage current	$I_{LI}$	-10		10	$\mu\text{A}$	$V_{IN} = 0\ \text{to } V_{CC}$
Operating supply current	$I_{CC}$			30	mA	
Program voltage current	$I_{PP}$			30	mA	$\overline{CE} = V_{IL}$ ; $\overline{OE} = V_{IH}$

**AC Characteristics**

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5.0 V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>

Parameter	Symbol	μPD27C4001-15		μPD27C4001-17		μPD27C4001-20		Unit	Test Conditions (Note 1)
		Min	Max	Min	Max	Min	Max		
<b>Read Operation and Standby</b>									
Address to output delay	t <sub>ACC</sub>		150		170		200	ns	$\overline{OE} = \overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t <sub>CE</sub>		150		170		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t <sub>OE</sub>		70		70		75	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ to data output float delay	t <sub>DF</sub>	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold time	t <sub>OH</sub>	0		0		0		ns	$\overline{OE} = \overline{OE} = V_{IL}$

**AC Characteristics (cont)**

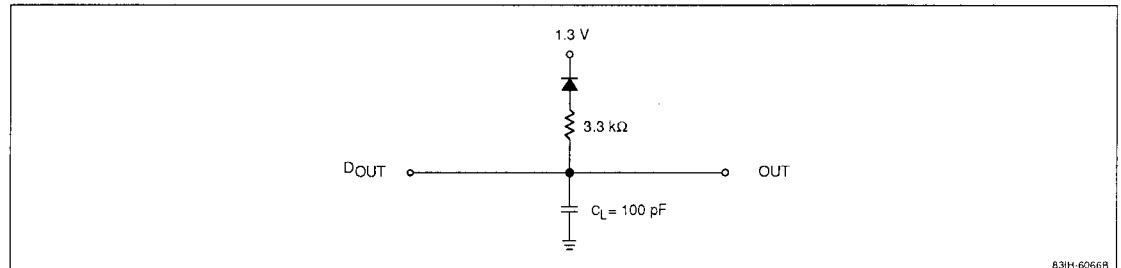
T<sub>A</sub> = +25 ± 5°C; V<sub>CC</sub> = +6.5 V ± 0.25; V<sub>PP</sub> = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions (Note 1)
<b>Programming Operation</b>						
Address setup time	t <sub>AS</sub>	2			μs	
$\overline{OE}$ setup time	t <sub>OES</sub>	2			μs	
Data setup time	t <sub>DS</sub>	2			μs	
Address hold time	t <sub>AH</sub>	2			μs	
Data hold time	t <sub>DH</sub>	2			μs	
Output enable to output float delay	t <sub>DF</sub>	0		130	ns	
V <sub>PP</sub> setup time	t <sub>VPS</sub>	2			μs	
Program pulse width	t <sub>PW</sub>	0.095	0.1	0.105	ms	
V <sub>CC</sub> setup time	t <sub>VCS</sub>	2			μs	
Data valid from $\overline{OE}$	t <sub>OE</sub>			150	ns	

**Notes:**

- (1) Inputs levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

**Figure 1. Output Load**



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### PROGRAMMING OPERATION

Begin programming by erasing all data; this sets all bits at a high logic level. The μPD27C4001 is originally shipped in this condition. To enter data, apply valid data at the eight output pins of the chosen address. Raise  $V_{CC}$  to  $+6.5\text{ V} \pm 0.25$ ; then raise  $V_{PP}$  to  $+12.5\text{ V} \pm 0.3$ .

$\overline{OE}$  should be set high to to start programming the initial address. Apply a 0.1-ms program pulse to  $\overline{CE}$  as shown in the programming portion of the timing waveforms. Set  $\overline{OE}$  low to verify the eight bits prior to making a program/no program decision. If the address is not programmed, apply another 0.1-ms pulse to  $\overline{CE}$ , up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower  $V_{PP}$  and then  $V_{CC}$  to  $+5.0\text{ V} \pm 10\%$  and verify all data again.

### Program Inhibit

This option is used to program multiple μPD27C4001s connected in parallel. All like inputs except  $\overline{CE}$  and  $\overline{OE}$  may be common. Program individual devices by applying a high level to all  $\overline{OE}$  pins and a low-level TTL pulse to the  $\overline{CE}$  pin of the device to be programmed. Applying a high-level signal to the  $\overline{CE}$  pins of the other devices prevents them from being programmed.

### Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to all  $\overline{CE}$  pins and a low logic level applied to the  $\overline{OE}$  pin of the device to be verified. A high logic level should be applied to the  $\overline{OE}$  pins of all other devices.

### Program Erasure

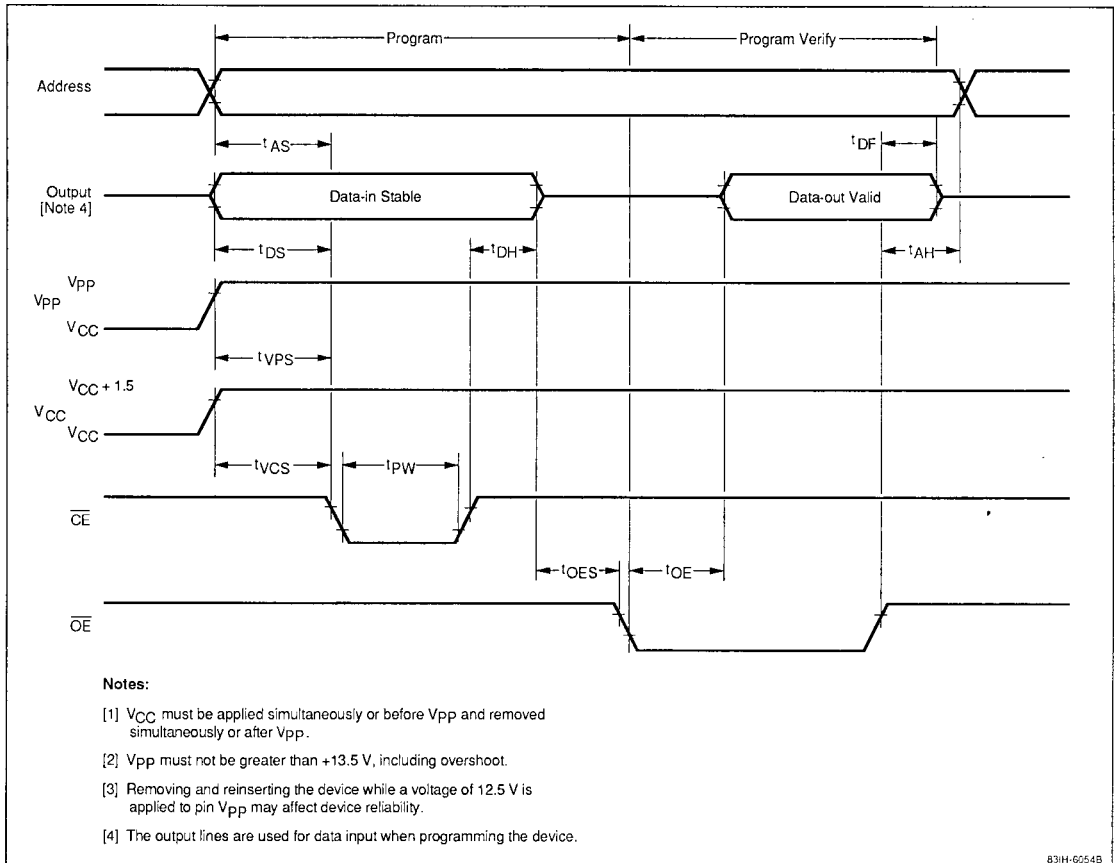
Erase data on the μPD27C4001 by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm<sup>2</sup> (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm<sup>2</sup> takes approximately 20 minutes to complete erasure. Place the μPD27C4001 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

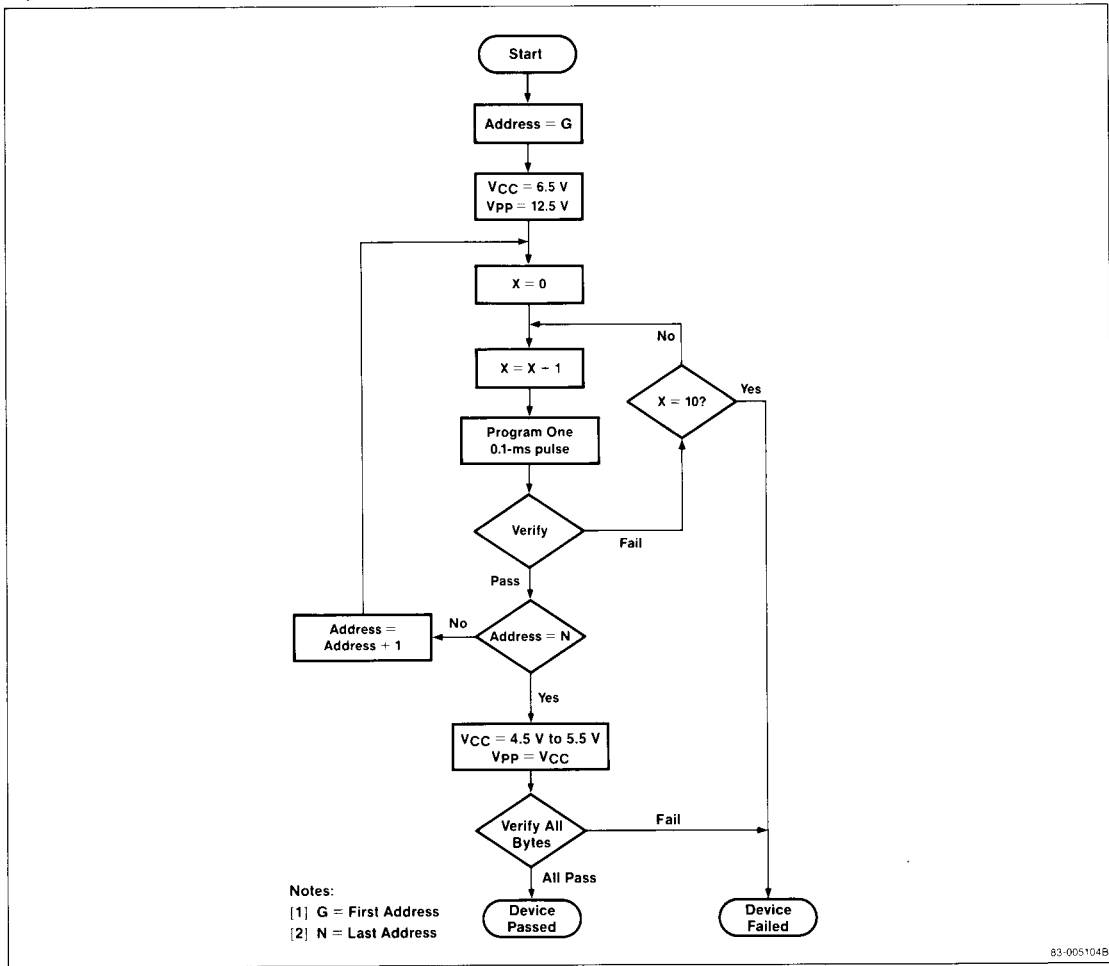
Timing Waveforms

Programming Cycle



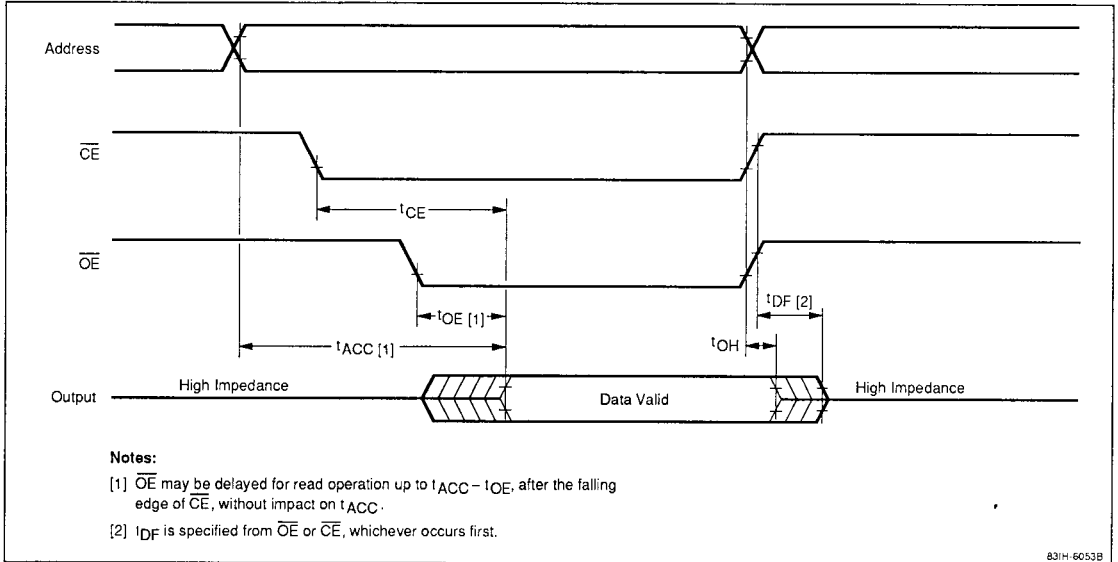
831H-6054B

**Figure 2. Programming Flowchart**



Timing Waveforms (cont)

Read Cycle



831H-6053B