Low-Power, High-Speed, Latchable CMOS Analog Switches

Features

- Latched Control Inputs
- Rail-to-Rail Analog Input Range
- On-Resistance: 25 Ω
- Fast Switching Action—t_{ON}: 170 ns
- Micropower Requirements—P_D: 35 nW
- TTL and CMOS Logic Compatible
- Low Leakage: 40 pA

Benefits

- µP Compatible
- Wide Dynamic Range
- Reduced Component Count
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery-Compatible Operation

Applications

- Data Bus Switching
- Sample-and-Hold Circuits
- Programmable Filters
- µP Controlled Analog Systems
- Portable Instruments
- Telecommunication Systems

Description

The DG421/423/425 are monolithic analog switches featuring latchable logic inputs to simplify interfacing with microprocessors. This series combines fast switching speed (t_{ON}: 170 ns, typ), and low on-resistance ($r_{DS(on)}$: 25 Ω, typ) making it ideally suited for battery powered industrial and military applications that require microprocessor compatible analog switches.

The DG421 has two normally open switches (SPST). The DG423 has two single-pole, double-throw (SPDT) pairs. The DG425 has two normally open pairs (DPST).

To achieve high-voltage ratings and superior switching performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

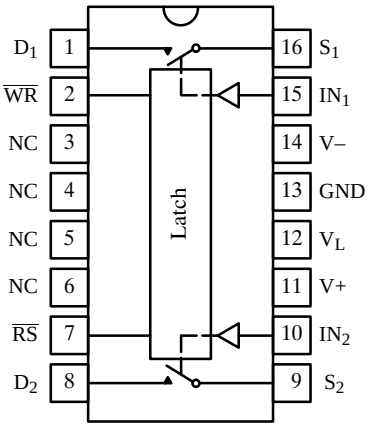
Each switch conducts equally well in both directions when on and blocks input voltages up to the supply rail voltages when off.

The input data latches become transparent when $\overline{WR}$ is set low. When $\overline{WR}$ goes high the latches store the logic control data. A low on $\overline{RS}$ resets all switches to their default state (all inputs low).

Functional Block Diagram and Pin Configuration

DG421

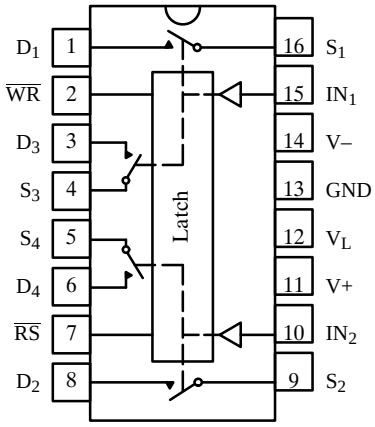
Dual-In-Line



Top View

DG425

Dual-In-Line



Top View

Truth Table – DG421/DG425

$\overline{WR}$	$\overline{RS}$	IN_X	Switch
0	1	0	OFF
		1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

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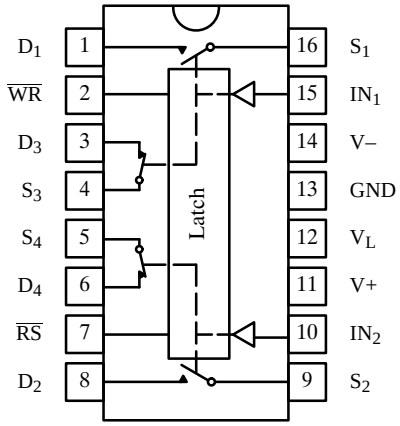
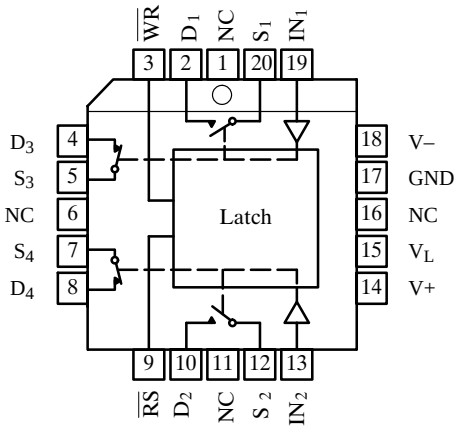
Functional Block Diagram and Pin Configuration (Cont'd)

DG423
Dual-In-Line



Top View

DG423
PLCC



Top View

Truth Table – DG423

$\overline{WR}$	$\overline{RS}$	IN_X	SW_1, SW_2	SW_3, SW_4
0	1	0	OFF	ON
		1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Ordering Information – DG421/423/425

Temp Range	Package	Part Number
–40 to 85°	16-Pin Plastic DIP	DG421DJ
		DG423DJ
		DG425DJ
	20-Pin PLCC	DG423DN

Latch Operation Truth Table

IN_X	$\overline{RS}$	$\overline{WR}$	Latch/Switch X
X	1	0	Transparent latch operation
X	1	⌐	Control data latched-in, switches on or off as selected by last IN_X
X	0	X	All latches reset, switches on or off as when IN_X = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 1
X	⌐	X	

Absolute Maximum Ratings

Voltages Referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
V_L . . . . . (GND –0.3 V) to (V+) +0.3 V
Digital Inputs[a] V_S, V_D . . . . . V– minus 2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . 40 mA
Current, S or D (Pulsed 1 ms, 10% duty) . . . . . 100 mA
Storage Temperature . . . . . –65 to 125°C

Power Dissipation (Package)[b]

16-Pin Plastic DIP[c] . . . . . 470 mW
20-Pin PLCC[d] . . . . . 800 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

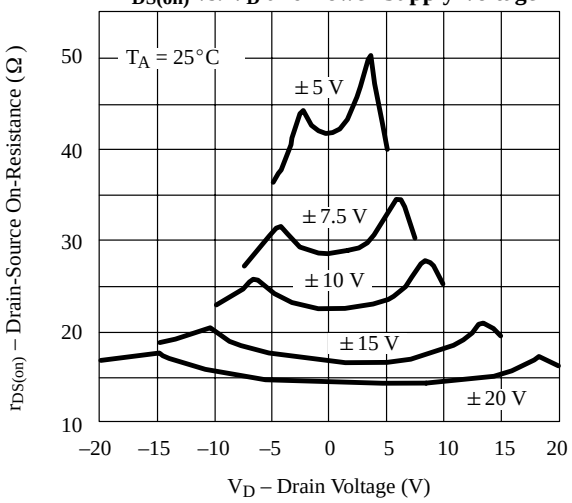
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±8.5 V V+ = 13.5 V, V– = –13.5 V	Room Full		25	35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V– = –16.5 V V_D = ∓15.5 V, V_S = ±15.5 V	Room Full	–0.25 –5	±0.01	0.25 5	nA
	$I_{D(off)}$		Room Full	–0.25 –5	±0.01	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V– = –16.5 V	Room Full	–0.4 –10	±0.04	0.4 10	
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, all other = 2.4 V	Full	–0.5	0.005	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V, all other = 0.8 V	Full	–0.5	0.005	0.5	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room Full		170	250 300	ns
Turn-Off Time	t_{OFF}		Room Full		140	200 200	
Latch Timing	t_{WW}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V	Room Full	200 200			
	t_{DW}		Room Full	100 100			
	t_{WD}		Room Full	60 100			
Break-Before-Make Time Delay	t_D	DG423 Only, R_L = 300 Ω, C_L = 35 pF See Figure 3	Room	5	25		
Charge Injection[d]	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω, See Figure 4	Room		60		pC
Off Isolation Reject Ratio	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		65		dB
Crosstalk (Channel-to-Channel)	X_{TALK}	Between Any Two Channels R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		76		
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz	Full		9		pF
Drain Off Capacitance	$C_{D(off)}$		Full		9		
Channel On Capacitance	$C_{D(on)}$		Full		35		
Power Supply							
Positive Supply Current	I+	V+ = 16.5 V, V– = –16.5 V V_{IN} = 0 or 5 V	Room Full		0.0001	1 5	µA
Negative Supply Current	I–		Room Full	–1 –5	–0.0001		
Logic Supply Current	I_L		Room Full		0.0001	1 5	
Ground Current	I_{GND}		Room Full	–1 –5	–0.0001		

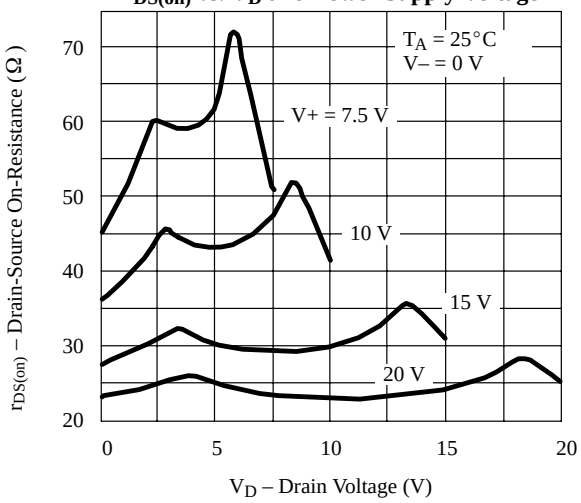
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Typical Characteristics

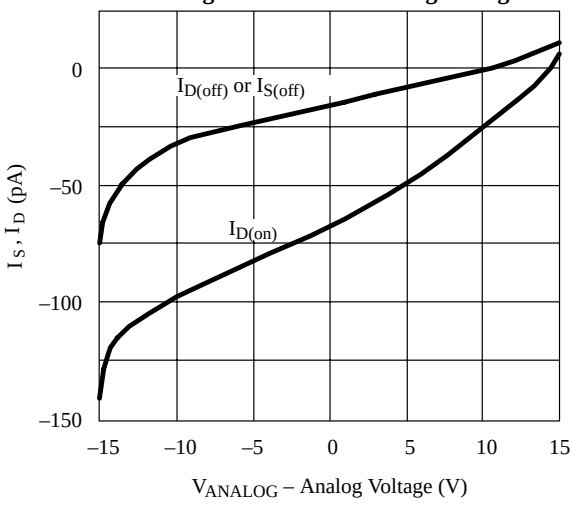
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



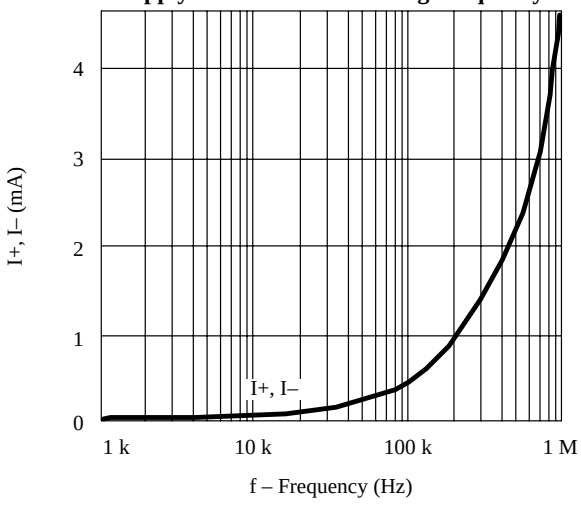
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



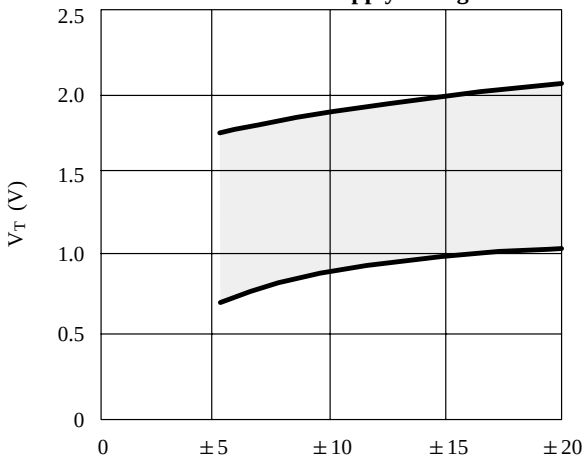
Leakage Currents vs. Analog Voltage



Supply Currents vs. Switching Frequency



Input Switching Theshold vs. V+ and V– Supply Voltages



Schematic Diagram (Typical Channel)

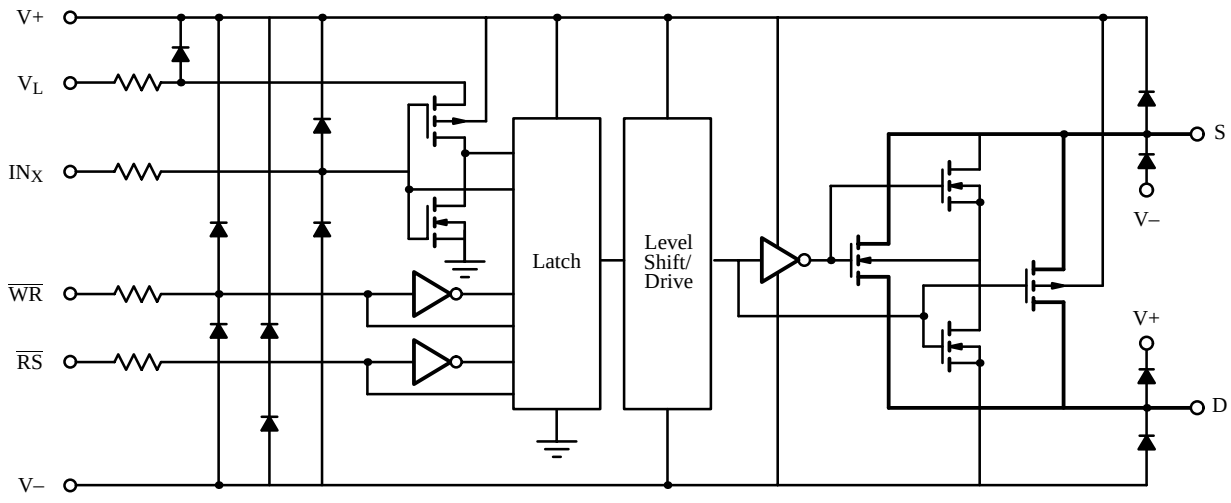
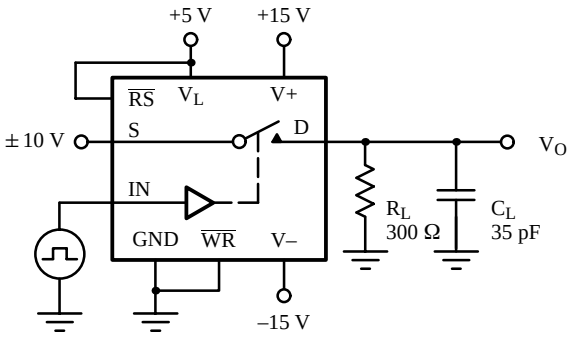


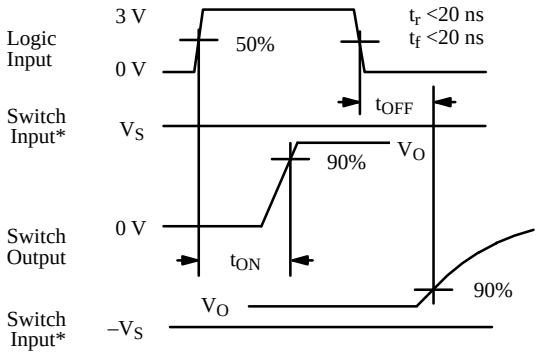
Figure 1.

Test Circuits



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



*V_S = 10 V for t_{ON}, V_S = –10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

Test Circuits (Cont'd)

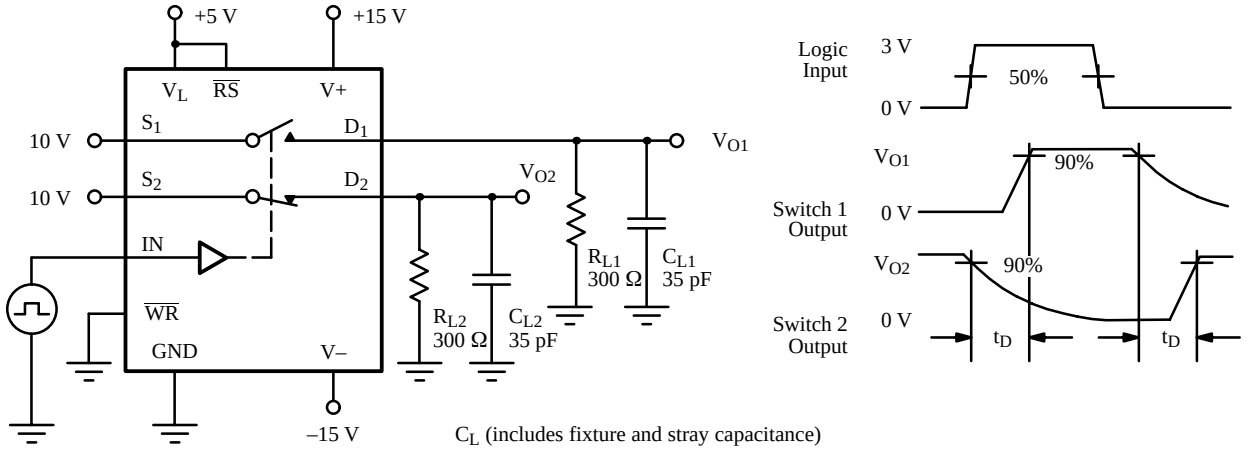


Figure 3. Break-Before-Make

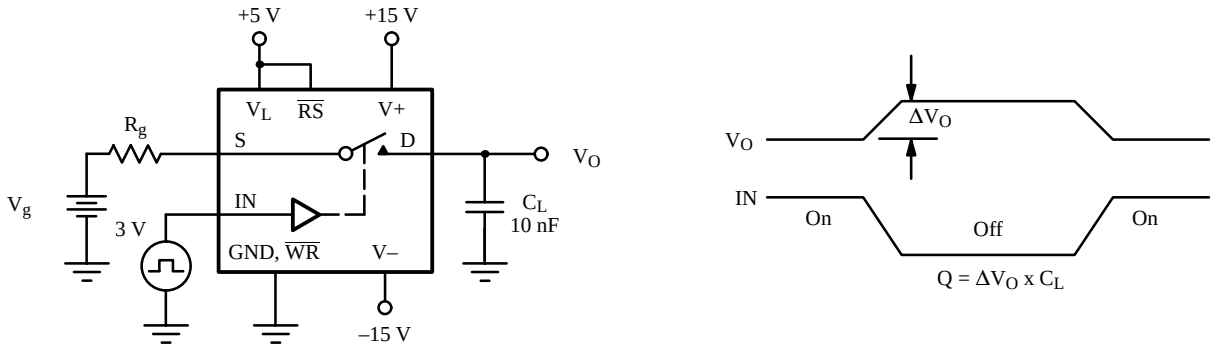


Figure 4. Charge Injection

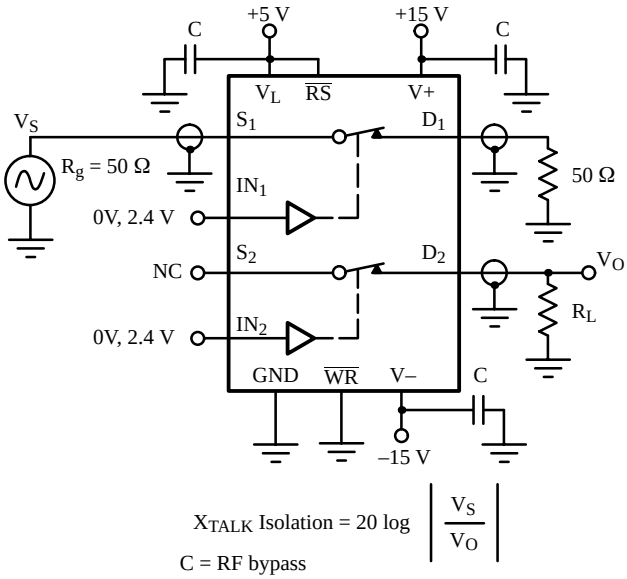


Figure 5. Crosstalk

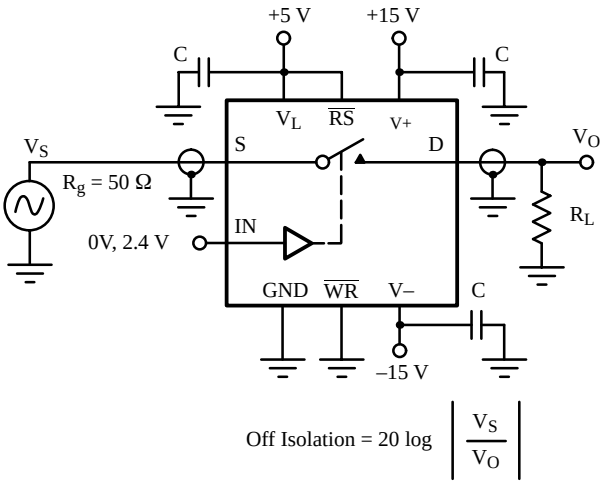


Figure 6. Off Isolation

Test Circuits (Cont'd)

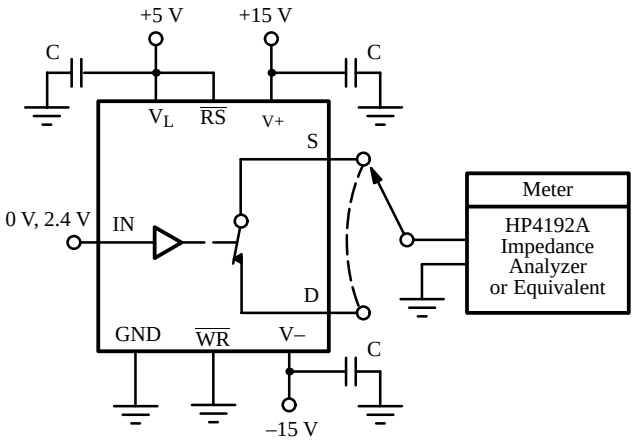


Figure 7. Source/Drain Capacitances

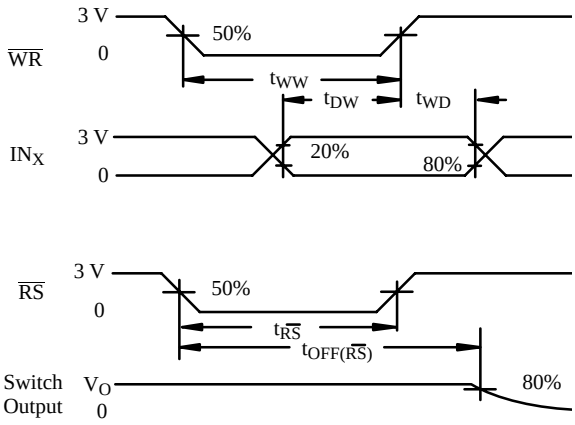


Figure 8. Latch Timing

Applications

Figure 9 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates with a sign plus magnitude code. A sign bit of "0" connects R_3 to GND, giving 12-bit resolution per quadrant.

12-Bit Plus Sign Magnitude Code Table

Sign Bit	Digital Input MSB		LSB	Analog Output (V_{OUT})
0	1111	1111	1111	$+(4095/4096)V_{IN}$
0	0000	0000	0000	0 V
1	0000	0000	0000	0 V
1	1111	1111	1111	$+(4095/4096)V_{IN}$

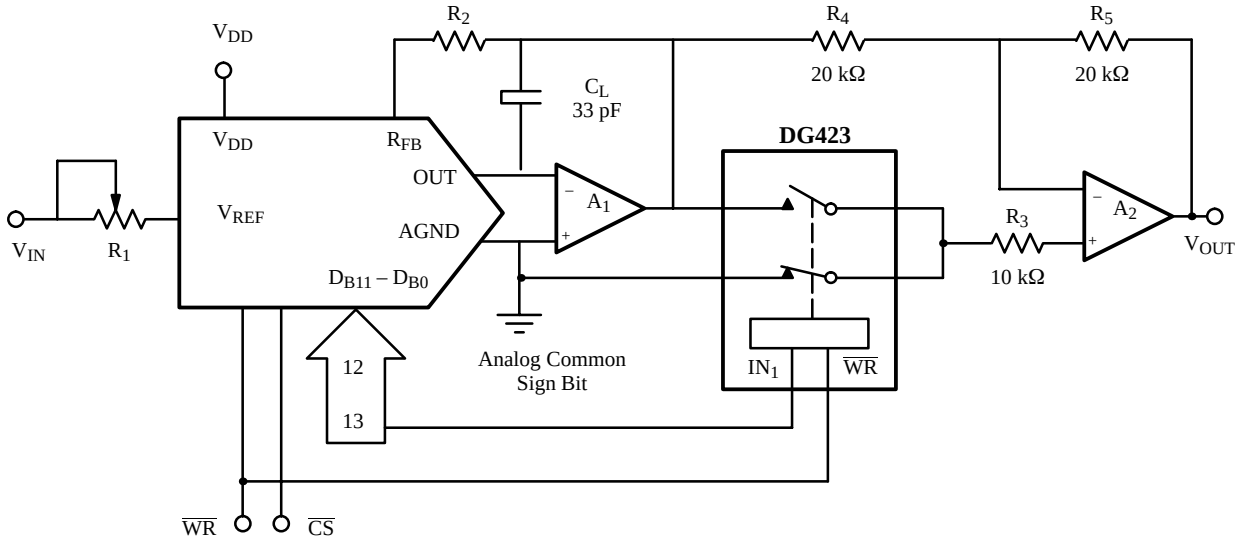


Figure 9. 12-Bit Plus Sign Magnitude D/A Converter

Applications

When switch S_1 of Figure 10 is closed, the op amp is placed in the familiar unity-gain non-inverting configuration. When switch S_2 is closed and S_1 is open the gain is given by:

$$A_V = 1 + \frac{R_1}{R_2}$$

The microprocessor system $\overline{WR}$ must gate the decoder output to ensure proper timing.

Figure 11 shows a balanced-line microphone input stage that provides selection or summing between two balanced-line microphones and also performs differential-to-single-ended conversion. Either MIC A or MIC B can be selected, and neither and/or both may be summed at the output. This configuration uses "virtual ground" switching, a method which minimizes distortion resulting from the analog switch on-resistance modulation. The actual voltage swings experienced by the analog switch barely exceed 1 V for a 15-V full-scale range input.

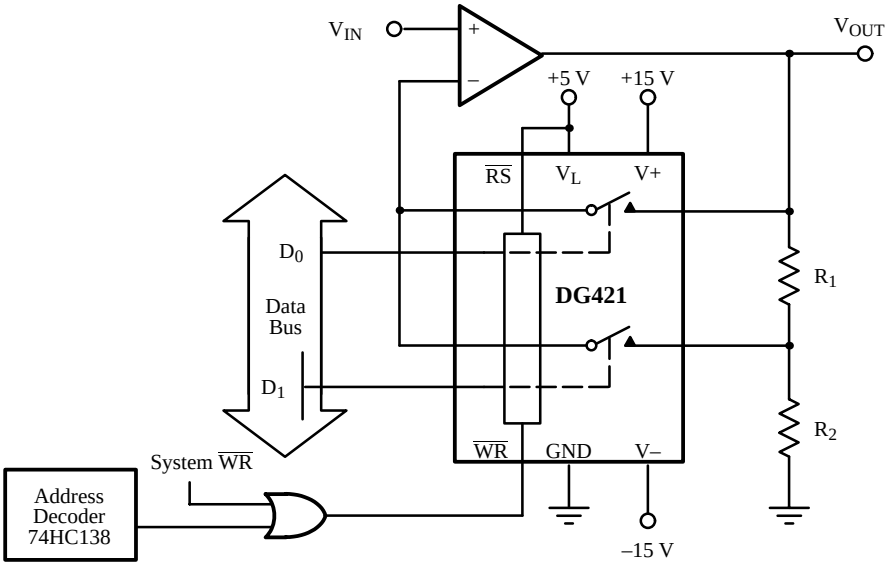
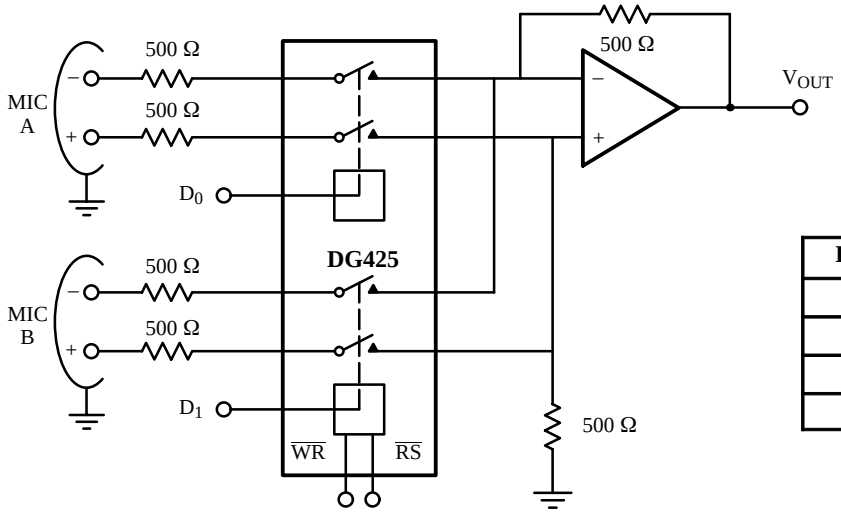


Figure 10. Bus-Controlled Precision Gain-Ranging Circuit



D_1	D_2	Output
0	0	None
0	1	MIC A
1	0	MIC B
1	1	MIC A and MIC B

Figure 11. Bus-Controlled Selector for Balanced-Line Microphones