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High-Speed Clock Synthesizer Evaluation Board GD90590

Preliminary

General Description

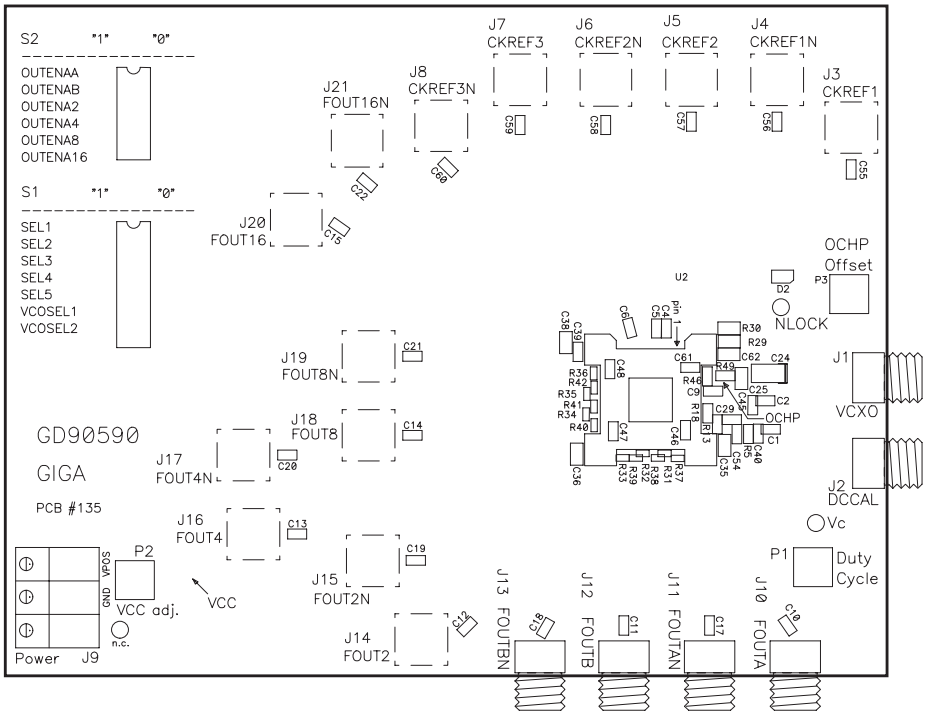
The GD90590 Evaluation Board is designed for testing the performance of the high-speed integrated device GD16590, a high-speed clock synthesizer with PLL.

The GD16590 generates six differential high-speed clocks from a common on-chip VCO or an external VCXO. The on-chip integrated PLL locks the outputs to one of three selectable input reference clocks.

All outputs are DC terminated on the evaluation board.

During the board design special attention has been paid to optimise the overall performance, with consideration of the GD16590's linear characteristics.

De-coupling capacitors are located as close as possible to the device, and the signal carrying traces in the PCB are kept free from via holes, sharp corners etc. to make the transmission line design as smooth as practically possible.



Features

- Easy evaluation of high-speed performance in carefully designed PCB.
- High-speed data in/outputs available via standard SMA connectors.
- Integrated 50 Ω transmission lines in the PCB ensure matching interconnection of input and output signals.
- Input and output signals are AC coupled, i.e. the device can be used with circuits with positive as well as negative supply.
- Single unregulated power supply: +6 V, 400 mA.
- Board dimensions: 101 × 133 mm incl. connectors.
- Gerber files for PCB layout available on request.

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Functional Details

General

The GD16590 offers a fully integrated PLL including on-chip VCO, and with inputs for use of an external VCXO. Three selectable differential reference clock inputs and six subdivided differential oscillator outputs are available on the GD90590 evaluation board.

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Reference Clock inputs

The three differential reference clock inputs (J3/J4, J5/J6 and J7/J8) are AC coupled LVPECL inputs, internally terminated in the GD16590 device. Selection of the active input is done from DIP switch (S1).

Clock Output Signals

The subdivided clock outputs are generated as differential LVPECL signals. Each signal is DC terminated on the board via 120 Ω to ground. The signals are AC coupled out of the board to the SMA connectors (J10…J21). The signals can be DC coupled to the load if the internal termination resistors are removed and the coupling capacitors are replaced by 0 Ω resistors. Each of the six outputs can be switched off by pulling the corresponding LVT select signal (OUTENAx) to ground. The output select signals are controlled by DIP switch (S2).

Important note: Failure to terminate an active (enabled) output may cause degradation of the device performance.

Loop Filter

The PLL loop filter is composed of the components R49/C24. For a specific application the mounted default values may need to be changed for optimum performance since the jitter performance of the PLL depends on the input frequency. There is space for an additional loop filter capacitor (C25). When the internal VCO is used, the loop current flows from OCHP via R46 to the VCTL input.

On-board VCXO

The GD90590 evaluation board comprises a VCXO mounted in position U4. This VCXO may be used as an alternative to the VCO integrated in the GD16590. When the VCXO is used the control loop for the PLL comprises an active loop filter composed of the operations amplifier (U3 - LMV358M). The filter, which has a DC adjustment of the working point in P3, controls the VCXO (U4 - VF900409). The VCXO output is AC coupled via C45 to the VCXO input terminal of the GD16590. The VCXO input is a differential input to the GD16590. Hence the trigger point of the device, i.e. the input duty cycle can be adjusted by P1.

External Oscillator

An alternative to the on-chip VCO and the on-board VCXO is to add an external clock signal. Use J1 (VCXO) for single ended input or J1/J2 (VCXO/DCCAL) for differential input. The external clock is terminated in R13/R18. Remove capacitors C40 and C45 to avoid stub reflections and conflicts with U4.

When using single ended input duty cycle can be adjusted by means of P1, if R5 = 470 Ω is mounted.

Mode Control

The GD16590 compares selected reference clock input signal with the selected subdivided oscillator frequency. The charge pump output OCHP reflects the phase relationship between the compared signals. The frequency of the charge pump output (the error signal frequency) follows the reference clock frequency directly. This means the gain of the PLL loop is directly proportional with the input reference clock frequency. Hence you should expect the jitter performance of the application to be dependent on the reference clock frequency in use.

General Purpose Clock Divider Operation

In addition to the frequency limited clean-up operation the GD16590 can be used as a general purpose high speed clock divider. The clock input is J1(/J2) as described above, and one or more outputs will provide a binary divided clock output in the terminals J10…J21, depending on the output enable signal setting in DIP switch (S2).

Power Supply

The GD90590 evaluation board may be powered from an unregulated power supply, delivering +6 V, 400 mA minimum.

A stabilised 3.3 V supply for the GD16590 is generated locally on the board.

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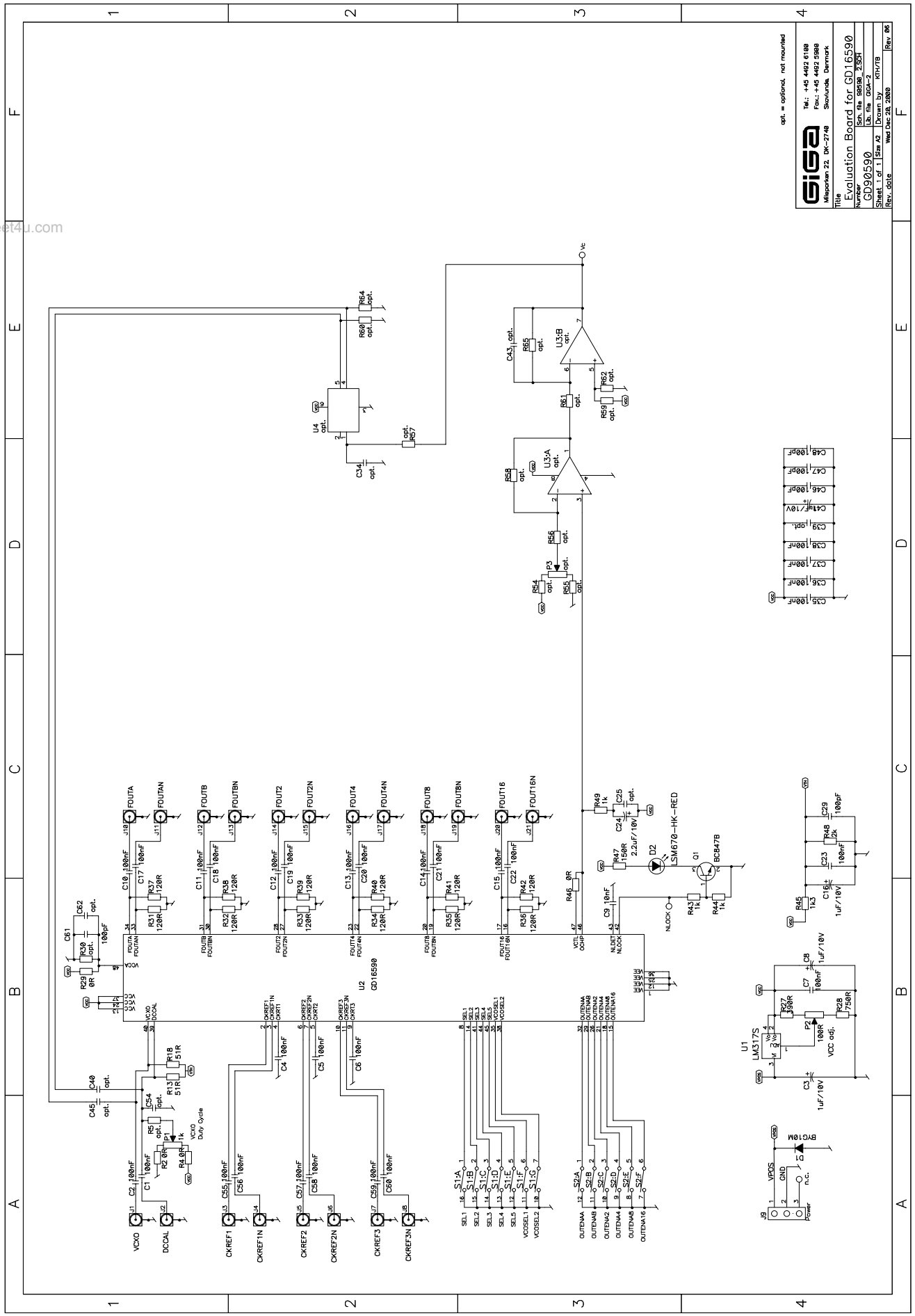

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DIP Switch Factory Settings

S1 – Divisor select, Clock input select.

ON = 0, OFF = 1

S1-1	On	SEL1 control	Select input reference source.
S1-2	On	SEL2 control	
S1-3	Off	SEL3 control	Select clock frequency for phase detector input.
S1-4	On	SEL4 control	
S1-5	On	SEL5 control	
S1-6	On	VCOSEL1 control	Select clock source for the divider.
S1-7	Off	VCOSEL2 control	

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Please refer to GD16590 Data Sheet for description.

S2 - Output enable selection

ON = 0 = Output Disable, OFF = 1 = Output Enable

S2-1	Off	Output FOUTA
S2-2	Off	Output FOUTB
S2-3	On	Subdivided Output FOUT2
S2-4	On	Subdivided Output FOUT4
S2-5	On	Subdivided Output FOUT8
S2-6	On	Subdivided Output FOUT16

References

- GD16590 Data Sheet (latest revision).
- GD16590 Test Report, available from GIGA A/S.

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Ordering Information

To order, please specify as shown below:

Order Number:	Description:
GD90590	The evaluation kit comprises: Evaluation board in antistatic bag GD16590 device mounted on the board How to get started GD90590 Data sheet (this document)

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