Integrated Device Technology, Inc.

CMOS HIGH-SPEED STATIC RAM 72K (8K X 9-BIT)

ADVANCE INFORMATION
IDT7169S
IDT7169L

FEATURES:

- 8192-words x 9-bits organization
- JEDEC standard 28-pin DIP, SOJ, and 32-Pin LCC
- Fast access time:
  - — Commercial: 20/25/35ns (max.)
  - — Military: 25/35/45/55ns (max.)
- Battery backup operation
  - — 2V data retention (L-version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL-compatible
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7169 is a 73,728-bit high-speed static RAM organized as 8K x 9. It is fabricated using IDT's high-performance, high-reliability CEMOS™ technology.

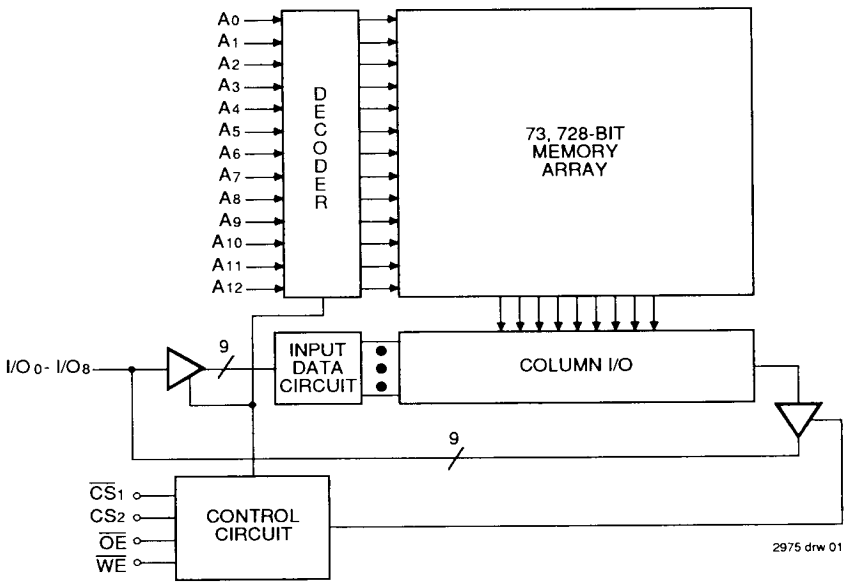
The IDT7169 offers address access times as fast as 15ns. The ninth bit is optimal for systems using parity.

All inputs and outputs of the IDT7169 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT7169 is packaged in an industry standard 300-mil 28-pin ceramic and plastic DIP and SOJ, along with a 32-pin LCC package.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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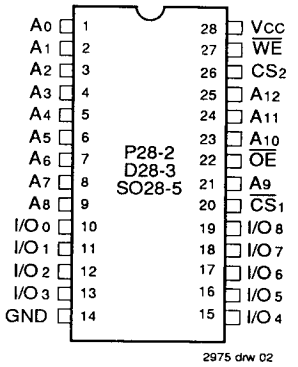
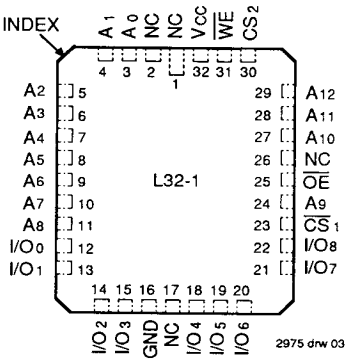
PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE[1]

CS2	$\overline{CS_1}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	High Z	Deselect chip, Power down
L	X	X	X	High Z	Deselct chip
H	L	L	H	DOUT	Read
H	L	X	L	DIN	Write
H	L	H	H	High Z	Outputs Disabled

NOTE: 2975 tbl 01
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +135	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2975 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2975 tbl 03
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2975 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2975 tbl 04
1. VIL = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7169S20 7169L20		7169S25 7169L25		7169S35 7169L35		7169S45/55 7169L45/55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = 0[2]	S	90	—	90	110	90	100	—	100	mA
		L	80	—	80	100	80	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = f_{MAX}[2]	S	180	—	170	190	150	160	—	160	mA
		L	160	—	150	170	130	140	—	130	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS_1}$ ≥ V_{IH}, V_{CC} = Max., CS_2 = V_{IL} Outputs Open, f = f_{MAX}[2]	S	20	—	20	20	20	20	—	20	mA
			L	3	—	3	5	3	5	—	5
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[2] $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC} CS_2 ≤ V_{LC}, V_{CC} = Max.	S	15	—	15	20	15	20	—	20	mA
		L	0.2	—	0.2	1.0	0.2	1.0	—	1.0	

2975 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2975 tbl 07

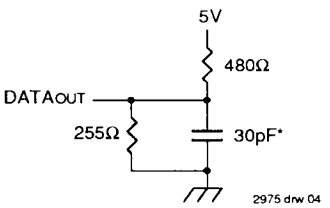


Figure 1. Output Load

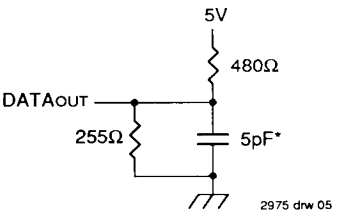


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7169S Min.	IDT7169S Max.	IDT7169L Min.	IDT7169L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}, CS_2 = V_{IL}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

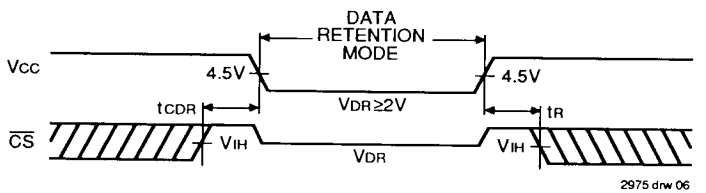
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	1. $\overline{CS_1} \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2975 tbl 09

LOW Vcc DATA RETENTION WAVEFORM



2975 drw 06

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7169S20[1] 7169L20[1]		7169S25 7169L25		7169S35 7169L35		7169S45/55[3] 7169L45/55[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45/55	—	ns
tAA	Address Access Time	—	19	—	25	—	35	—	45/55	ns
tACS1	Chip Select-1 Access Time	—	20	—	25	—	35	—	45/55	ns
tACS2	Chip Select-2 Access Time	—	25	—	35	—	40	—	45/55	ns
tCLZ1, 2	Chip Select to Output in Low Z[2]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	12	—	18	—	25/30	ns
tOLZ	Output Enable to Output in Low Z[2]	3	—	3	—	3	—	3	—	ns
tCHZ1, 2	Chip Select-1, 2 to Output in High Z[2]	—	9	—	13	—	15	—	20/25	ns
tOHZ	Output Disable to Output in High Z[2]	—	8	—	10	—	15	—	20/25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	20	—	25	—	35	—	45/55	—	ns
tAW	Address Valid to End of Write	15	—	18	—	25	—	33/50	—	ns
tCW1	Chip Select to End of Write ($\overline{CS_1}$)	15	—	18	—	25	—	33/50	—	ns
tCW2	Chip Select to End of Write (CS_2)	15	—	18	—	25	—	33/50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	21	—	25	—	25/50	—	ns
tWR1	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
tWHZ	Write Enable to Output in High Z[2]	—	8	—	10	—	14	—	18/25	ns
tDW	Data to Write Time Overlap	10	—	13	—	15	—	20/25	—	ns
tDH1	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
tOW	Output Active from End of Write[2]	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed but not tested.
3. -55° to +125°C. temperature range only.

2975 tbl 10

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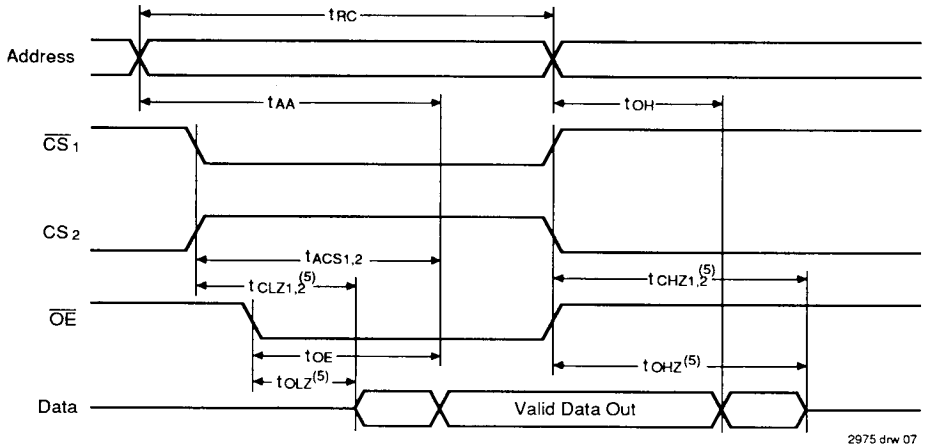
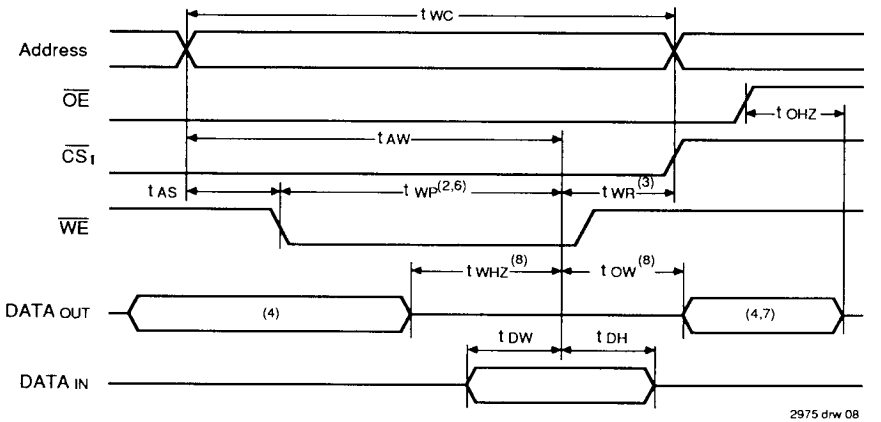
TIMING WAVEFORM OF READ CYCLE (1)



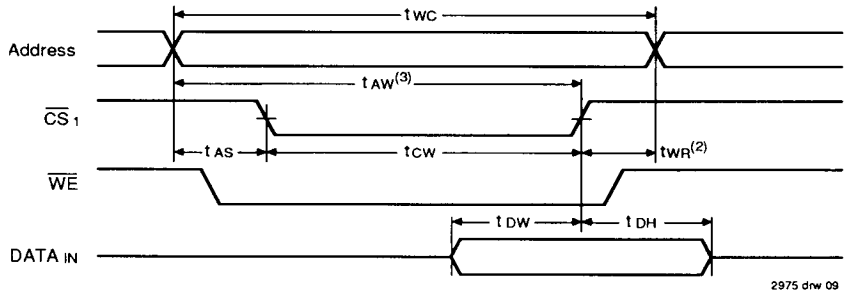
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low and CS_2 transition high.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS_1}$ and a high CS_2.
3. tWR1, 2 is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ +tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWR.
7. DATAOUT is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1,3]



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
3. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
4. Transition is measured ±200mV from steady state.

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ORDERING INFORMATION