

GENERAL DESCRIPTION

The ML86V7655 is an NTSC/PAL compatible digital video encode. It encodes digital image data such as ITU-R BT.656 and ITU-R BT.601 to analog video signals.

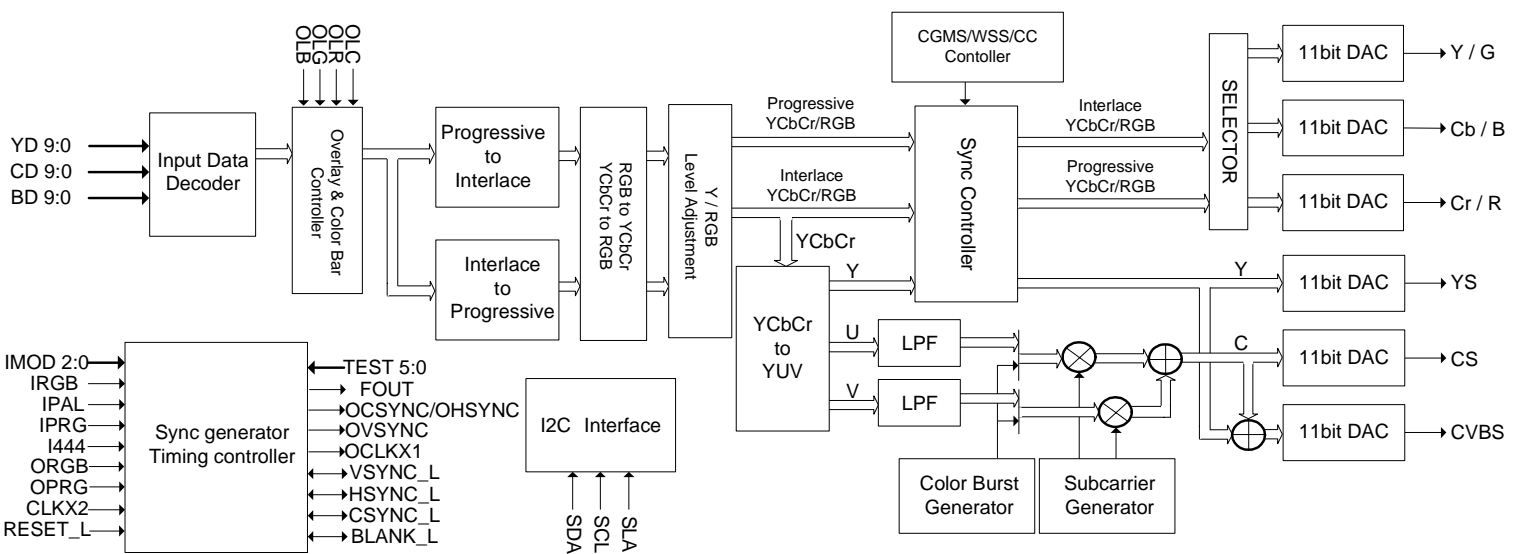
As digital input, RGB (4:4:4), YCbCr (4:4:4), and progressive scan signals are supported besides generic ITU-R BT.601 and ITU-R BT.656. As analog video output, RGB and component signals can be output in interlace or progressive format in addition to NTSC/PAL S-Video and composite outputs. DAC simultaneous 6-channel output or independent output for each channel can be selected. With the I/P and P/I conversion function, interlaced digital signals can be output as progressive signals or progressive digital signals can be output as interlaced signals. The ML86V7656 supports Macrovision copy protection (compliant with version 7.1.L1 for interlace and version 1.2 for progressive).

FEATURES

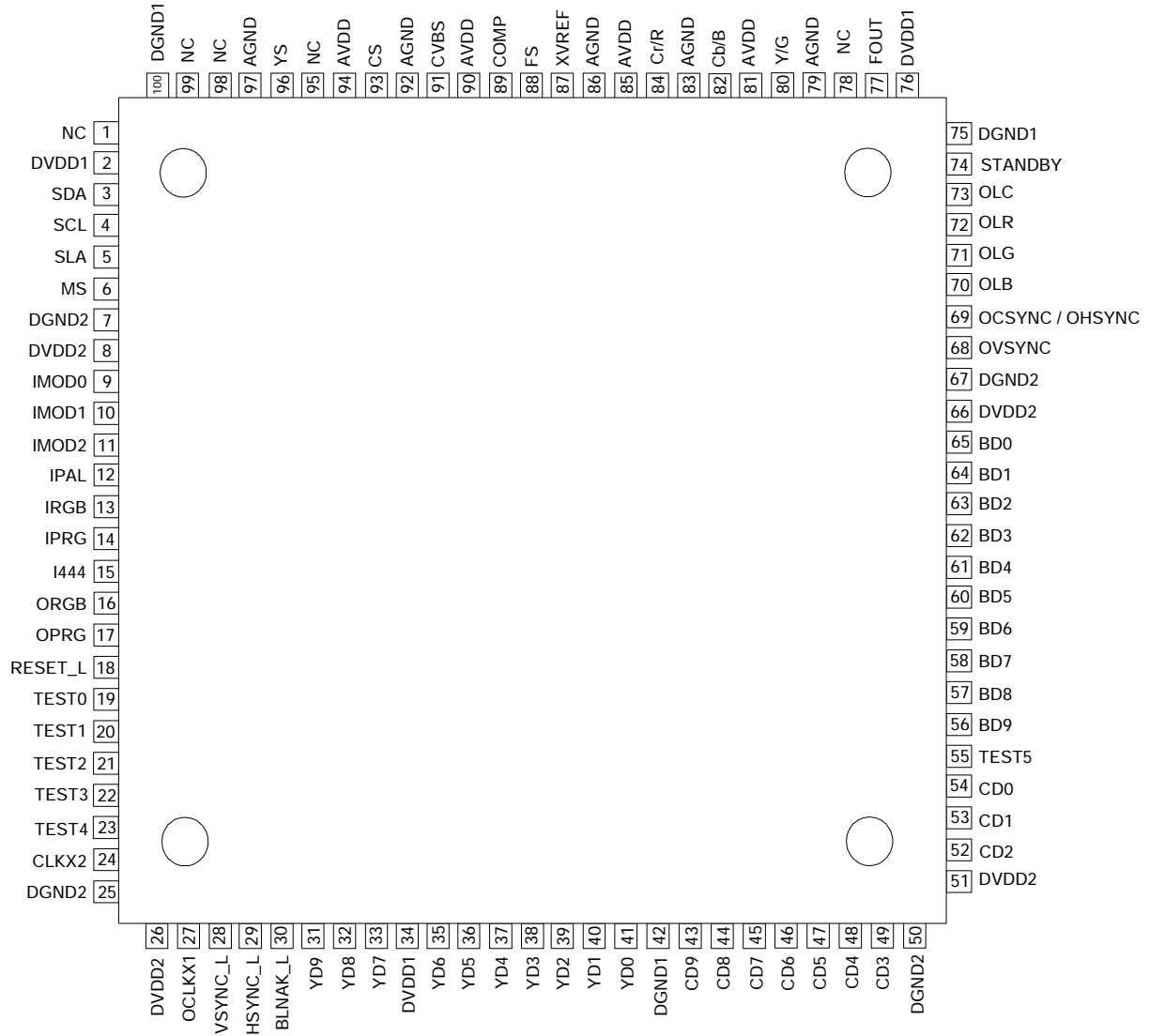
- Supported video type: NTSC/PAL
- Scanning method: Interlace/Progressive/Single-field signals
- Input data format
 - ITU-R BT.656-4 type (Y/CbCr 4:2:2 10-bit multiplexing, synchronization signal information added)
 - ITU-R BT.601 (Y/CbCr 4:2:2 20-bit non-multiplexing (Y/CbCr 4:1:1 20-bit non-multiplexing)
 - Y/CbCr 4:2:2 10-bit multiplexing, without synchronization signal
 - YCbCr 4:2:2 20-bit non-multiplexing (progressive)
 - YCbCr 4:4:4 30-bit/24-bit non-multiplexing (interlaced/progressive)
 - RGB 4:4:4 30-bit/24-bit non-multiplexing (interlaced/progressive)
- Input pixel frequency (Input double-speed clock frequency)
 - 12.272727 MHz (24.545454 MHz): NTSC Square Pixel
 - 13.5 MHz (27 MHz): NTSC/PAL ITU-R BT.601
 - 14.318182 MHz (28.636364 MHz): NTSC 4fsc
 - 14.75 MHz (29.5 MHz): PAL Square Pixel
 - 18 MHz (36 MHz): NTSC/PAL ITU-R BT.601 wide
- Output format
 - Composite (CVBS)
 - S-Video (Y/C separate signals)
 - RGB (Interlace/Progressive)
 - YCbCr component (Interlace/Progressive)
- Scan type conversion function / Color space conversion function
 - Interlace to Progressive / Progressive to Interlace
 - YCbCr to RGB / RGB to YCbCr
- Built-in 6ch 11-bit DAC: Capable of simultaneous output of composite, S-video, YCbCr or RGB
- Output load resistance: 300Ω (A video amp is required when a TV monitor is connected.)
- Master/Slave operation (Slave only for ITU-R BT.656 mode)
- Color bar output
- 3-bit title graphic input interface
- Luminance adjustment
- RGB gain adjustment
- Expanded luminance range mode
- Synchronization signal level adjustment
- CGMS/WSS information adding function
- Closed caption information adding function

- Supports Macrovision copyguard function (only available in the ML86V7656)
Conforms to version 7.1.L1 for interlace
Conforms to version 1.2 for progressive
- I2C-bus type serial interface
- Supply voltage: 3.3 V (I/O supply)/2.5 V (core supply) (SCL and SDA pins only, 5 V tolerant)
- Package: 100-pin plastic TQFP (TQFP100-P-1414-0.5-K) (ML86V7655TB/ML86V7656TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic TQFP

PIN FUNCTION

| Pin | Symbol | Type | Description |
|-----|---------|------|---|
| 1 | NC | | No connection |
| 2 | DVDD1 | | I/O power supply (3.3 V) |
| 3 | SDA | I/O | Data pin for I ² C bus (5 V tolerant pin) |
| 4 | SCL | I | Data pin for I ² C bus (5 V tolerant pin) |
| 5 | SLA | I | I ² C bus slave address least significant bit specification pin |
| 6 | MS | I | Master/slave select pin "1": Master mode "0": Slave mode |
| 7 | DGND2 | | Core digital power supply (2.5 V) |
| 8 | DVDD2 | | Core digital power supply (2.5 V) |
| 9 | IMOD0 | I | Input mode-0 control pin |
| 10 | IMOD1 | I | Input mode-1 control pin |
| 11 | IMOD2 | I | Input mode-2 control pin |
| 12 | IPAL | I | PAL/NTSC mode select pin "1": PAL, "0": NTSC |
| 13 | IRGB | I | RGB/YCbCr input select pin "1": RGB input, "0": YcbCr input |
| 14 | IPRG | I | Progressive/interlaced input select pin "1": Progressive input, "0": Interlaced input |
| 15 | I444 | I | 4:2:2/4:4:4 select pin "1": 4:4:4 input, "0": 4:2:2 input |
| 16 | ORGB | I | RGB/YCbCr output select pin "1": RGB output, "0": YcbCr output |
| 17 | OPRG | I | Progressive output/interlaced output select pin "1": Progressive output, "0": /Interlaced output |
| 18 | RESET_L | I | System reset pin. Reset at a "L" level. |
| 19 | TEST0 | I | Test mode control 0. Tie this pin to GND. |
| 20 | TEST1 | I | Test mode control 1. Tie this pin to GND. |
| 21 | TEST2 | I | Test mode control 2. Tie this pin to GND. |
| 22 | TEST3 | I | Test mode control 3. Tie this pin to GND. |
| 23 | TEST4 | I | Test mode control 4. Tie this pin to GND. |
| 24 | CLKX2 | I | System clock input pin |
| 25 | DGND2 | | Core digital GND |
| 26 | DVDD2 | | Core digital power supply (2.5 V) |
| 27 | OCLKX1 | O | CLKX1 output pin Outputs 1/2-divided frequency of CLKX2 |
| 28 | VSYNC_L | I/O | Vertical sync signal input-output pin When in master mode: output; when in slave mode: input |
| 29 | HSYNC_L | I/O | Horizontal sync signal input-output pin When in master mode: output; when in slave mode: input |
| 30 | BLANK_L | I/O | BLANK signal input-output pin When in master mode: output; when in slave mode: input |
| 31 | YD9 | I | Video signal input pin; Brightness Y, G signal, bit[9] |
| 32 | YD8 | I | Video signal input pin; Brightness Y, G signal, bit[8] |
| 33 | YD7 | I | Video signal input pin; Brightness Y, G signal, bit[7] |

PIN FUNCTION (continued)

| Pin | Symbol | Type | Description |
|-----|-------------------|------|---|
| 34 | DVDD1 | | I/O power supply (3.3 V) |
| 35 | YD6 | I | Video signal input pin; brightness Y, G signal, bit[6] |
| 36 | YD5 | I | Video signal input pin; brightness Y, G signal, bit[5] |
| 37 | YD4 | I | Video signal input pin; brightness Y, G signal, bit[4] |
| 38 | YD3 | I | Video signal input pin; brightness Y, G signal, bit[3] |
| 39 | YD2 | I | Video signal input pin; brightness Y, G signal, bit[2] |
| 40 | YD1 | I | Video signal input pin; brightness Y, G signal, bit[1] |
| 41 | YD0 | I | Video signal input pin; brightness Y, G signal, bit[0] |
| 42 | DGND1 | | I/O GND |
| 43 | CD9 | I | Video signal input pin; color difference C/Cr, R signal, bit[9] |
| 44 | CD8 | I | Video signal input pin; color difference C/Cr, R signal, bit[8] |
| 45 | CD7 | I | Video signal input pin; color difference C/Cr, R signal, bit[7] |
| 46 | CD6 | I | Video signal input pin; color difference C/Cr, R signal, bit[6] |
| 47 | CD5 | I | Video signal input pin; color difference C/Cr, R signal, bit[5] |
| 48 | CD4 | I | Video signal input pin; color difference C/Cr, R signal, bit[4] |
| 49 | CD3 | I | Video signal input pin; color difference C/Cr, R signal, bit[3] |
| 50 | DGND2 | | Core digital GND |
| 51 | DVDD2 | | Core digital power supply (2.5 V) |
| 52 | CD2 | I | Video signal input pin; color difference C/Cr, R signal, bit[2] |
| 53 | CD1 | I | Video signal input pin; color difference C/Cr, R signal, bit[1] |
| 54 | CD0 | I | Video signal input pin; color difference C/Cr, R signal, bit[0] |
| 55 | TEST5 | I/O | Test pin. Tie this pin to GND. |
| 56 | BD9 | I/O | Video signal input pin; color difference Cb, B signal, bit[9] |
| 57 | BD8 | I/O | Video signal input pin; color difference Cb, B signal, bit[8] |
| 58 | BD7 | I/O | Video signal input pin; color difference Cb, B signal, bit[7] |
| 59 | BD6 | I/O | Video signal input pin; color difference Cb, B signal, bit[6] |
| 60 | BD5 | I/O | Video signal input pin; color difference Cb, B signal, bit[5] |
| 61 | BD4 | I/O | Video signal input pin; color difference Cb, B signal, bit[4] |
| 62 | BD3 | I/O | Video signal input pin; color difference Cb, B signal, bit[3] |
| 63 | BD2 | I/O | Video signal input pin; color difference Cb, B signal, bit[2] |
| 64 | BD1 | I/O | Video signal input pin; color difference Cb, B signal, bit[1] |
| 65 | BD0 | I/O | Video signal input pin; color difference Cb, B signal, bit[0] |
| 66 | DVDD2 | | Core digital power supply (2.5 V) |
| 67 | DGND2 | | Core digital GND |
| 68 | OVSYNC | O | Component vertical sync signal output |
| 69 | OCSYNC/ OHSYNC | O | Composite synchronization signal output/Component horizontal synchronization signal output Select either output with the internal register OCHSEL. |
| 70 | OLB | I | Overlay text color (blue) input pin |
| 71 | OLG | I | Overlay text color (green) input pin |
| 72 | OLR | I | Overlay text color (red) input pin |
| 73 | OLC | I | Transparency control. When set to "1", an overlay signal is displayed. Connect this pin to GND if it is not used. |
| 74 | STANDBY | I | Standby enable input pin "1": Standby, "0": Normal operation |

PIN FUNCTION (continued)

| Pin | Symbol | Type | Description |
|-----|--------|------|--|
| 75 | DGND1 | | I/O GND |
| 76 | DVDD1 | | I/O power supply (3.3 V) |
| 77 | FOUT | O | Field information signal output pin |
| 78 | NC | | No connection |
| 79 | AGND | | Analog GND |
| 80 | Y/G | O | Y/G output pin |
| 81 | AVDD | | Analog power supply |
| 82 | Cb/B | O | Cb/B output pin |
| 83 | AGND | | Analog GND |
| 84 | Cr/R | O | Cr/B output pin |
| 85 | AVDD | | Analog power supply |
| 86 | AGND | | Analog GND |
| 87 | XVREF | I/O | Reference voltage input pin |
| 88 | FS | I | Video output full-scale adjustment pin |
| 89 | COMP | O | Internal reference voltage output pin |
| 90 | AVDD | | Analog power supply |
| 91 | CVBS | O | Composite signal output pin |
| 92 | AGND | | Analog GND |
| 93 | CS | O | Separate C signal output pin |
| 94 | AVDD | | Analog power supply |
| 95 | NC | | No connection |
| 96 | YS | O | Separate Y signal output pin |
| 97 | AGND | | Analog GND |
| 98 | NC | | No connection |
| 99 | NC | | No connection |
| 100 | DGND1 | | I/O GND |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------|------------------|-----------|------------------|------|
| Power supply voltage (I/O) | VDD1 | Ta = 25°C | -0.3 V to +4.6 V | V |
| Power supply voltage (Core) | VDD2 | Ta = 25°C | -0.3 V to +3.6 V | V |
| Power supply voltage (Analog) | AVDD | Ta = 25°C | -0.3 V to +4.6 V | V |
| Input voltage | V _I | Ta = 25°C | -0.3 V to +6.0 V | V |
| Output short-circuit current | I _{OS} | — | 50 | mA |
| Power dissipation | P _D | Ta = 25°C | 1 | W |
| Storage temperature | T _{stg} | — | -55 to +150 | °C |

Caution: Product quality may suffer if any of the absolute maximum ratings above is exceeded, even for an instant. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage. Therefore the product must be used under conditions that ensure that no absolute maximum rating will ever be exceeded.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------|--------------------|------|------|------|------|
| Power supply voltage (I/O) | VDD1 | 3.0 | 3.3 | 3.6 | V |
| Power supply voltage (Core) | VDD2 | 2.25 | 2.5 | 2.75 | V |
| Power supply voltage (Analog) | AVDD | 3.0 | 3.3 | 3.6 | V |
| Operating temperature | T _a | -40 | — | +85 | °C |
| External reference voltage | V _{refex} | — | 1.23 | — | V |
| D/A output setting resistance | R _{iadj} | 500 | 1000 | 1330 | Ω |
| D/A output load resistance | R _L | — | 300 | — | Ω |

ELECTRICAL CHARACTERISTICS

DC Characteristics 1

Ta = -40 to +85°C, DVDD1 = 3.3 V ±0.3 V, VDD2 = 2.5 ±0.25 V, AVDD = 3.3 V ±0.3 V,
DGND1, DGND2, AGND = 0 V

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|--------------------------------|---|------|------|---------------|------|
| "H" level input voltage 1 | V _{IH1} | — | 2.2 | — | VDD1 +0.3V | V |
| "H" level input voltage 2 | V _{IH2} ^{*1} | — | 2.2 | — | 5.5 | V |
| "L" level input voltage | V _{IL} | — | -0.3 | — | +0.8 | V |
| Voltage at Schmitt trigger threshold value | V _{T+} | — | — | — | 2.1 | V |
| Voltage at Schmitt trigger threshold value | V _{T-} | — | 0.7 | — | — | V |
| Voltage at Schmitt trigger hysteresis value | V _H | — | — | 0.4 | — | V |
| "H" level output voltage | V _{OH} | I _{OH} = -4 mA | 2.4 | — | — | V |
| "L" level output voltage | V _{OL} | I _{OL} = 4 mA | — | — | 0.4 | V |
| Input leakage current | I _{LI} | V _{IN} = VDD1 or GND1 | -10 | — | +10 | μA |
| "H" level input current (pull-down resistance) | I _{IH} | V _{IN} = VDD1 | 20 | — | 250 | μA |
| Output leakage current | I _{LO} | V _{OUT} = VDD1 or GND1 | -10 | — | +10 | μA |
| Power supply current (during operation) | I _{DD1} | CLKX2 = 36 MHz, R _L = 300Ω | — | — | 160 | mA |
| Power supply current (when stopped 1) | I _{DDs1} | CLKX2 = 0 MHz, V _{IN} = V _{IL} | — | — | 45 | mA |
| Power supply current (when stopped 2) | I _{DDs2} | CLKX2 = 0 MHz, V _{IN} = V _{IL} STANDBY = V _{IH} | — | — | 5 | mA |

*1: VIH2 is applied to the SDA and SCL pins only.

Note: The power supply current does not include the current consumption of the output buffer (no load).

DC Characteristics 2

Ta = -40 to +85°C, DVDD1 = 3.3 V ±0.3 V, VDD2 = 2.5 ±0.25 V, AVDD = 3.3 V ±0.3 V,
DGND1, DGND2, AGND = 0 V

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------|-----------|-------|------|-------|------|
| DAC internal reference voltage | V _{REFIN} | — | 1.187 | 1.23 | 1.313 | V |
| DAC integral linearity | SINL | — | — | ±4 | — | LSB |
| DAC differential linearity | SDNL | — | — | ±2 | — | LSB |

AC Characteristics

Ta = -40 to +85°C, DVDD1 = 3.3 V ±0.3 V, VDD2 = 2.5 ±0.25 V, AVDD = 3.3 V ±0.3 V,
DGND1, DGND2, AGND = 0 V

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------------|--------------------|---------------------------|------|-----------|------|------|
| Clock frequency (CLKX2 frequency) | F _{CLK} | NTSC square pixel | — | 24.545454 | — | MHz |
| | | PAL square pixel | — | 29.5 | — | MHz |
| | | NTSC 4Fsc | — | 28.636364 | — | MHz |
| | | NTSC/PAL ITU-R BT601 | — | 27 | — | MHz |
| | | NTSC/PAL ITU-R BT601 wide | — | 36 | — | MHz |
| Clock duty ratio | dt _{CLK} | — | 45 | — | 55 | % |
| Input data setup time | t _{SI} | — | 6 | — | — | ns |
| Input data hold time | t _{HI} | — | 5 | — | — | ns |
| Output delay time | t _{OD} | C _L = 20 pF | — | — | 18 | ns |
| Reset pulse time | t _{RSTP} | — | 100 | — | — | ns |
| I ² C clock cycle time | t _{CCI2C} | Rpull_up = 4.7 kΩ | 10 | — | — | μs |
| I ² C clock "H" level time | t _{HI2C} | Rpull_up = 4.7 kΩ | 4 | — | — | μs |
| I ² C clock "L" level time | t _{LI2C} | Rpull_up = 4.7 kΩ | 4.7 | — | — | μs |
| I ² C data setup time | t _{DSI2C} | Rpull_up = 4.7 kΩ | 250 | — | — | ns |
| I ² C data hold time | t _{DHI2C} | Rpull_up = 4.7 kΩ | 0 | — | 3.45 | μs |

POWER-ON SEQUENCE

Turn on the power supplies in the following order: DVDD1 → AVDD → DVDD2. Turn them off in the reverse order. After every power supply reaches its specified voltage and the clock CLKX2 is stabilized, input the reset signal.

RESET INPUT TIMING

Input the reset signal for the reset pulse time t_{RSTP} .

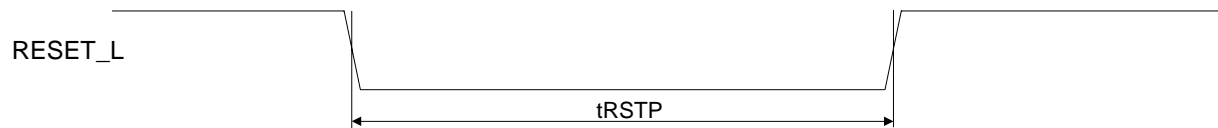


Figure 1 Reset Signal Input Timing

I²C INTERFACE TIMING

Use the I²C interface to set the internal register values. The I²C interface is compliant with the 100 kHz (SCL frequency) standard mode. Figure 2 shows the basic timing. Make sure that the SDA value does not change while SCL is at a “H” level. For information on timing parameter values refer to the AC characteristics.

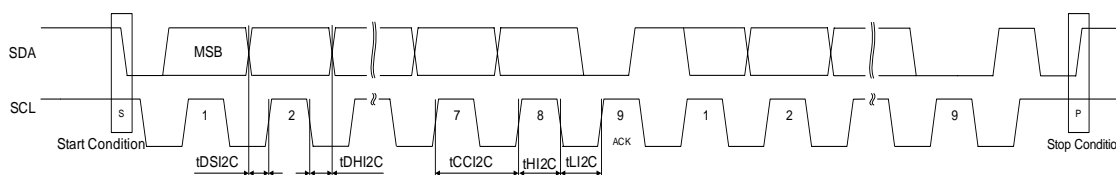


Figure 2 I²C Interface Basic Timing

Figures 3 and 4 show the I²C interface input format.

Write format

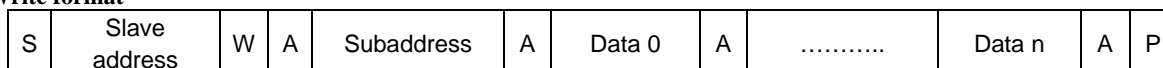


Figure 3 Write Format

Write data to the specified subaddress register. If multiple data items are written in succession, the subaddress is incremented automatically for each data item.

Read format

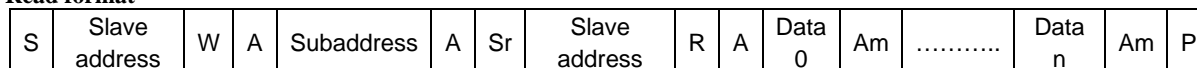


Figure 4 Read Format

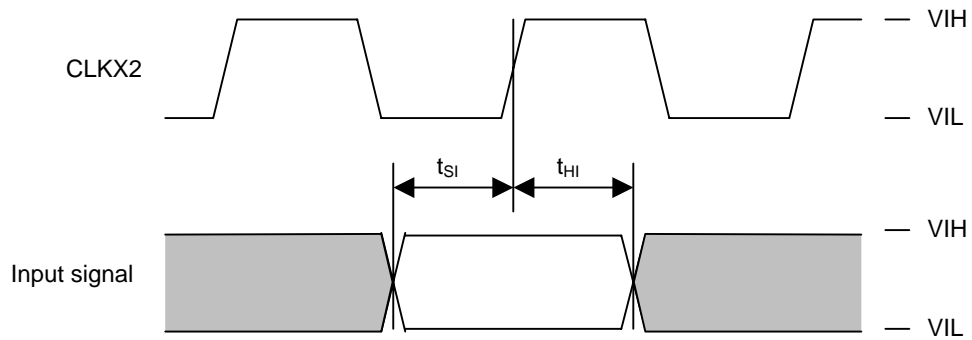
Read data of the register at the specified subaddress. If multiple data items are written in succession, the subaddress is incremented automatically for each data item.

Table 1 Symbols Used in the Input Formats

| Symbol | Meaning |
|---------------|---|
| S | Start condition |
| Sr | Restart condition |
| Slave address | Slave address “100_010X” Specify X from the SLA pin (“1” or “0”) |
| W | Write |
| R | Read |
| A | Acknowledge (slave) |
| Am | Acknowledge (master) |
| Sub address | Subaddress |
| Data n | Write and read data at subaddress |
| P | Stop condition |

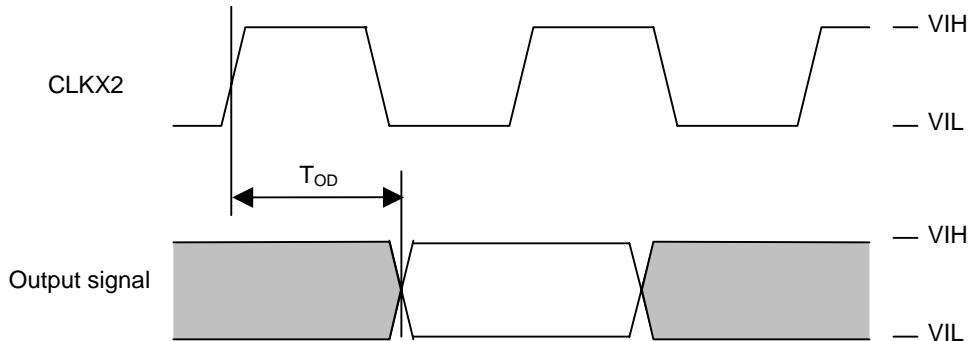
INPUT-OUTPUT TIMING

(1) Input timing



Input signal: VSYNC_L, HSYNC_L, BLANK_L, IMOD0 to 3, IPAL, IRGB, IPRG, I444, ORGB, OPRG, MS, YD, CD, BD OLC, OLR, OLG, OLB

(2) Output timing



Output signal: VSYNC_L, HSYNC_L, BLANK_L, OVSYNC, OCSYNC/OHSYNC, FOUT, OCLKX1
 (VSYNC_L, HSYNC_L, and BLANK_L are configured as output pins in master mode.)

DESCRIPTION OF FUNCTIONAL BLOCKS

This section describes the functions of the blocks shown in the Block Diagram. For a detailed explanation of all the functions, refer to the User's Manual.

- (1) **Input Data Decoder**
 Converts the video data format based on the format of the digitally input video data. ITU BT.656, 20-bit 4:2:2 YCbCr, and 10-bit 4:2:2 YCbCr input data are converted to 4:4:4 YCbCr data. When ITU BT.656 is input, the synchronization information is separated from the SAV and EAV information to generate a synchronization signal. RGB input data is output to the next block.
 The input video signal limiter function clips the input video signal at the quantization level (64–940) specified by ITU-R BT601. In the extended luminance range mode, the limiter function clips the input video signal at the quantization level (4–1016).
- (2) **Overlay & Color Bar Controller**
 A 3-bit title graphic and color bar are generated. The 3-bit title graphic becomes effective when the OLC pin is set to "H". The RGB graphic data input from the OLR, OLG and OLB pins can be replaced with input video data in pixel units. The input video data supports YCbCr input, RGB input, interlaced input and progressive input. With this function, letters can be displayed on the screen, as with the OSD function. The built-in color bar becomes effective by setting the internal register value. The color bar is a color bar with a luminance order (25%, 50%, 75% and 100%). It supports NTSC, PAL and YCbCr, RGB, CVBS, S-Video, interlaced and progressive.
- (3) **Progressive to Interlace**
 Converts progressive video data (YCbCr, RGB) to interlaced video data. Progressive video data to be input supports YCbCr (4:2:2 and 4:4:4) and RGB.
- (4) **Interlace to Progressive**
 Converts interlaced video data (YCbCr, RGB) to progressive video data.
- (5) **RGB to YCbCr/YCbCr to RGB**
 Converts RGB/YCbCr data to YCbCr/RGB data.
- (6) **Y/RGB Level Adjustment**
 This block adjusts the levels of the luminance signal Y, RGB data. The luminance signal level can be adjusted in 16 steps (78.125% to 125%, in increments of 3.125%) by setting the internal register value. RGB data gain can be set from 0.0 to 2.0 times by setting the internal register value. A different setting can be made for each channel of R, G, and B.
- (7) **YCbCr to YUV**
 Converts YCbCr data to YUV data.
- (8) **Sync Controller**
 This block adds a synchronization signal to the video signal, adds VBI data, and adjusts the synchronization signal level and offset of the signal.
- (9) **CGMS/WSS/CC Controller**
 This block generates data of CGMS-A(Copy Generation Management System - Analog), WSS (Wide Screen Signaling), and CC (Closed Caption).
- (10) **LPF**
 Removes high frequency components from video data.

- (11) Color Burst & Subcarrier Generator
These blocks generate the amplitude of the U and V components of a burst signal, and generate an color subcarrier.
- (12) 11-bit DAC
Converts digital video signals, with 11-bit resolution, to analog video signals and outputs them. The DAC output is of the current drive type. Connect an external load resistor (300 Ω) to the analog output pin. Connect a video amplifier to the output stage of the encoder to drive a 75 Ω load.
- (13) Sync Generator & Timing Controller
This block generates video synchronization signals and controls the timing of internal operations. A slave mode and a master mode are available. In the slave mode, operation is based on synchronization signals input from outside. In the master mode, operation is based on synchronization signals generated within the LSI.
- (14) I2C Interface
I²C-bus serial interface. Used to set operation modes and internal register values.

VIDEO DATA INPUT CONTROL

(1) Types of input video pixel frequencies

The ML86V7655/56 support the pixel frequencies for input video shown in Table 2. Every pixel frequency can be selected.

(Note) The input clock frequency should be double the pixel frequency.

Table 2 Types of Input Pixel Frequencies

| Pixel frequency (MHz) | | Input CLKX2 frequency (MHz) |
|-----------------------|-----------|-----------------------------|
| NTSC ITU-R BT601 | 13.5 | 27 |
| PAL ITU-R BT601 | 13.5 | 27 |
| NTSC Square Pixel | 12.272727 | 24.545454 |
| NTSC 4Fsc | 14.318182 | 28.63634 |
| PAL Square Pixel | 14.75 | 29.5 |
| NTSC ITU-R BT601 Wide | 18.0 | 36 |
| PAL ITU-R BT601 Wide | 18.0 | 36 |

(2) Input data formats for interlaced and progressive scanning

Table 3 shows the scanning method (interlaced/progressive) and data type.

Table 3 Types of Input Data Formats

| Input data format | | | Data input pin |
|-------------------|-----------|------------------------------------|----------------|
| Scanning method | Data type | Sampling rate for color difference | |
| Interlaced | YCbCr | 4:2:2 or 4:1:1 *1 | YD/CD or YD *2 |
| Interlaced | YCbCr | 4:4:4 | YD/CD/BD |
| Interlaced | RGB | 4:4:4 | YD/CD/BD |
| Progressive | YCbCr | 4:2:2 | YD/CD |
| Progressive | YCbCr | 4:4:4 | YD/CD/BD |
| Progressive | RGB | 4:4:4 | YD/CD/BD |

*1 : Change internal register value to select 4:2:2 or 4:1:1.

*2 : Use only the YD pin for video data/synchronized information multiplexing input (e.g., ITU-R BT-656).

Table 4 shows the available scanning methods for NTSC and PAL.

Table 4 Scanning Methods

| Scanning method | No. of lines | Frequency |
|------------------|--------------|-----------|
| NTSC interlaced | 262.5 | 60 Hz |
| NTSC progressive | 525 | 60 Hz |
| PAL interlaced | 312.5 | 50 Hz |
| PAL progressive | 625 | 50 Hz |

(3) Video data/synchronization information multiplexing input format types

The ML86V7655/56 support the video data/synchronization information multiplexing input interfaces and data multiplexing (no multiplexing for sync signals) input interfaces shown in Table 5.

Table 5 Types of Multiplexed Input Interfaces

| Input interface | Input CLKX2 frequency (MHz) | Data input pin |
|--|-----------------------------|----------------|
| NTSC ITU-R BT656 style(*1) | 27 | YD |
| PAL ITU-R BT656 style(*1) | 27 | YD |
| NTSC 4:2:2 10-bit multiplexing (no multiplexing for sync signals)(*2) | 27 | YD |
| NTSC Square Pixel 4:2:2 10-bit multiplexing (no multiplexing for sync signals)(*2) | 24.545454 | YD |
| NTSC 4Fsc 4:2:2 10-bit multiplexing (no multiplexing for sync signals)(*2) | 28.63634 | YD |
| PAL 4:2:2 10-bit multiplexing (no multiplexing for sync signals)(*2) | 27 | YD |
| PAL Square Pixel 4:2:2 10-bit multiplexing (no multiplexing for sync signals)(*2) | 29.5 | YD |
| NTSC Square Pixel ITU-R BT656 style(*3) | 24.545454 | YD |
| PAL Square Pixel ITU-R BT656 style(*3) | 28.63634 | YD |
| NTSC 4FSC ITU-R BT656 style(*3) | 29.5 | YD |

*1: ITU-R BT656 style input interface. For details, refer to “Video Interface Timing” in the User’s Manual.

*2: 4:2:2 10-bit multiplexing (no multiplexing for sync signals) interface. This interface multiplexes YCbCr and inputs the data from the YD pin. Input the synchronization signal from the VSYNC_L, HSYNC_L and BLANK_L pins. For details, refer to the “Input Data Format” and “Video Interface Timing” sections in the User’s Manual.

*3: ITU-R BT656 style input interface for SquarePixel and 4FSC. This interface multiplexes video data and synchronization information and inputs the data from the YD pin. Synchronization information is multiplexed as SAV and EAV. For details, refer to the “Video Interface Timing” section in the User’s Manual.

VIDEO DATA OUTPUT CONTROL

Video signals (composite signals, separate video signals and component YCbCr/RGB signals) can be simultaneously output from the 6-channel D/A converter. Composite signals are output from the CVBS pin, and separate video signals are output from the YA and CS pins. YCbCr or RGB signals are exclusively output from the Y/G, Cb/B and Cr/R pins.

For each input data scanning method, conversion from interlaced to progressive and from progressive to interlaced is possible. Color space conversion, such as YCbCr→RGB and RGB→YcbCr, is also possible. Table 6 shows the available output formats for each input format.

For example, 4:2:2 YCbCr progressive video data can be simultaneously output in three different video formats, composite, S-Video and YCbCr interlaced.

Table 6 Correspondence of Input Formats and Output Formats

| Input format | Output format | | | | | |
|-------------------------|---------------|---------|------------------|-------------------|----------------|-----------------|
| | Composite | S-Video | YCbCr interlaced | YCbCr progressive | RGB interlaced | RGB progressive |
| 4:2:2/4:1:1 YCbCr | ○ | ○ | ○ | ○ | ○ | ○ |
| 4:4:4 YCbCr interlaced | ○ | ○ | ○ | ○ | ○ | ○ |
| 4:2:2 YCbCr progressive | ○ | ○ | ○ | ○ | ○ | ○ |
| 4:4:4 YCbCr progressive | ○ | ○ | ○ | ○ | ○ | ○ |
| RGB interlaced | ○ | ○ | ○ | ○ | ○ | ○ |
| RGB progressive | ○ | ○ | ○ | ○ | ○ | ○ |

○: Output enabled

Table 7 shows the output pins from which video data is output. Change the internal register values to enable/disable D/A converter output for each channel.

Table 7 Video Output Pins

| Output format | Pin name |
|----------------------------------|-----------------|
| Composite | CVBS |
| S-Video | YS, CS |
| YCbCr/RGB interlaced/progressive | Y/G, Cb/B, Cr/R |

INTERNAL REGISTERS

Use the I2C interface to change the internal register values. For details on register functions, refer to the User's Manual.

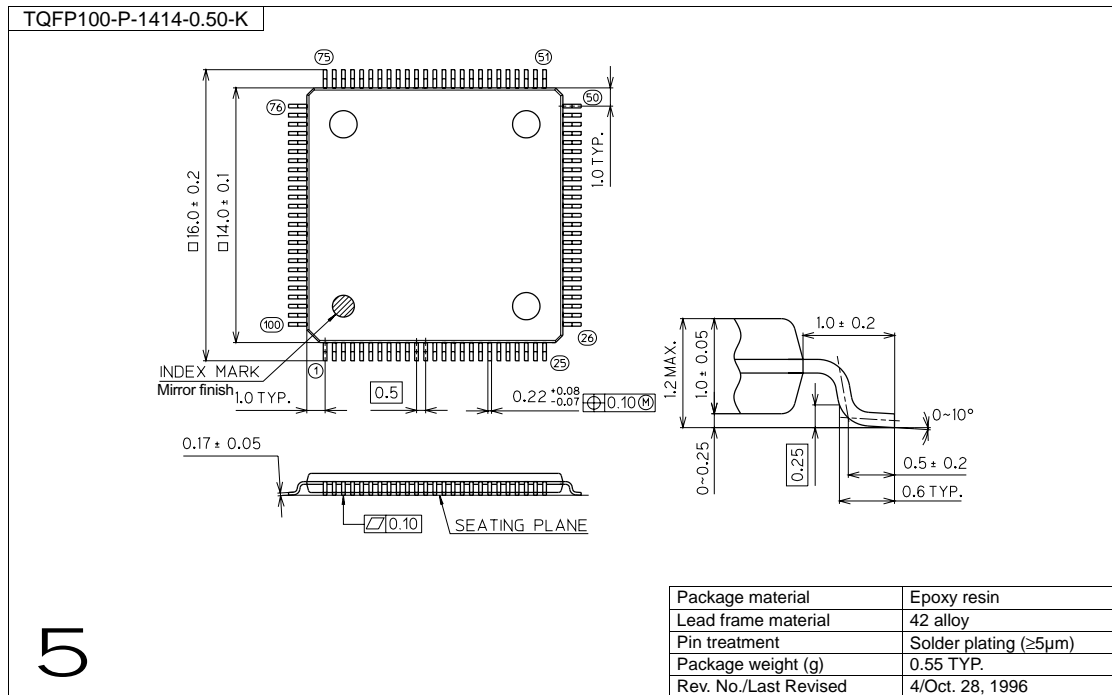
Table 8 Register Map

| Sub address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|---|---------------------|--------------|------------|-------------|---------------------|--------------|---------|
| 00 | EXTSEL | MSSEL | Reserved | | MLTDAT | IMODSEL[2:0] | | |
| 01 | Reserved | IN2S | I411 | SPL411 | NPSEL | I444SEL | IRGBSEL | IPRGSEL |
| 02 | SONSEL | LDSEL | PISEL | OFINV | OHCSEL | CSSEL | ORGBSEL | OPRGSEL |
| 03 | CBON | BBON | MCON | SBON | RGBLEV | SETUP | OUTLEV[1:0] | |
| 04 | Reserved | | | DMASK1 | Reserved | | | DMASK2 |
| 05 | Reserved | | | | | | | |
| 06 | CNTCTL | TFON | Reserved | FRUN | BLKADJ[3:0] | | | |
| 07 | Reserved | SYNCLEV1(CVBS)[2:0] | | | Reserved | SYNCLEV2(COMP)[2:0] | | |
| 08 | NOSIG | Reserved | | | LUMLEV[3:0] | | | |
| 09 | GGAIN[7:0] | | | | | | | |
| 0A | BGAIN[7:0] | | | | | | | |
| 0B | RGAIN[7:0] | | | | | | | |
| 0C | DACOFFSET[1:0] | | DACOFF[5:0] | | | | | |
| 0D | Reserved FFM | | Reserved | | | | | |
| 0E | Reserved | | | | | | | |
| 0F | Reserved - - - - - - - | | | | | | | |
| 10 | CCEN [1:0] | | Reserved | CCLN [4:0] | | | | |
| 11 | CCOD0 [7:0] | | | | | | | |
| 12 | CCOD1 [7:0] | | | | | | | |
| 13 | CCED0 [7:0] | | | | | | | |
| 14 | CCED1 [7:0] | | | | | | | |
| 15 | Reserved | | | | | | CCSTAT [1:0] | |
| 16 | CGMSEN | Reserved | WD01 [5:0] | | | | | |
| 17 | WD02 [7:0] | | | | | | | |
| 18 | CRCON | Reserved | CRCDATA[5:0] | | | | | |
| 19 | GP12 [7:0] | | | | | | | |
| 1A | WSSSEN | Reserved | GP34 [5:0] | | | | | |
| 1B to 3F | Reserved | | | | | | | |

Reserved: Reserved for the system. Do not use these registers.

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|--------------|---------------|------------------|-----------------|-----------------------|
| | | Previous Edition | Current Edition | |
| PEDL7655-000 | Sep. 14, 2004 | – | – | Preliminary edition 1 |

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