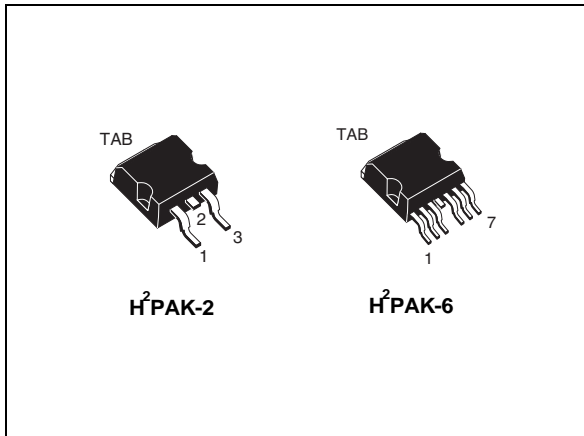


## N-channel 100 V, 1.9 mΩ typ., 180 A STripFET™ VII DeepGATE™ Power MOSFET in H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6 packages

Datasheet - production data



### Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH310N10F7-2	100 V	2.3 mΩ	180 A
STH310N10F7-6			

- Ultra low on-resistance
- 100% avalanche tested

### Applications

- Switching applications

### Description

These devices utilize the 7<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

Figure 1. Internal schematic diagram

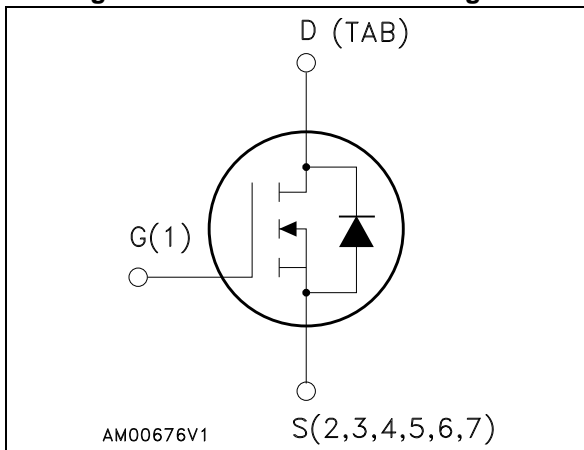


Table 1. Device summary

Order codes	Marking	Package	Packaging
STH310N10F7-2	310N10F7	H <sup>2</sup> PAK-2	Tape and reel
STH310N10F7-6		H <sup>2</sup> PAK-6	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating factor	2.1	W/°C
$E_{AS}^{(3)}$	Single pulse avalanche energy ( $T_J = 25^\circ\text{C}$ , $L=0.55\text{ mH}$ , $I_{AS}=65\text{ A}$ )	1	J
$T_j$ $T_{stg}$	Operating junction temperature storage temperature	- 55 to 175	°C

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting  $T_J=25^\circ\text{C}$ ,  $I_D=60\text{ A}$ ,  $V_{DD}=50\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2oz Cu

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\text{ V}$			1	$\mu A$
		$V_{DS} = 100\text{ V}, T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		1.9	2.3	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	12800	-	pF
$C_{oss}$	Output capacitance		-	3500	-	pF
$C_{riss}$	Reverse transfer capacitance		-	170	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}, I_D = 180\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )	-	180	-	nC
$Q_{gs}$	Gate-source charge		-	78	-	nC
$Q_{gd}$	Gate-drain charge		-	34	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}, I_D = 90\text{ A}, R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> , <a href="#">Figure 18</a> )	-	62	-	ns
$t_r$	Rise time		-	108	-	ns
$t_{d(off)}$	Turn-off delay time		-	148	-	ns
$t_f$	Fall time		-	40	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=60\text{ A}, V_{GS}=0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=180\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=80\text{ V}, T_j=150^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	85		ns
$Q_{rr}$	Reverse recovery charge		-	200		nC
$I_{RRM}$	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area.

2. Pulse duration = 300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

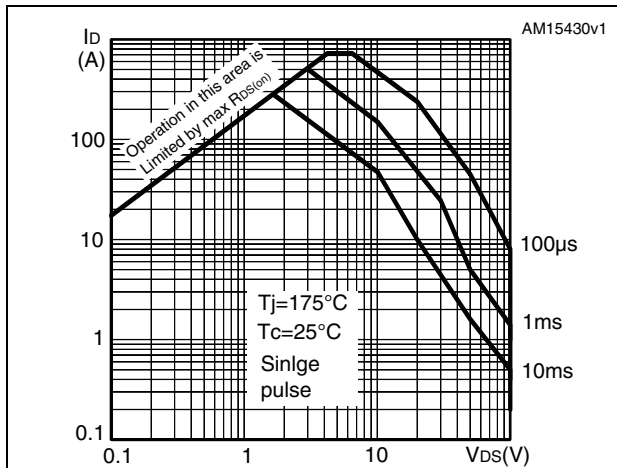


Figure 3. Thermal impedance

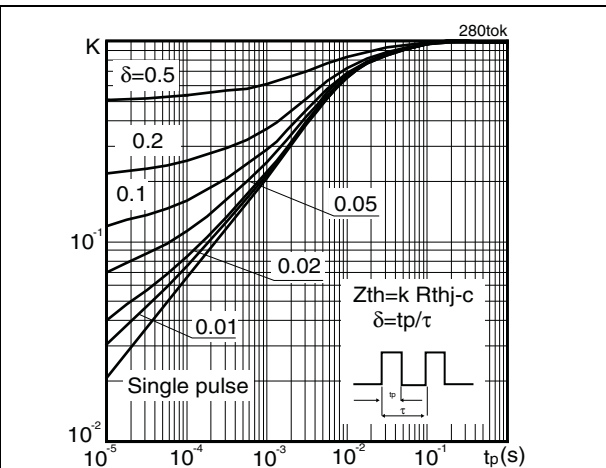


Figure 4. Output characteristics

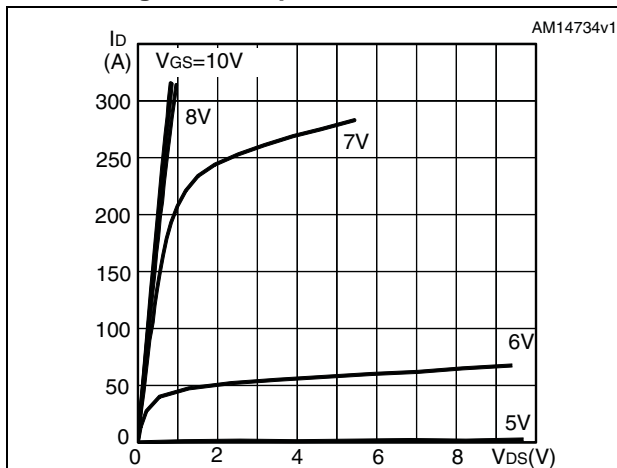


Figure 5. Transfer characteristics

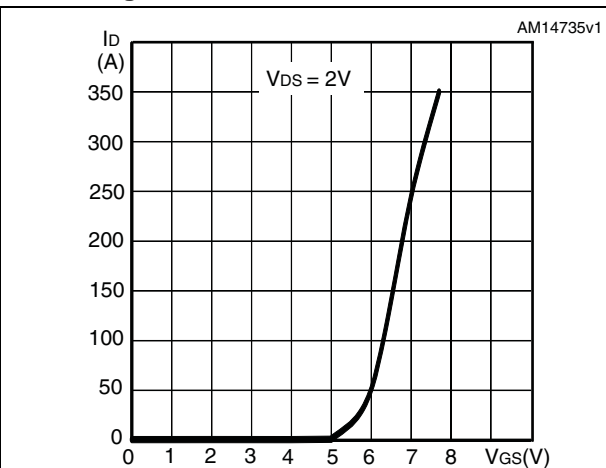


Figure 6. Gate charge vs gate-source voltage

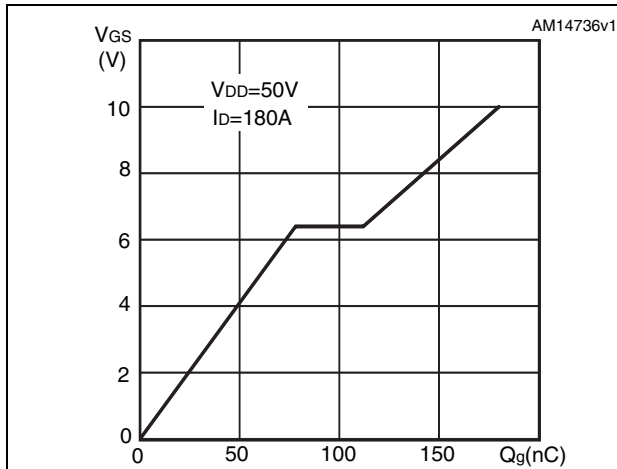


Figure 7. Static drain-source on-resistance

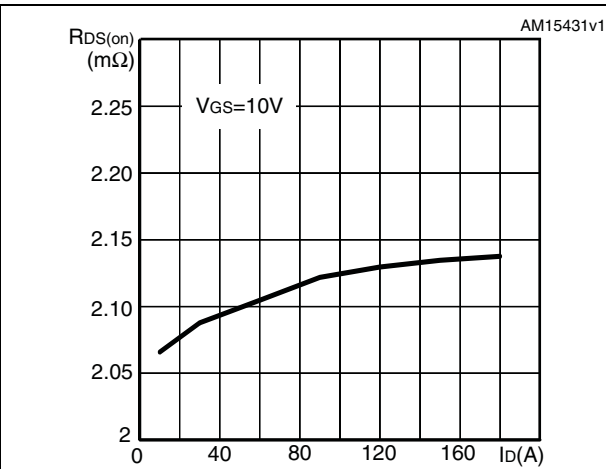


Figure 8. Normalized  $B_{VDSS}$  vs temperature

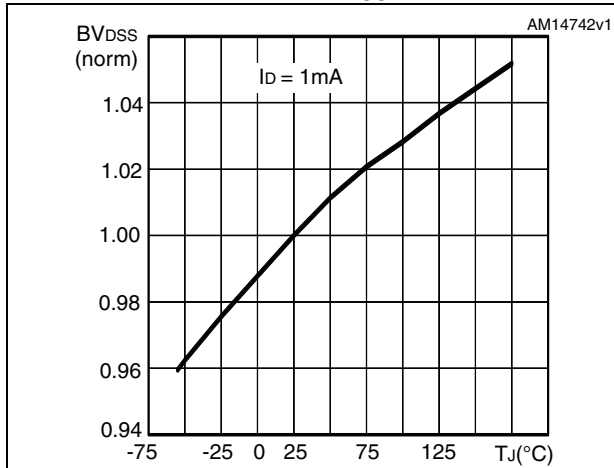


Figure 9. Capacitance variations

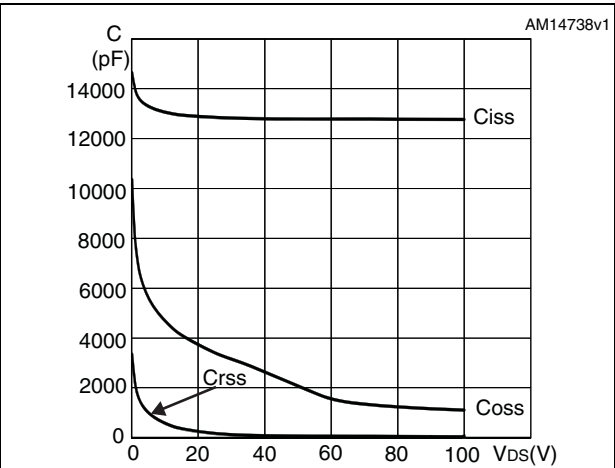


Figure 10. Source-drain diode forward characteristics

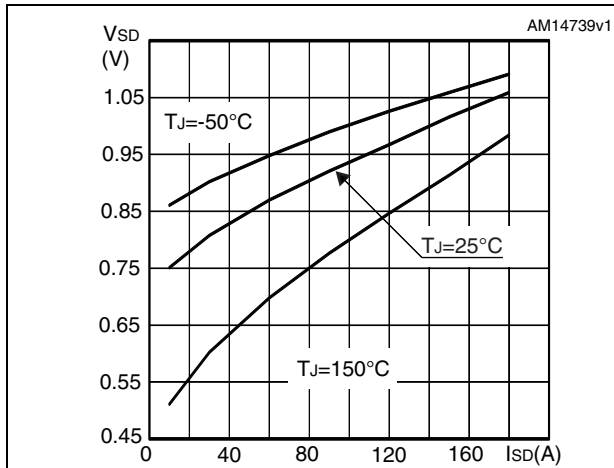


Figure 11. Normalized gate threshold voltage vs temperature

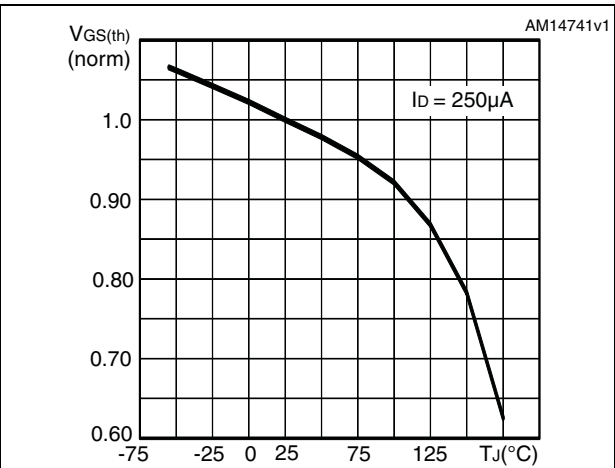
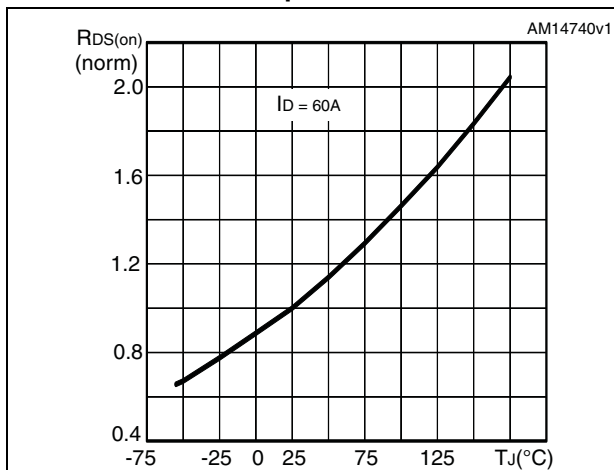


Figure 12. Normalized on-resistance vs temperature



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

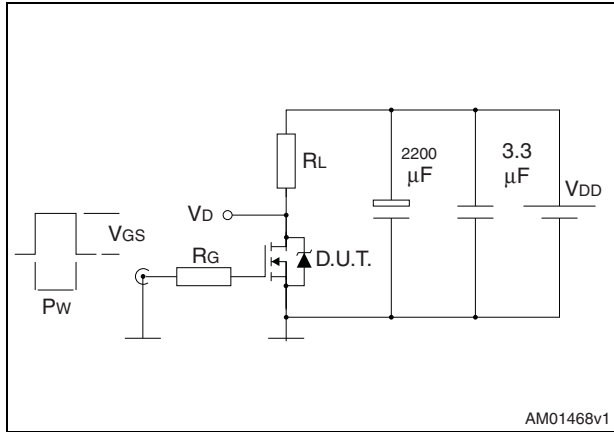


Figure 14. Gate charge test circuit

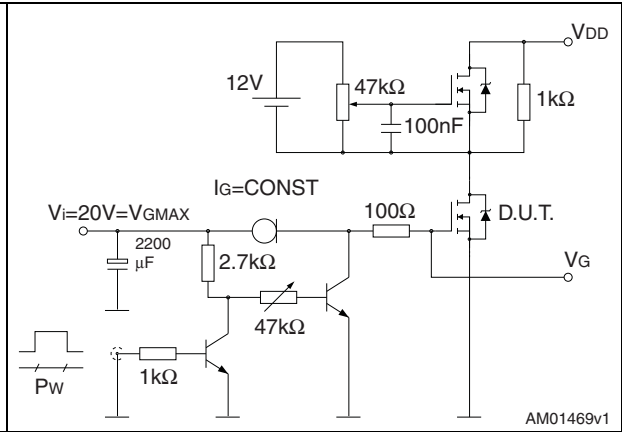


Figure 15. Test circuit for inductive load switching and diode recovery times

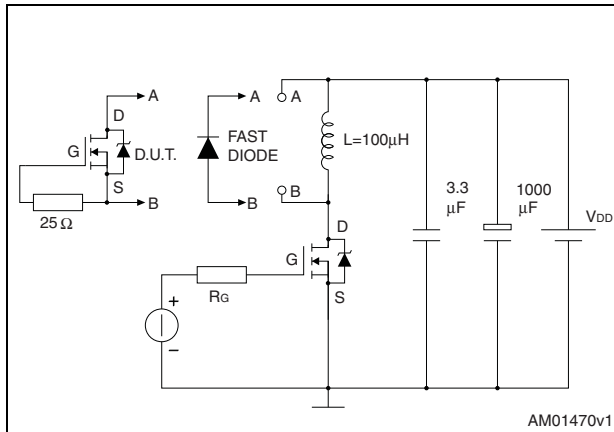


Figure 16. Unclamped inductive load test circuit

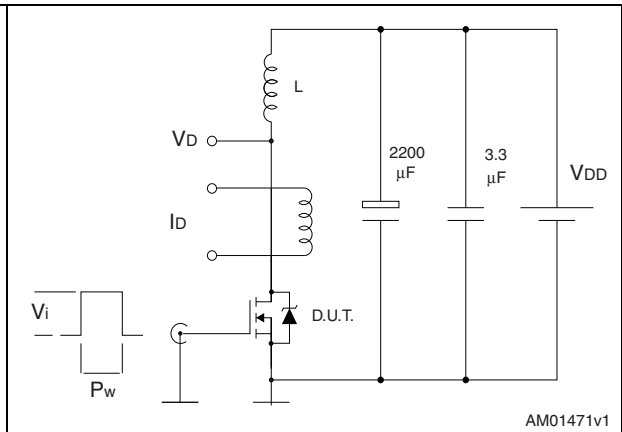


Figure 17. Unclamped inductive waveform

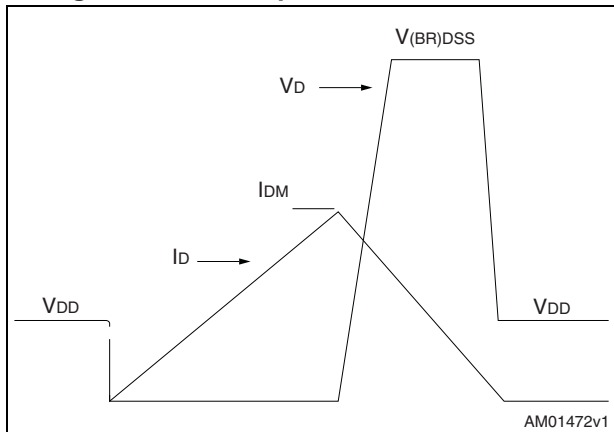
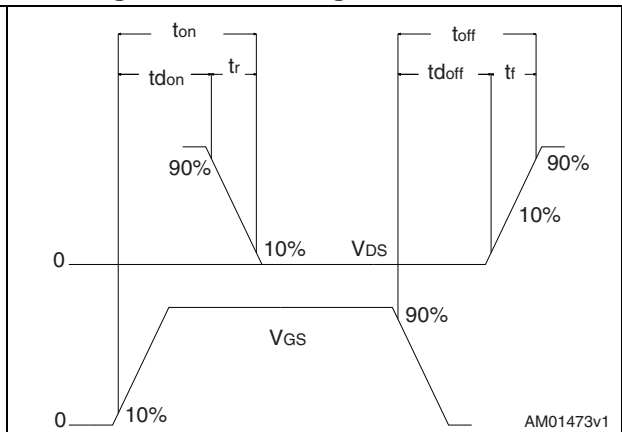


Figure 18. Switching time waveform





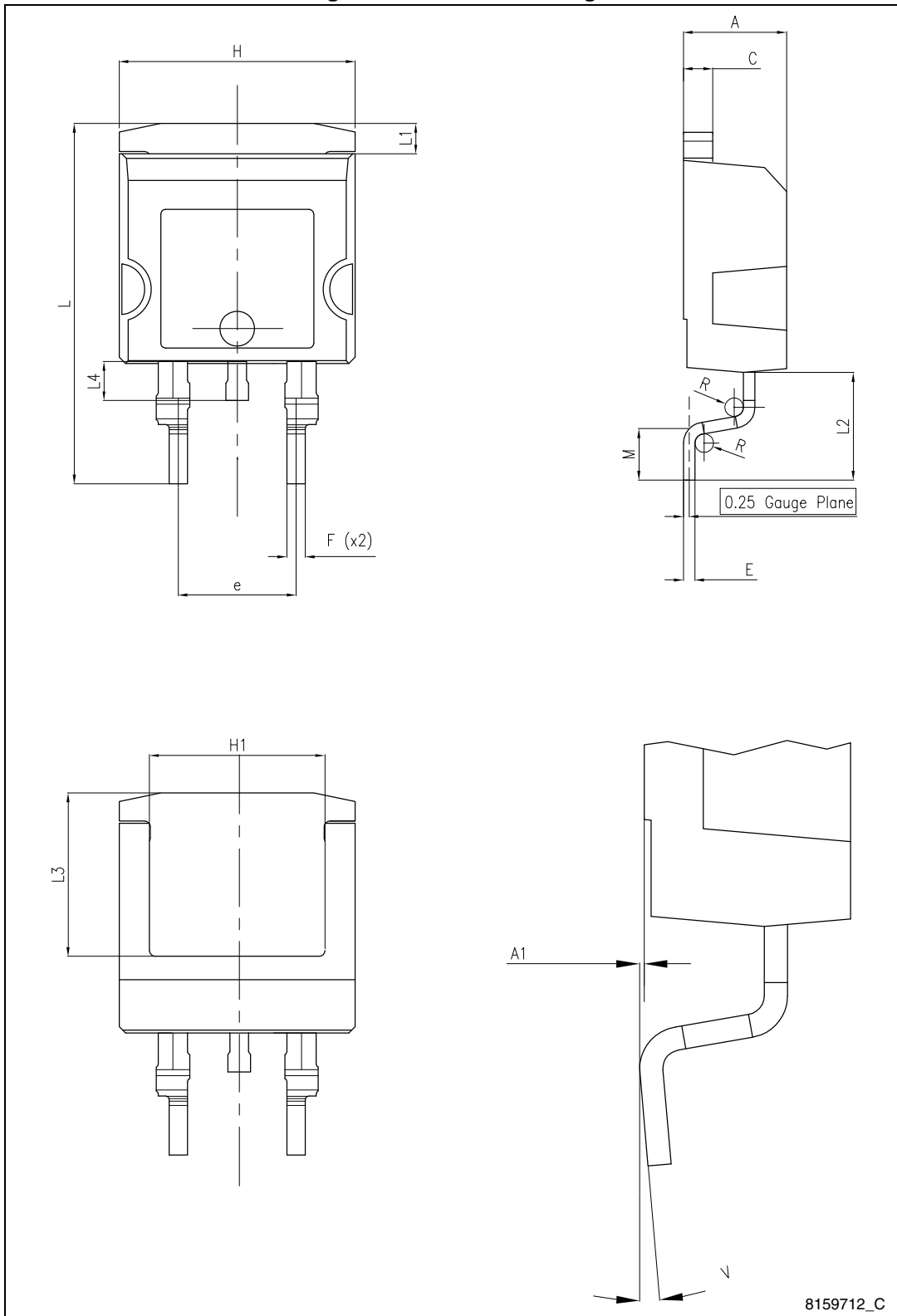
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. H<sup>2</sup>PAK-2 mechanical data

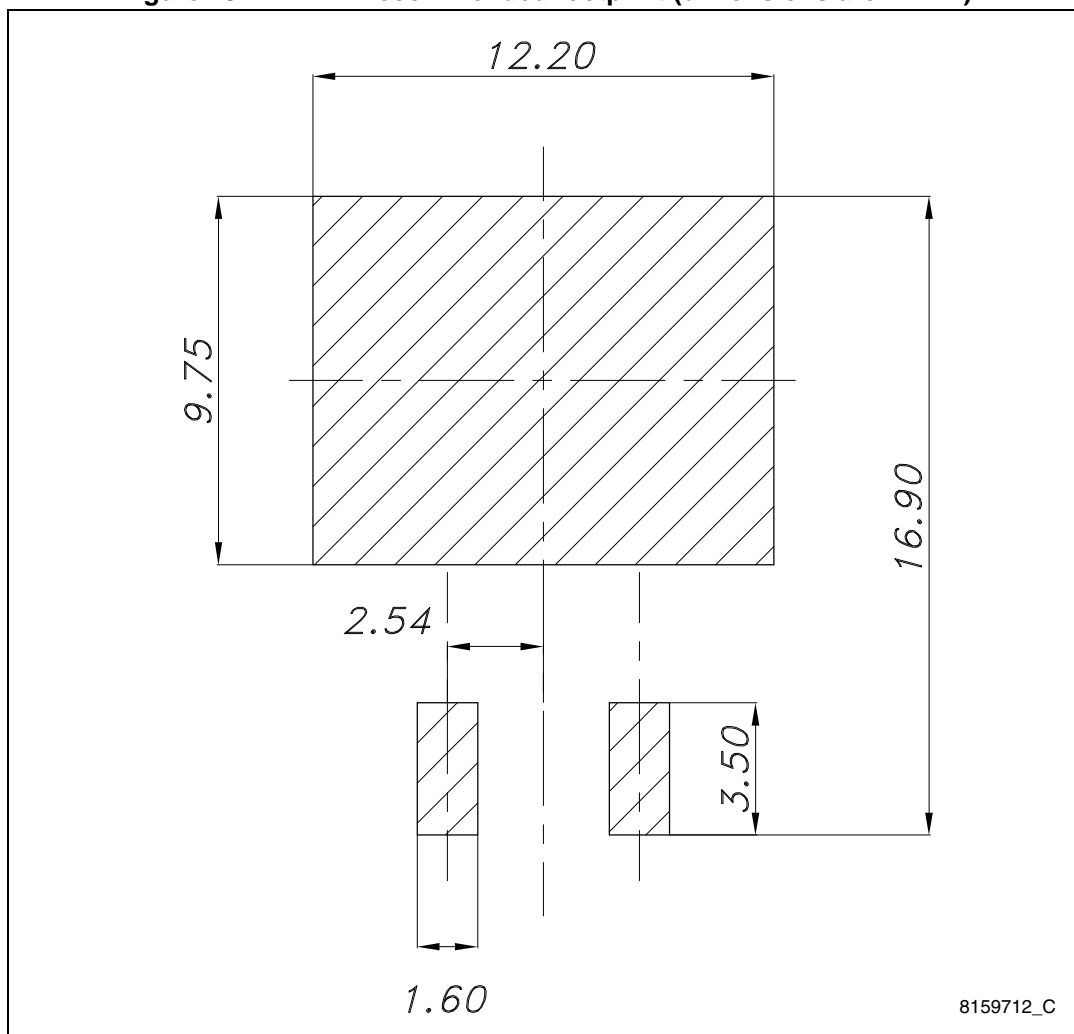
Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 19. H<sup>2</sup>PAK-2 drawing



8159712\_C

Figure 20. H<sup>2</sup>PAK-2 recommended footprint (dimensions are in mm)



8159712\_C

Table 9. H<sup>2</sup>PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 21. H<sup>2</sup>PAK-6 drawing

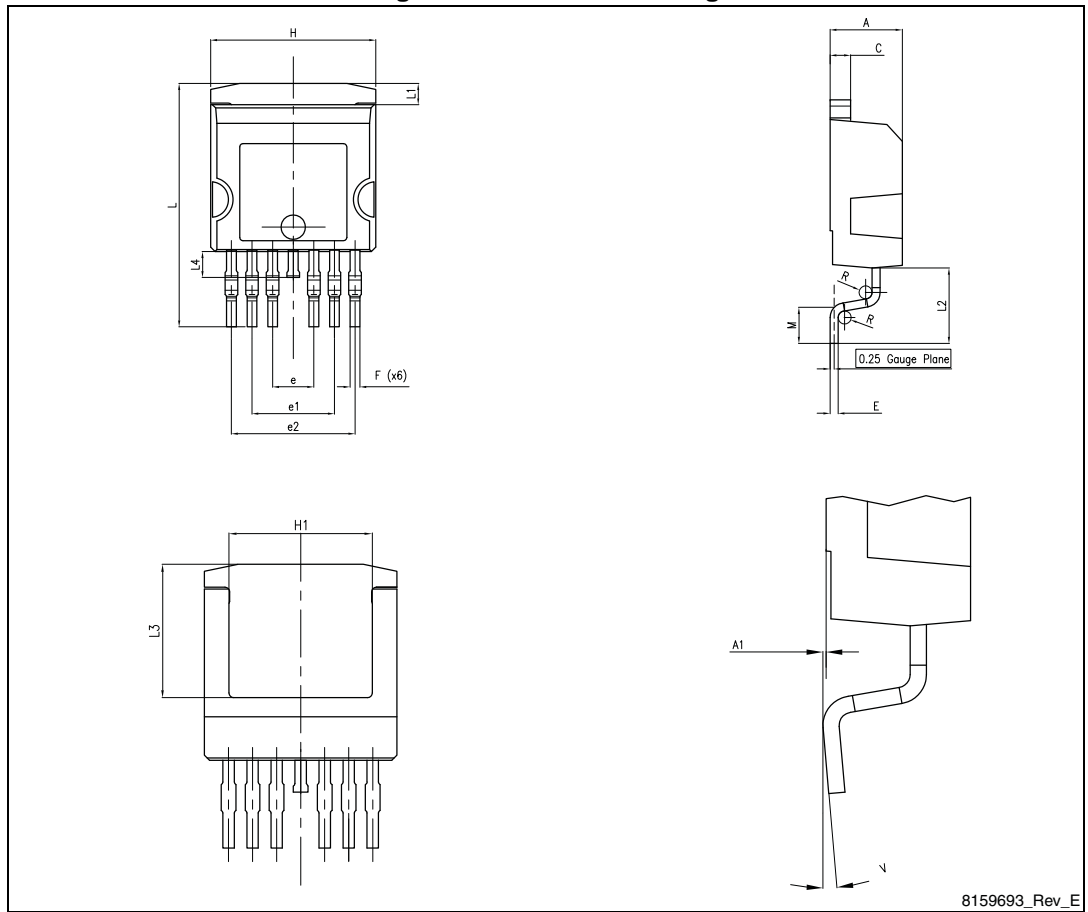
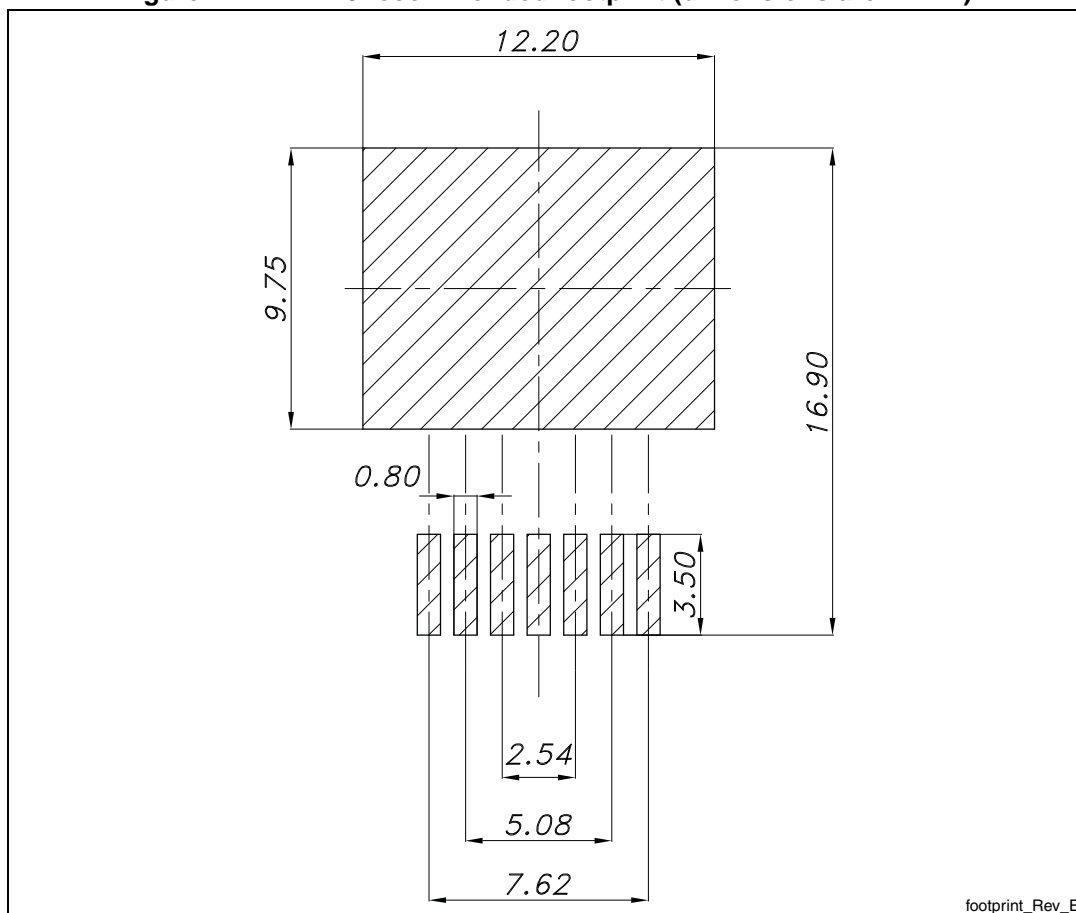


Figure 22. H<sup>2</sup>PAK-6 recommended footprint (dimensions are in mm)



## 5 Packaging mechanical data

Table 10. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			



Figure 23. Tape

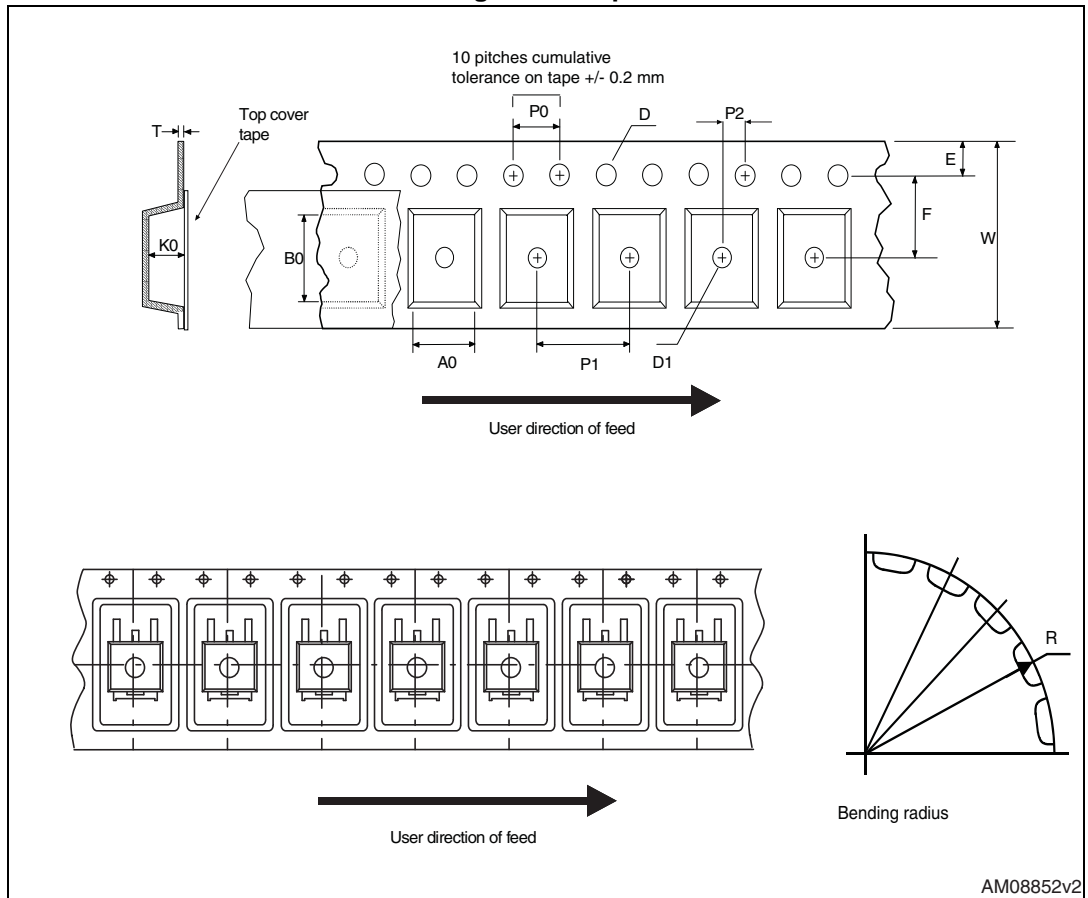
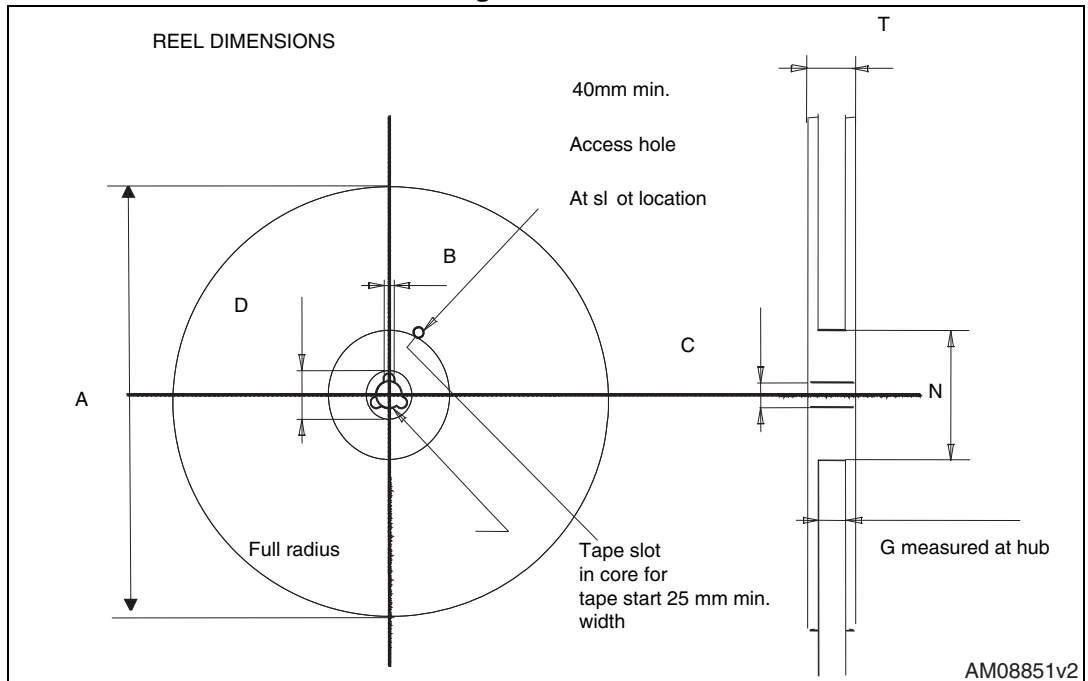


Figure 24. Reel



## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
10-Dec-2012	1	Initial release. Part number(s) previously included in datasheet ID 022287
23-Jul-2013	2	<ul style="list-style-type: none"><li>– Modified: <math>I_{DSS}</math> and <math>V_{GS(th)}</math> values on <a href="#">Table 4</a>.</li><li>– Added: <math>E_{AS}</math> value in <a href="#">Table 2</a></li><li>– Document status promoted from preliminary data to production data</li><li>– Minor text changes</li></ul>

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