POWER MOSFET TRANSISTORS

500 Volt, 0.85 Ohm
N-Channel

UFN440
UFN441
UFN442
UFN443

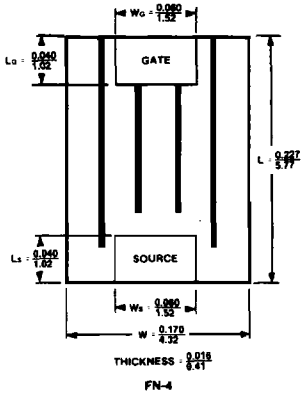
FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

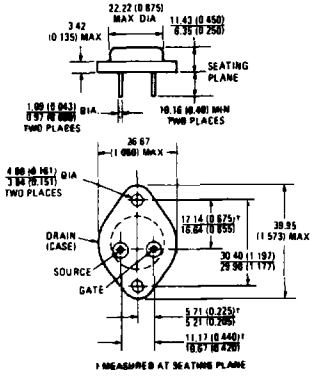


PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
UFN440	500V	0.85Ω	8.0A
UFN441	450V	0.85Ω	8.0A
UFN442	500V	1.10Ω	7.0A
UFN443	450V	1.10Ω	7.0A

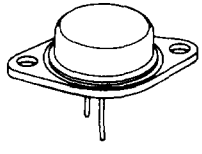
MECHANICAL SPECIFICATIONS

UFN440 UFN441 UFN442 UFN443



Dimensions in Millimeters and (Inches)

TO-204AA (TO-3)



UNITRODE

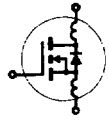
ABSOLUTE MAXIMUM RATINGS

Parameter		UFN440	UFN441	UFN442	UFN443	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	UFN440 UFN442	500	–	–	V	V_{GS} = 0V
		UFN441 UFN443	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	UFN440 UFN441	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		UFN442 UFN443	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	UFN440 UFN441	–	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		UFN442 UFN443	–	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 200V, I_D = 4.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	UFN440 UFN441	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		UFN442 UFN443	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	UFN440 UFN441	–	–	32	A	
		UFN442 UFN443	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	UFN440 UFN441	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		UFN442 UFN443	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

Fig. 1 – Typical Output Characteristics

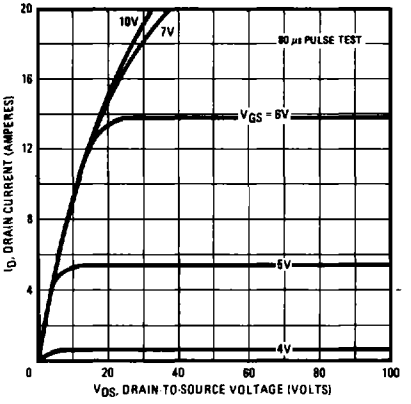

Fig. 2 – Typical Transfer Characteristics

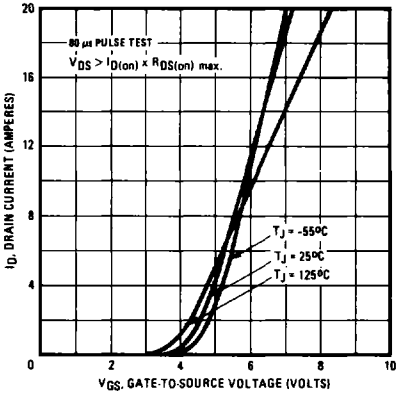

Fig. 3 – Typical Saturation Characteristics

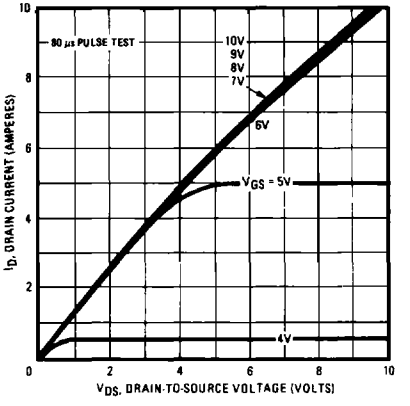

Fig. 4 – Maximum Safe Operating Area

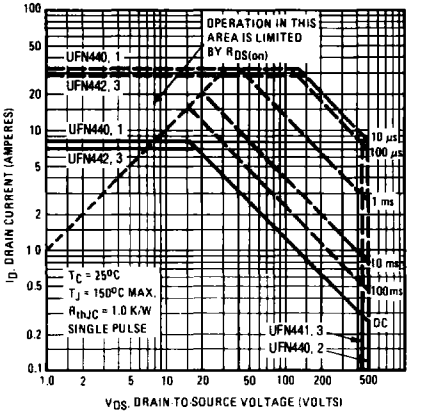

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Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

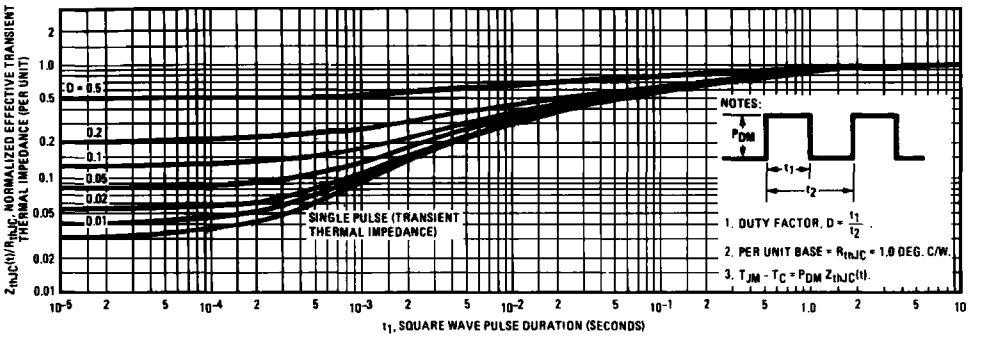

Fig. 6 – Typical Transconductance Vs. Drain Current

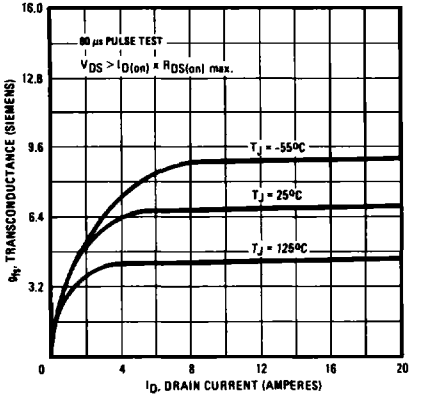

Fig. 7 – Typical Source-Drain Diode Forward Voltage

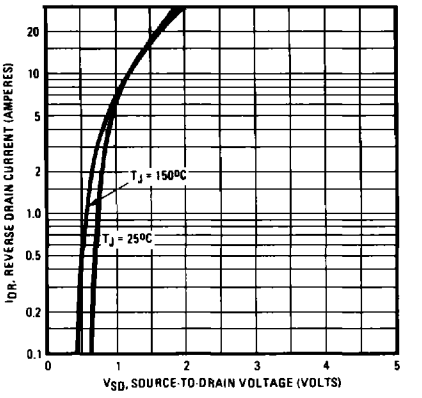

Fig. 8 – Breakdown Voltage Vs. Temperature

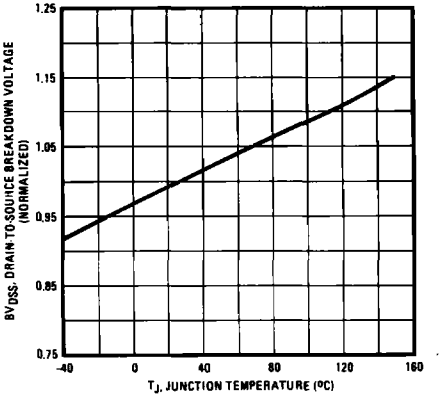

Fig. 9 – Normalized On-Resistance Vs. Temperature

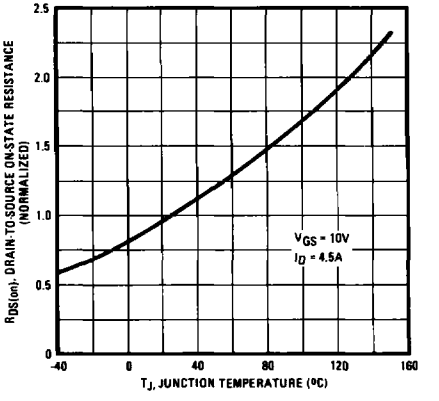

Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

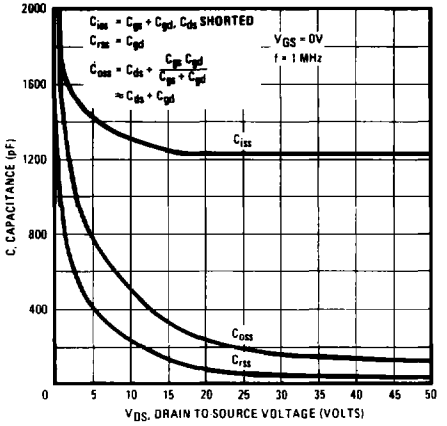

Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

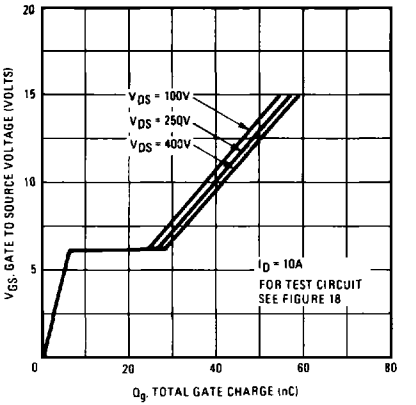

Fig. 12 – Typical On-Resistance Vs. Drain Current

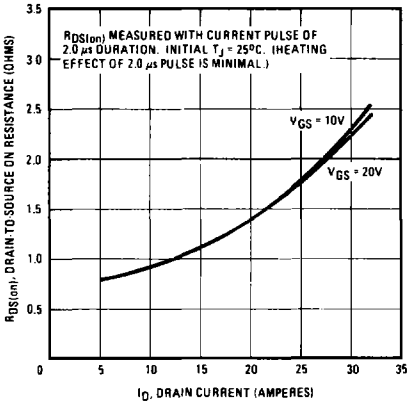

Fig. 13 – Maximum Drain Current Vs. Case Temperature

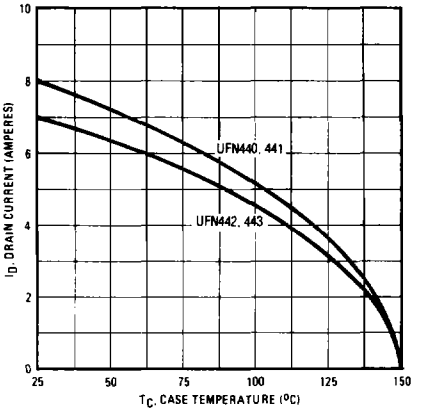

Fig. 14 – Power Vs. Temperature Derating Curve

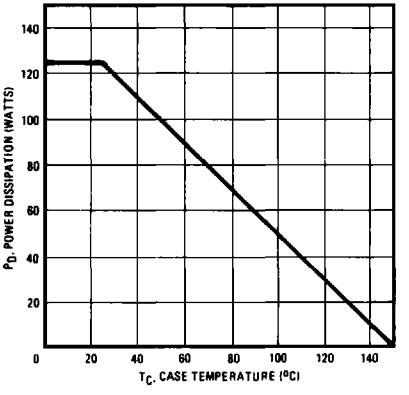

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Fig. 15 – Clamped Inductive Test Circuit

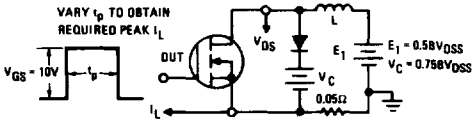

Fig. 16 – Clamped Inductive Waveforms

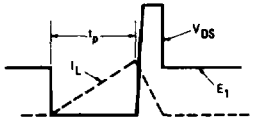

Fig. 17 – Switching Time Test Circuit

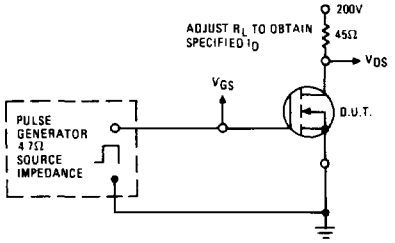

Fig. 18 – Gate Charge Test Circuit