54AC/74AC725 • 54ACT/74ACT725

512 x 9 First-In, First-Out Memory (FIFO)

Description
The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for zero fall-through time; it is suited for high-speed applications.

- **First-In, First-Out Dual Port Memory**
- **512 x 9 Organization**
- **Low Power Consumption**
- **Asynchronous and Simultaneous Read and Write**
- **Fully Expandable by Word Depth and/or Bit Width**
- **Half-Full Flag Capability in Single Device Mode**
- **Master/Slave Multiprocessing Applications**
- **Bidirectional and Rate Buffer Applications**
- **Empty and Full Warning Flags**
- **Auto Retransmit Capability**
- **Outputs Source/Sink 8 mA**
- **'ACT725 has TTL-Compatible Inputs**
- **Pin and Functionally Compatible with IDT7201**
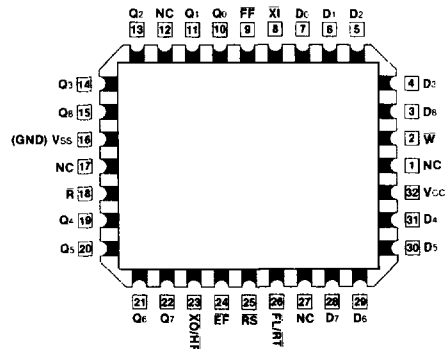- **35 MHz Read; Write-Read Capability**

Ordering Code: See Section 6

Logic Symbol
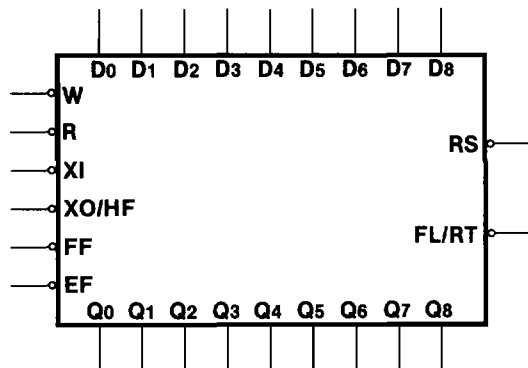
Connection Diagrams
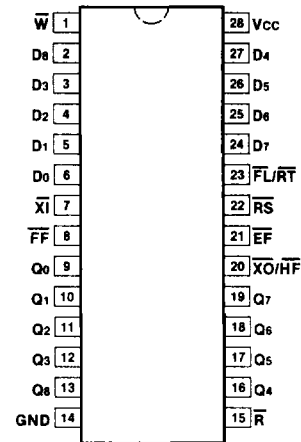
**Pin Assignment
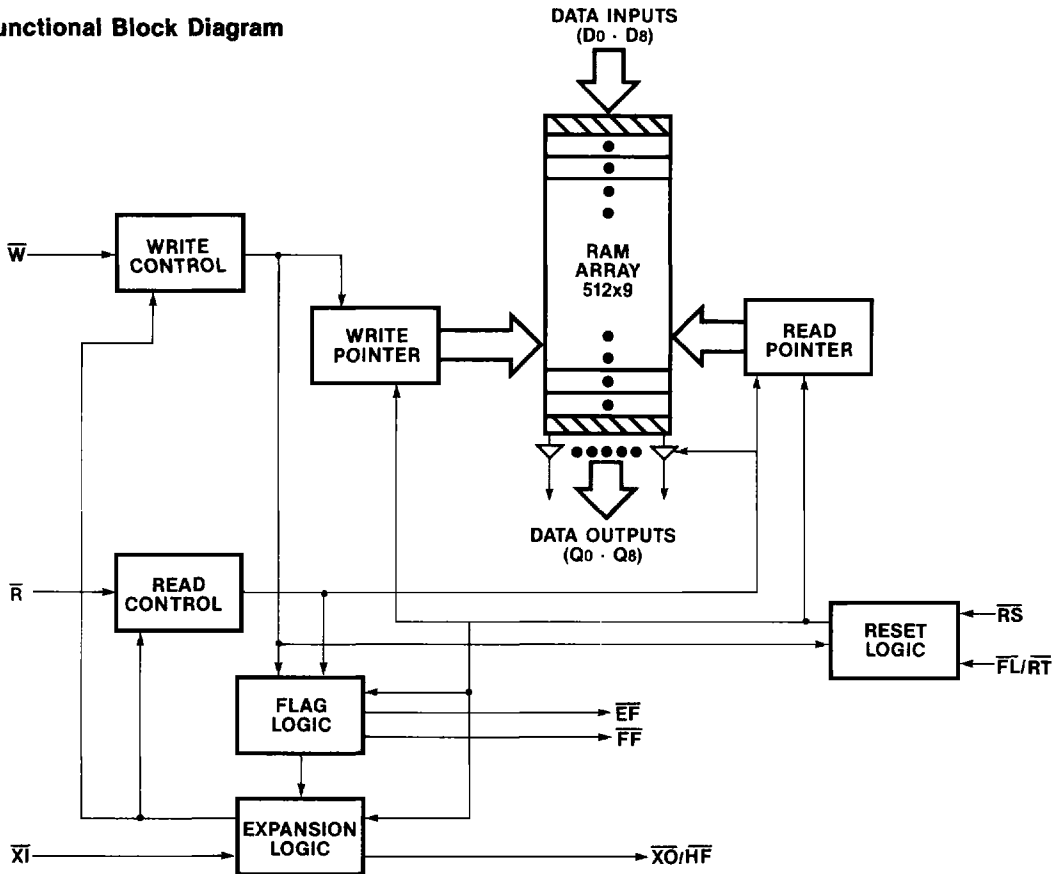for DIP, Flatpak and SOIC**

**Pin Assignment
for LCC and PCC**

Pin Names

D_0 - D_8	Data Inputs
Q_0 - Q_8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO}/HF$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit

Functional Block Diagram

Functional Description

The 'AC/'ACT725 is a dual port memory which loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow. Expansion logic allows for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins.

The device employs a 9-bit wide data array for control and parity bits which are under the control of the user. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability; the read pointer is reset to its initial position when $\overline{RT}$ is pulsed LOW to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

The 'AC/'ACT725 is ideal for those applications which require asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

AC725 • ACT725

Signal Descriptions

Inputs
Data In (D0 - D8)
Data inputs for 9-bit wide data.

Controls
Reset ($\overline{RS}$)
When the Reset ($\overline{RS}$) input is taken LOW, a reset is accomplished. During reset, both internal read and write pointers are set to the first location. A reset is required upon power up before a write operation can take place. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be HIGH during reset. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Master Reset ($\overline{RS}$).

Write Enable ($\overline{W}$)
A write cycle is initiated on the falling edge of $\overline{W}$ when a Full Flag ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When half of the memory is filled and the falling edge of the next write operation occurs, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain LOW until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. $\overline{HF}$ is then reset by the rising edge of the read operation.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, $\overline{FF}$ will go HIGH after tRFF, allowing a valid write to begin.

Read Enable ($\overline{R}$)
A read cycle is initiated on the falling edge of Read Enable ($\overline{R}$) if the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a first-in, first-out basis; it is independent of any ongoing write operations. After $\overline{R}$ goes HIGH, the data outputs (Q0 - Q8) return to a high impedance condition until the next read operation. When all data has been read from the FIFO, $\overline{EF}$ will go LOW and inhibit further read operations; the data outputs remain in a high impedance state. Upon completing a valid write operation, $\overline{EF}$ will go HIGH after tWEF, and a valid read can then begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)
This is a dual purpose output. In the multiple device mode, $\overline{FL}/\overline{RT}$ is grounded, indicating it is the first device loaded.

In the single device mode, this pin acts as the retransmit input. The single device mode is initiated by grounding the Expansion In ($\overline{XI}$).

The 'AC/'ACT725 can retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation sets the internal read pointer to the first location and will not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be HIGH during retransmit. Retransmit is useful when less than 512 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion mode; it will affect $\overline{HF}$ depending on the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)
$\overline{XI}$ is a dual purpose input. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. $\overline{XI}$ is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

Outputs
Full Flag ($\overline{FF}$)
If brought LOW, the Full Flag ($\overline{FF}$) will inhibit further write operation when the write pointer is one location from the read pointer; the device is full. If the read pointer is not moved after $\overline{RS}$, $\overline{FF}$ will go LOW after 512 writes.

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)
This is a dual purpose output. In the single device mode, when $\overline{XI}$ is grounded, $\overline{XO}/\overline{HF}$ acts as an indicator of a half-full memory.

When half of the memory is filled, on the falling edge of the next write operation, $\overline{HF}$ will be set LOW and will remain set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. $\overline{HF}$ is then reset by the rising edge of the read operation.

In the Multiple Device mode, $\overline{XI}$ is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain; $\overline{XO}/\overline{HF}$ provides a pulse to the next device when the previous device reaches the last location of memory.

Data Outputs (Q0 - Q8)
Data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever $\overline{R}$ is HIGH.

Truth Tables

Table 1: Reset and Transmit
Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location 0	Location 0	0	1	1
Retransmit	1	0	0	Location 0	Unchanged	X	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X	X

*Pointer will increment if flag is HIGH

Table 2: Reset and First Load Truth Table
Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	*	Location 0	Location 0	0	1
Reset All Other Devices	0	0	*	Location 0	Location 0	0	1
Read/Write	1	X	*	X	X	X	X

*$\overline{XI}$ is connected to $\overline{XO}$ of previous device (see Figure 12)
$\overline{RS}$ = Reset input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag output, $\overline{FF}$ = Full Flag output,
$\overline{XI}$ = Expansion input, $\overline{HF}$ = Half-Full Flag input

5

AC725 • ACT725

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C				Units	Conditions
		Typ	54AC/ACT	74AC/ACT			
			Guaranteed Limit				
IIN	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
IOZ	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
ICCQ	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
VOH	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = $-$ 8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = $-$ 8 mA, V_{CC} = 5.5 V
VOL	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
IOLD	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
IOHD	Minimum Dynamic Output Current			$-$ 32	$-$ 32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC T$_A$ = +25°C C$_L$ = 50 pF			54AC T$_A$ = −55°C to +125°C C$_L$ = 50 pF		74AC T$_A$ = −40°C to +85°C C$_L$ = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t$_A$	Access Time	3.3 5.0								ns	
t$_{RLZ}$	Read Pulse LOW to Data Bus at Low Z	3.3 5.0								ns	
t$_{WLZ}$	Write Pulse HIGH to Data Bus at Low Z	3.3 5.0								ns	
t$_{DV}$	Data Valid from Read Pulse HIGH	3.3 5.0								ns	
t$_{RHZ}$	Read Pulse HIGH to Data Bus at High Z	3.3 5.0								ns	
t$_{EFL}$	Reset to Empty Flag LOW	3.3 5.0								ns	
t$_{REF}$	Read LOW to Empty Flag LOW	3.3 5.0								ns	
t$_{RFF}$	Read HIGH to Full Flag HIGH	3.3 5.0								ns	
t$_{WEF}$	Write HIGH to Empty Flag HIGH	3.3 5.0								ns	
t$_{WFF}$	Write LOW to Full Flag LOW	3.3 5.0								ns	
t$_{WHF}$	Write LOW to Half Full Flag LOW	3.3 5.0								ns	
t$_{RHF}$	Read HIGH to Half Full Flag HIGH	3.3 5.0								ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC725 • ACT725

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC TA = +25°C CL = 50 pF	54AC TA = −55°C to +125°C CL = 50 pF	74AC TA = −40°C to +85°C CL = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
tRC	Read Cycle Time	3.3 5.0				ns	
tRR	Read Recovery Time	3.3 5.0				ns	
tRPW	Read Pulse Width	3.3 5.0				ns	
tWC	Write Cycle Time	3.3 5.0				ns	
tW	Write Pulse Width	3.3 5.0				ns	
tREC	Write Recovery Time	3.3 5.0				ns	
ts	Data Setup Time	3.3 5.0				ns	
tH	Data Hold Time	3.3 5.0				ns	
tRSC	Reset Cycle Time	3.3 5.0				ns	
tW	Reset Pulse Width	3.3 5.0				ns	
tREC	Reset Recovery Time	3.3 5.0				ns	
tRTC	Retransmit Cycle Time	3.3 5.0				ns	
tW	Retransmit Pulse Width	3.3 5.0				ns	
tREC	Retransmit Recovery Time	3.3 5.0				ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

| Symbol	Parameter	Vcc* (V)	74ACT TA = +25°C CL = 50 pF			54ACT TA = −55°C to +125°C CL = 50 pF		74ACT TA = −40°C to +85°C CL = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
tA	Access Time	5.0								ns	
tRLZ	Read Pulse LOW to Data Bus at Low Z	5.0								ns	
tWLZ	Write Pulse HIGH to Data Bus at Low Z	5.0								ns	
tDV	Data Valid from Read Pulse HIGH	5.0								ns	
tRHZ	Read Pulse HIGH to Data Bus at High Z	5.0								ns	
tEFL	Reset to Empty Flag LOW	5.0								ns	
tREF	Read LOW to Empty Flag LOW	5.0								ns	
tRFF	Read HIGH to Full Flag HIGH	5.0								ns	
tWEF	Write HIGH to Empty Flag HIGH	5.0								ns	
tWFF	Write LOW to Full Flag LOW	5.0								ns	
tWHF	Write LOW to Half Full Flag LOW	5.0								ns	
tRHF	Read HIGH to Half Full Flag HIGH	5.0								ns	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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5

AC725 • ACT725

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT TA = +25°C CL = 50 pF	54ACT TA = −55°C to +125°C CL = 50 pF	74ACT TA = −40°C to +85°C CL = 50 pF		Units	Fig. No.
			Typ	Guaranteed Minimum				
tRC	Read Cycle Time	5.0					ns	
tRR	Read Recovery Time	5.0					ns	
tRPW	Read Pulse Width	5.0					ns	
tWC	Write Cycle Time	5.0					ns	
tW	Write Pulse Width	5.0					ns	
tREC	Write Recovery Time	5.0					ns	
ts	Data Setup Time	5.0					ns	
tH	Data Hold Time	5.0					ns	
tRSC	Reset Cycle Time	5.0					ns	
tW	Reset Pulse Width	5.0					ns	
tREC	Reset Recovery Time	5.0					ns	
tRTC	Retransmit Cycle Time	5.0					ns	
tW	Retransmit Pulse Width	5.0					ns	
tREC	Retransmit Recovery Time	5.0					ns	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Figure 1

a: Typical Application — Signal Processing System
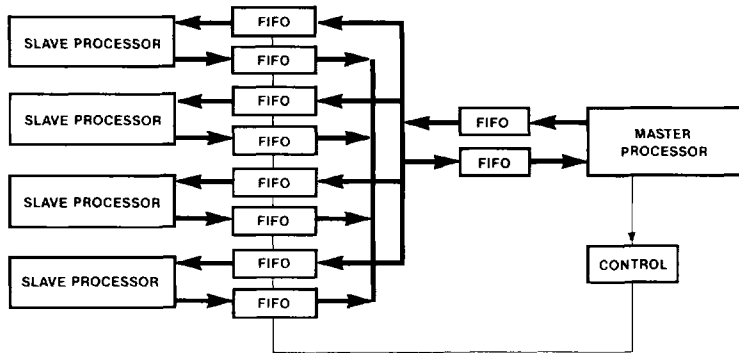
b: Typical Application — High-Speed Multiprocessing System

Figure 2: Reset
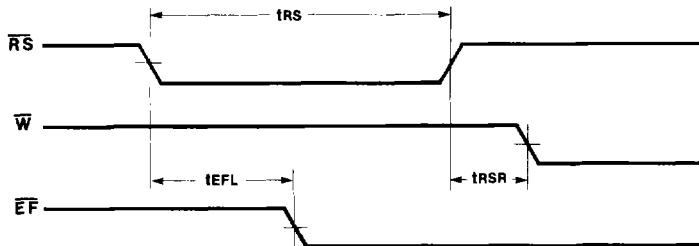
Notes: $t_{RSC} = t_{RS} + t_{RSR}$
$\overline{W}$ and $\overline{R} = V_{IH}$ during RESET

AC725 • ACT725

Figure 3: Asynchronous Write and Read Operation
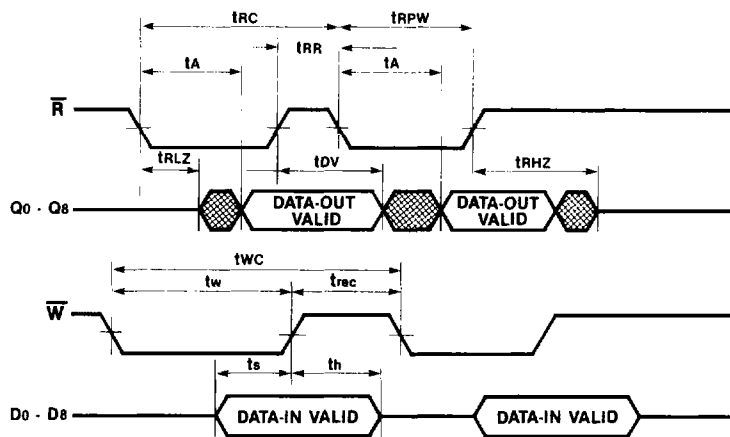
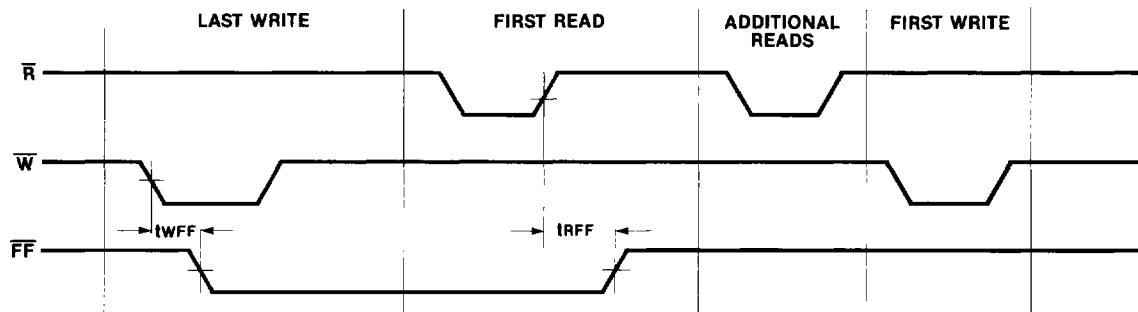Figure 4: Full Flag from Last Write to First Read
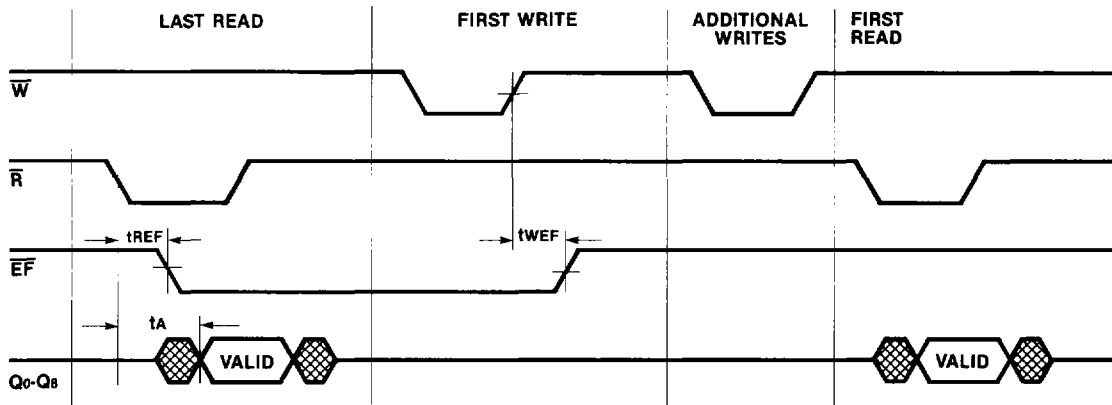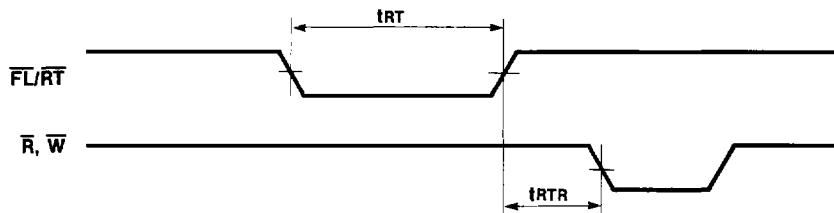
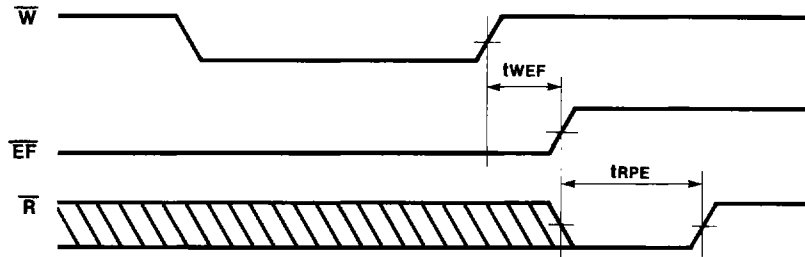## Figure 5: Empty Flag from Last Read to First Write

Figure 6: Retransmit

Notes: $t_{RTC} = t_{RT} + t_{RTR}$

$\overline{EF}/\overline{HF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7: Empty Flag Timing

Note: $t_{RPE} = t_{RPW}$

Figure 8: Full Flag Timing
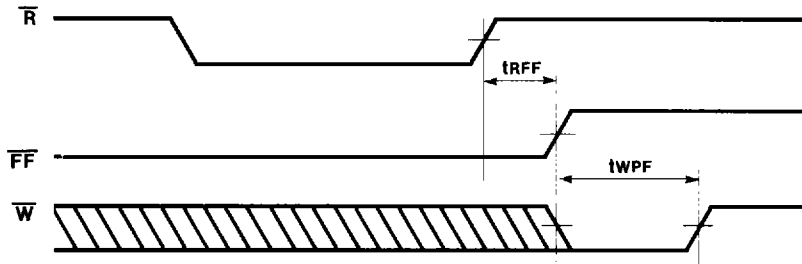
Note: $t_{WPF} = t_{WPW}$

Figure 9: Half-Full Flag Timing

Half-Full or Less ←——— | ←—— More than Half-Full ——→ | ——→ Half-Full or Less
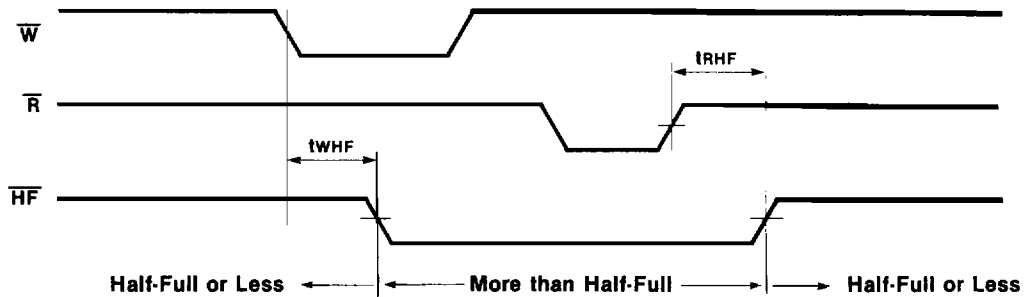
Operating Modes

Single Device Mode

A single 'AC/'ACT725 device may be utilized for applications requiring 512 words or less. The 'AC/'ACT725 is in a single device configuration when Expansion In ($\overline{XI}$) is grounded. In this mode, $\overline{HF}$ flag is valid.
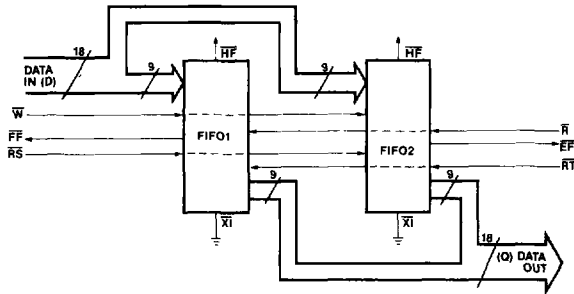
Width Expansion Mode

Word width may be easily increased by connecting the corresponding input control signals of multiple devices. Status flags, $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$, can be detected from any one device. Any word width can be obtained with additional 'AC/'ACT725s.

Figure 10: Block Diagram of Single 512 x 9 FIFO
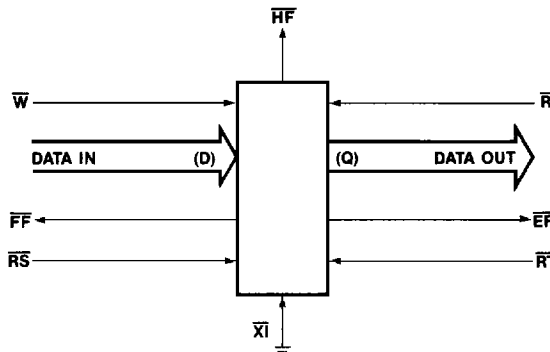
Operating Modes, cont'd

### Figure 11: Block Diagram of 512 x 18 x 18 FIFO Memory Used in Width Expansion Mode

Notes: Flag detection is accomplished by monitoring $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ on any device used in the width expansion configuration. Output signals should not be connected together.

Depth Expansion (Daisy Chain) Mode

The 'AC/'ACT725 can easily be adapted to applications when the requirements are for greater than 512 words. Any depth can be obtained with additional 'AC/'ACT725 devices. The 'AC/'ACT725 operates in the Depth Expansion mode when:

1. $\overline{FL}$ of the first device is grounded.
2. $\overline{FL}$ pins of all other devices are HIGH.
3. $\overline{XO}$ of each device is tied to $\overline{XI}$ of the next device.
4. External logic is needed to generate a composite $\overline{FF}$ and $\overline{EF}$. This requires ORing all $\overline{EF}$s and all $\overline{FF}$s, i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$.
5. The $\overline{RT}$ function and $\overline{HF}$ are not available in the Depth Expansion mode.

5

Figure 12: Block Diagram of a 1536 x 9 FIFO Memory (Depth Expansion)

AC725 • ACT725
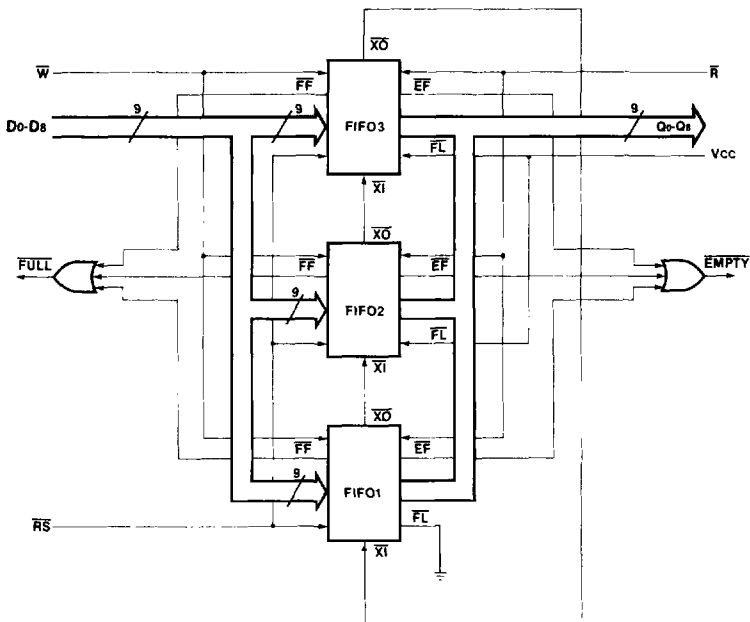
Operating Modes, cont'd

Compound Expansion Mode
The two expansion techniques described previously can be combined in a straightforward manner to achieve large FIFO arrays.

Bidirectional Mode
Applications which require data buffering between two systems (where each system is capable of read and write operations) can be achieved by pairing '725s as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system ($\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in the Bidirectional Mode.

Figure 13: Compound FIFO Expansion
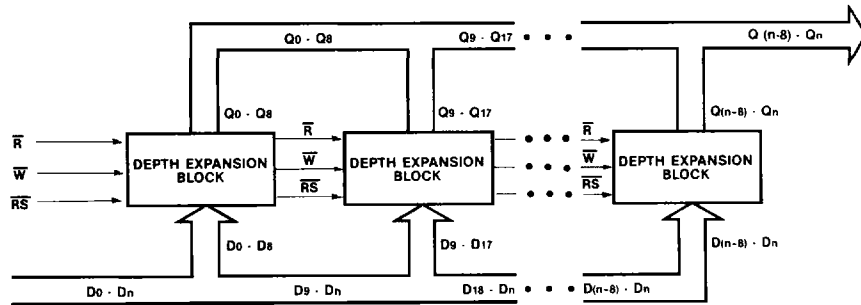
Notes: For depth expansion block, see Depth Expansion and Figure 12.
For flag detection, see Width Expansion and Figure 11.

### Figure 14: Bidirectional FIFO Mode
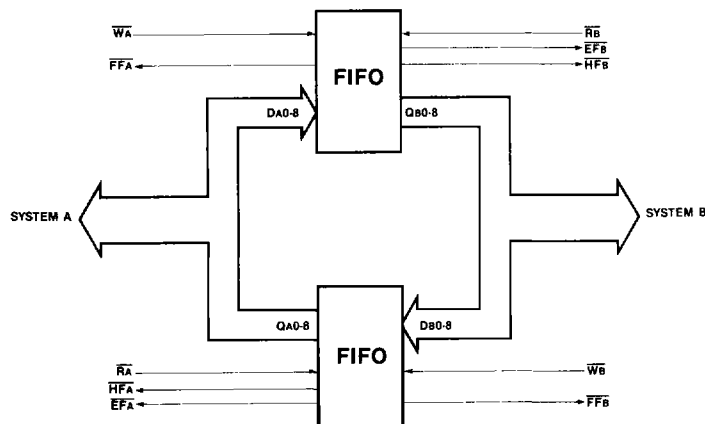
Data Flow-Through Modes

Two types of flow-through modes are permitted with the '725: read flow-through and write flow-through.

For the read flow-through mode (Figure 15), the FIFO permits reading a single word of data immediately upon writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 16), the FIFO permits writing a single word of data immediately after reading one word of data from a completely full FIFO.

Figure 15: Read Data Flow-Through Mode
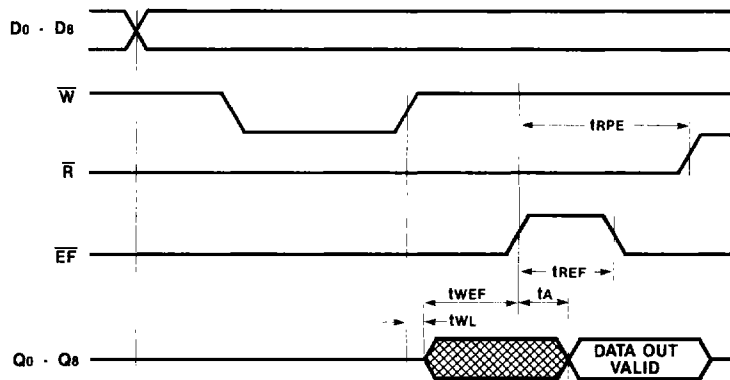
Figure 16: Write Data Flow-Through Mode