FS6244

Dual PLL Clock Generator IC

1.0 Features

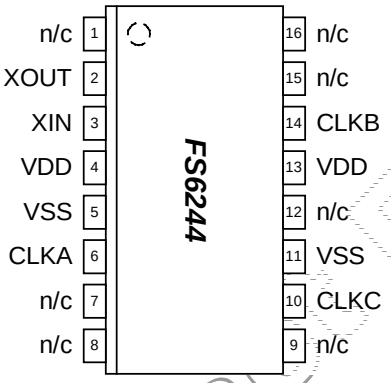
- Dual phase-locked loop (PLL) device with three output clock frequencies
- On-chip crystal oscillator for reference frequency generation
- 3.3V or 5V supply voltage available
- Small circuit board footprint (16-pin 0.150″ SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

2.0 Description

The FS6244 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

Two high-resolution phase-locked loops generate three output clocks through an array of post-dividers. All frequencies are ratiometrically derived from the crystal oscillator frequency. The locking of all the output frequencies together can eliminate unpredictable artifacts in video systems and reduce electromagnetic interference (EMI) due to frequency harmonic stacking.

Figure 1: Pin Configuration



16-pin (0.150″) SOIC

Table 1: Version Information

DEVICE	VDD (nom)	F_{XIN} (MHz)	CLKA (MHz)	CLKB (MHz)	CLKC (MHz)
FS6244-03	5	27.000	11.2896 (+1.1 ppm)	3.6864	27.000

NOTE: Contact AMI for custom versions

Figure 2: Block Diagram

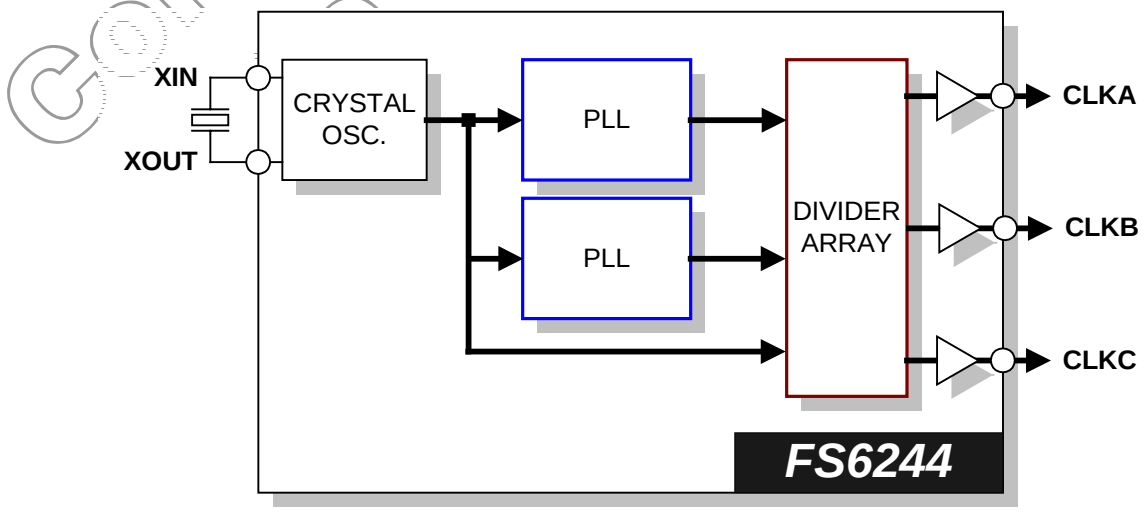


Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	-	N/C	No Connection
2	AO	XOUT	Crystal Oscillator Drive
3	AI	XIN	Crystal Oscillator Feedback
4	P	VDD	Power Supply (+3.3V or +5V)
5	P	VSS	Ground
6	DO	CLKA	Clock Output A
7	-	N/C	No Connection
8	-	N/C	No Connection
9	-	N/C	No Connection
10	DO	CLKC	Clock Output C
11	P	VSS	Ground
12	-	N/C	No Connection
13	P	VDD	Power Supply (+3.3V or +5V)
14	DO	CLKB	Clock Output B
15	-	N/C	No Connection
16	-	N/C	No Connection

3.0 Functional Block Description

3.1 Phase-Locked Loop (PLL)

The on-chip PLLs are a standard frequency- and phase-locked loop architecture. The PLL multiplies the reference oscillator to the desired frequency by a ratio of integers. The frequency multiplication is exact with a zero synthesis error unless otherwise indicated in the frequency table.

3.2 Crystal Oscillator

The Crystal Oscillator provides a stable, low-jitter frequency reference for the rest of the FS6244 system components. Loading capacitance for the crystal is internal to the FS6244. No external components (other than the resonator itself) are required for operation of the crystal oscillator.

4.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage (3.3 volt system)	V_{DD}	SEE NOTE 1	3.0	3.3	3.6	V
Supply Voltage (5.0 volt system)	V_{DD}	SEE NOTE 1	4.5	5.0	5.5	V
Ambient Operating Temperature Range	T_A	SEE NOTE 1	0		70	°C
Crystal Resonator Frequency	f_{XTAL}	Fundamental Mode	5		27	MHz

NOTE 1: These specifications represent generic FS6244 device capability. Device specifications for a particular version (i.e. FS6244-xx) are guaranteed only with the operating voltage and reference frequency specified in Version Information.

Table 5: DC Electrical Specifications (V_{DD} = 3.3V nominal)

Unless otherwise stated, V_{DD} = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{XTAL} = 27MHz; C_L = 10pF, V_{DD} = 3.3V (depends on output frequencies)		15		mA
Crystal Oscillator						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT		17		pF
Crystal Drive Level		R_{XTAL}=20Ω;		200		uW
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}			860		mV
High-Level Input Current	I_{IH}			34		µA
Low-Level Input Current	I_{IL}			-21		µA
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current	I_{OH}	V(XIN) = 0V, V_O = 0V		-0.5		mA
Low-Level Output Sink Current	I_{OL}	V(XIN) = 3.3V, V_O = 3.3V		15		mA
Clock Outputs (CLKx)						
High-Level Output Source Current *	I_{OH}	V_O = 2.0V		-40		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		17		mA
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-55		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		55		mA

Table 6: DC Electrical Specifications (V_{DD} = 5V nominal)

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{XTAL} = 27MHz; C_L = 10pF, V_{DD} = 5.0V (-03 version)		25		mA
Crystal Oscillator						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT		17		pF
Crystal Drive Level		R_{XTAL}=20Ω;		300		uW
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}			950		mV
High-Level Input Current	I_{IH}			50		µA
Low-Level Input Current	I_{IL}			-21		µA
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current	I_{OH}	V(XIN) = 0V, V_O = 0V		-1		mA
Low-Level Output Sink Current	I_{OL}	V(XIN) = 5V, V_O = 5V		20		mA
Clock Outputs (CLKx)						
High-Level Output Source Current *	I_{OH}	$V_O = V_{DD}$ –0.4V		-25		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		25		mA
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-80		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 5V; shorted for 30s, max.		80		mA

Table 7: AC Timing Specifications (V_{DD} = 3.3V nominal)

Unless otherwise stated, V_{DD} = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Overall							
Synthesis Error		(unless otherwise noted in Frequency Table)				0	ppm
Clock Output (CLKx)							
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$) to one clock period		45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$, C_L = 10pF			390		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	From 0-500µs at $V_{DD}/2$, C_L = 10pF compared to ideal clock source			155		ps
Rise Time *	t_r	V_{DD} = 3.3V; V_O = 0.3V to 3.0V; C_L = 10pF			1.7		ns
Fall Time *	t_f	V_{DD} = 3.3V; V_O = 3.0V to 0.3V; C_L = 10pF			1.7		ns

Table 8: AC Timing Specifications (V_{DD} = 5V nominal)

Unless otherwise stated, V_{DD} = 3.3V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Overall							
Synthesis Error		(unless otherwise noted in Frequency Table)				0	ppm
Clock Output (CLKx)							
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$) to one clock period		45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$, C_L = 10pF			390		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	From 0-500µs at $V_{DD}/2$, C_L = 10pF compared to ideal clock source			155		ps
Rise Time *	t_r	V_{DD} = 5V; V_O = 0.5V to 4.5V; C_L = 10pF			1.0		ns
Fall Time *	t_f	V_{DD} = 5V; V_O = 4.5V to 0.5V; C_L = 10pF			1.0		ns

5.0 Package Information

Table 9: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

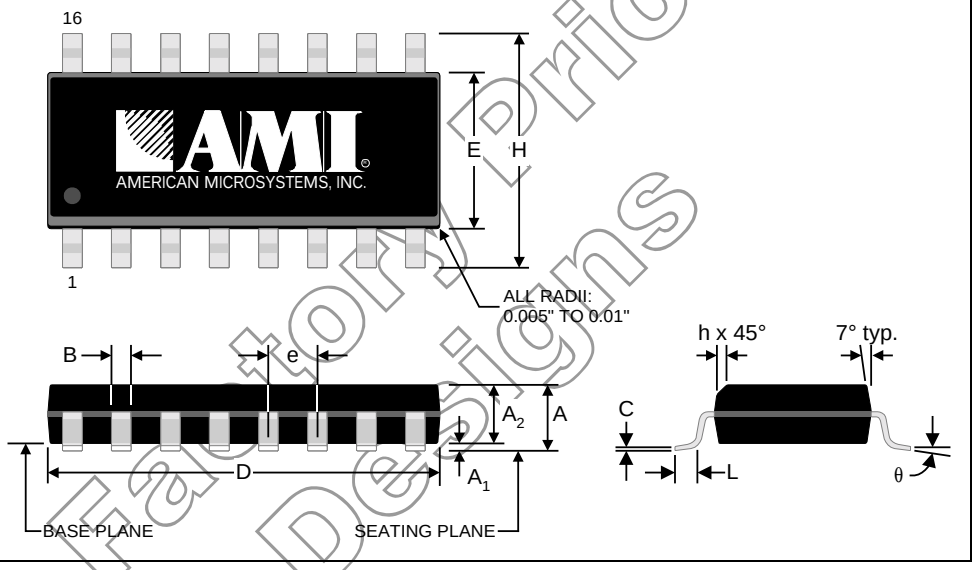


Table 10: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 16-pin 0.150" SOIC	Θ_{JA}	Air flow = 0 m/s	109	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

6.0 Ordering Information

Table 11: Device Ordering Codes

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-821	FS6244-03	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
11640-831	FS6244-03	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes

7.0 Revision Information

DATE	PAGE	DESCRIPTION
4/24/00	5, 7	Fixed formatting errors

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