CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX683
Call Progress and "Voice" Detector

D/683/1 June 2002

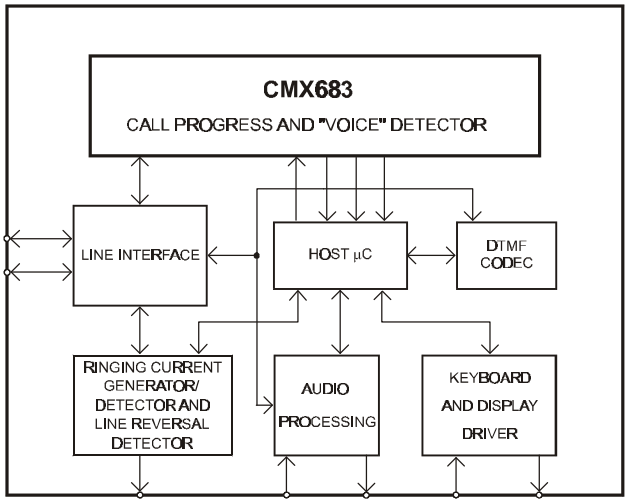
Advance Information

Features

- **Detects Single and Dual Call Progress Tones**
- **Worldwide Call Progress Tone Compatibility**
- **"Voice" Detect Outputs (Fast and Slow)**
- **Wide Dynamic Range with Low Falsing**
- **Low Power Operation: 600µA at 3.0V typ.**
- **3.58MHz Xtal/Clock Oscillator**

Applications

- **Worldwide Payphone Systems**
- **Telephone Redialling Systems**
- **Dialling Modems**
- **Banking and Billing Systems**
- **Telecom Test Equipment**
- **Telecom Security Systems**



1. Brief Description

The CMX683 is a general purpose Call Progress tone detector for use in monitoring the progress of calls in Public Switched Telephone System (PSTN) applications. Dial Tone, Ringing, Busy and Not Available states can be distinguished by using the host µC to qualify the cadence of the CP DETECT output. The CMX683 uses advanced digital techniques to characterise valid Call Progress tones, unwanted tones, line noise and voice or music signals. In contrast to Call Progress detection devices based on simple filtering techniques, the CMX683 offers excellent sensitivity coupled with low false detection rates.

The response time of the CMX683 allows it to operate with almost any Call Progress system. In particular the 'stuttered dial tone' of voice mail messaging systems is supported. The use of statistical processing techniques, which analyse signal frequency, duration and amplitude, enable the CMX683 to distinguish voice or music activity from DTMF or Call Progress signals. Separate outputs integrate the "voice" activity over both shorter and longer periods, enabling payphone and other billing systems to commence charging when a line connection has been established. A single 3.58MHz crystal ensures accurate and repeatable performance. With supply requirements between 2.7V and 5.5V and a low current consumption, the CMX683 can be easily integrated into a wide range of telecom equipments. The CMX683 has a similar pinout to all commonly used Call Progress detectors and is available in DIP, TSSOP or SOIC packages.

CONTENTS

Note: This product is in development: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

Information in this data sheet should not be relied upon for final product design.

2. Block Diagram

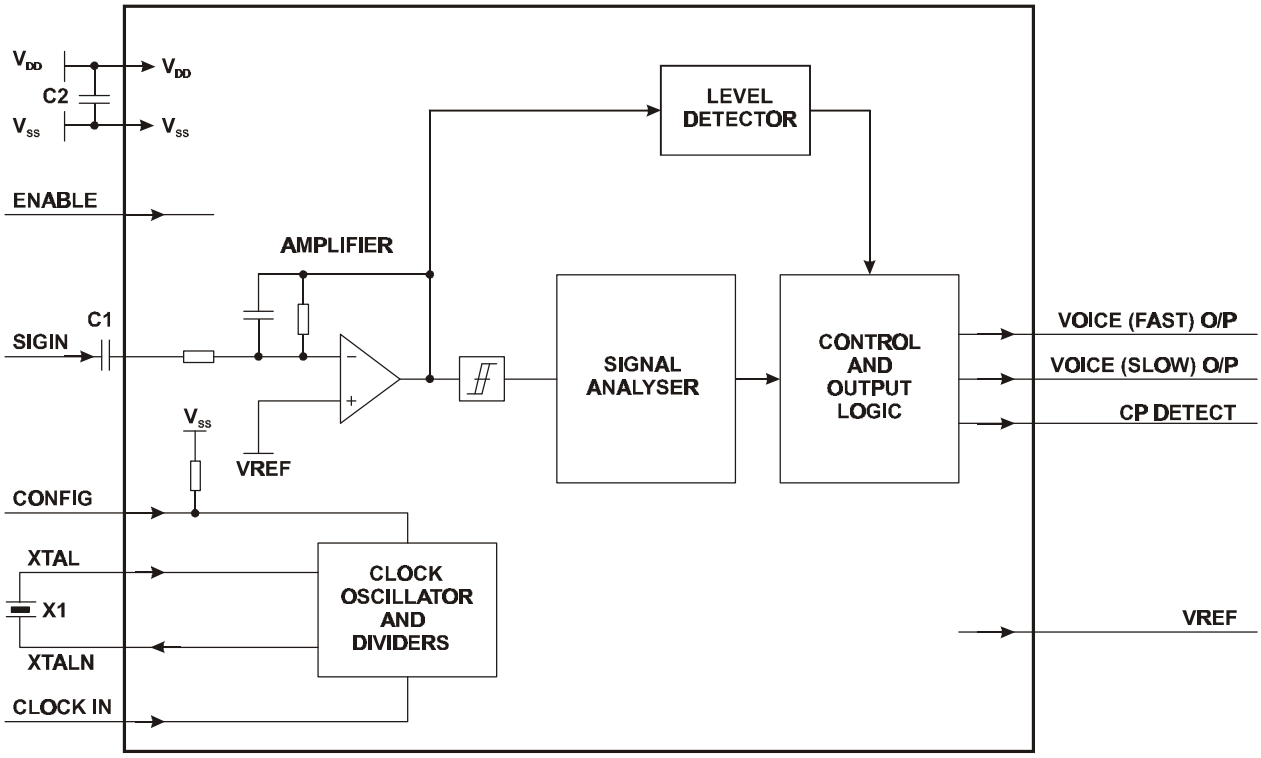


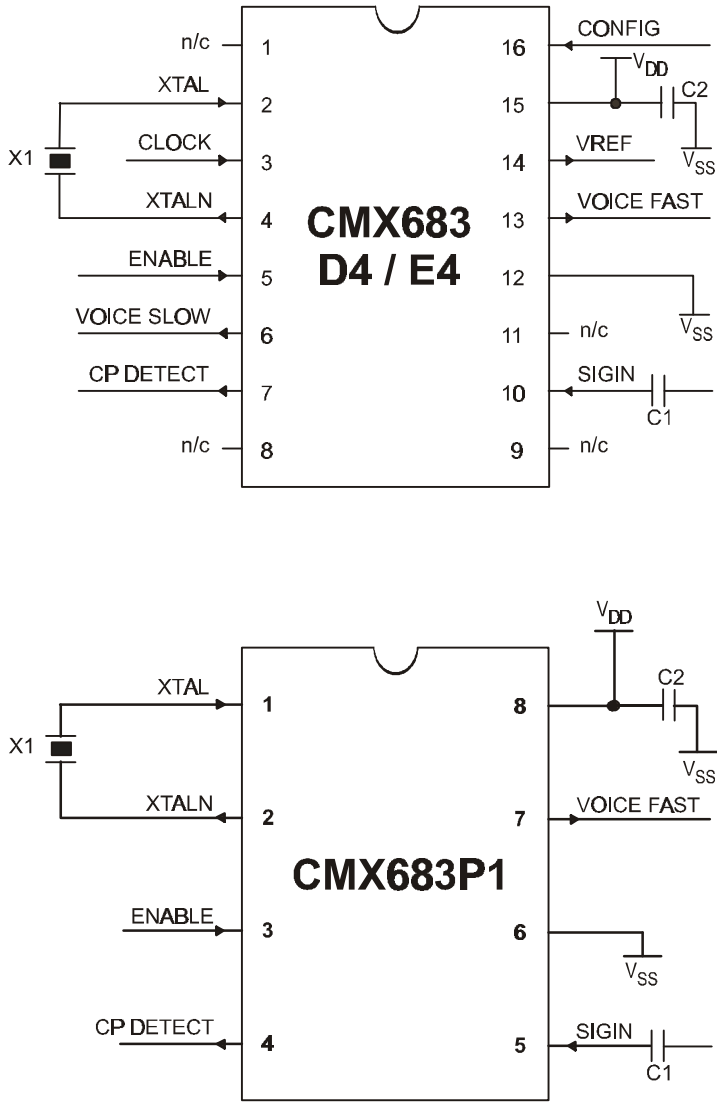
Figure 1 Block Diagram

3. Signal List

SOIC Package	TSSOP Package	DIP Package			
D4 Pin No.	**E4 Pin No.**	**P1 Pin No.**	**Signal Name**	**Type**	**Description**
1	1			NC	Reserved for future use. Do not make any connection to this pin.
2	2	1	XTAL	I/P	The input to the on-chip oscillator, to be used in conjunction with the XTALN output. An external crystal only is required. All other components are on-chip. If the on-chip oscillator is not used, this pin should be connected to V_{SS}.
3	3		CLOCK IN	I/P	The external clock input. Connect the CONFIG pin to V_{DD} to enable this input.
4	4	2	XTALN	O/P	The inverted output of the on-chip oscillator. Leave unconnected if not used.
5	5	3	ENABLE	I/P	A logic 1 applied to this input enables all detector outputs. A logic 0 will force all detector outputs to a logic 0.
6	6		VOICE SLOW	O/P	When a Non Call Progress signal is detected this output goes to a logic 1. (See Table 1).
7	7	4	CP DETECT	O/P	When a Call Progress signal is detected this output goes to a logic 1. (See Table 1).
8	8			NC	Reserved for future use. Do not make any connection to this pin.
9	9			NC	Reserved for future use. Do not make any connection to this pin.
10	10	5	SIGIN	I/P	Signal input (which should be ac coupled as the dc bias on this pin is set internally).
11	11			NC	Reserved for future use. Do not make any connection to this pin.
12	12	6	V_{SS}	Power	The negative supply rail (ground).
13	13	7	VOICE FAST	O/P	When a Non Call Progress signal is detected this output goes to a logic 1. (See Table 1).
14	14		VREF	O/P	Internally generated reference voltage held at $½V_{DD}$ and available to power external circuits.
15	15	8	V_{DD}	Power	The positive supply rail. This pin should be decoupled to V_{SS} by a capacitor.
16	16		CONFIG	I/P	Oscillator configuration. Leave unconnected when using an external crystal. This pin has an internal pulldown to the V_{SS} pin.

Notes: I/P = Input O/P = Output NC = No Connection

4. External Components



Typical Values:

C1	0.1µF	± 20%
C2	0.1µF	± 20%
X1	3.579545MHz (refer to Section 1.7.1)	

Note: C1 is not required if the input is referenced to VREF.

Figure 2 Recommended External Components

To achieve good noise performance, V_{DD} decoupling and protection of the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX683 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} decoupling capacitor.

5. General Description

5.1 Overall Function Description

The CMX683 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices from other suppliers use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300 and 700 Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech, music, DTMF and noise. False outputs are a common feature with these products. To avoid background noise causing a stuck “detect” output, the sensitivity of such devices is often poor.

The CMX683, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domains, with signal amplitude forming part of the decision process. This analysis includes checks on whether the signal has a profile which matches international standards for Call Progress tones, or whether the profile is more likely to match that of DTMF, speech, music, noise or no signal. The frequency response of the CMX683 is confined to the Call Progress band, plus a small extension above and below this band. This ensures that the CMX683 will not respond to FAX, Modem or other out-of-band signals.

The following Glossary and the Decode Truth Table in section 5.4 provide a simple explanation of the decoding functions and features offered by the CMX683.

5.2 Glossary

Call Progress Tones: The single and dual frequency tones in the range 350 to 620 Hz which are specified widely for call progress signalling.

Call Progress Band: The nominal range 315 to 650 Hz within which the CMX683 will detect Call Progress tones. The detection algorithm requires that these tones have the characteristics typical of Call Progress Tones.

No Signal: The absence of an input signal (below the detection threshold) or
A signal below 190Hz or
A signal between 900Hz and 10kHz.

Non Call Progress ("Voice") Signal:
A signal falling within the nominal range of 190 to 895 Hz,
but NOT within the Call Progress band or
A signal falling within the nominal range of 190 to 895 Hz,
but NOT meeting the Call Progress detection requirements for that part of the signal which falls within the Call Progress band. Subject to the duration and other characteristics of such signals, the CMX683 will usually interpret these as a Non Call Progress signal (ie "Voice" activity).

Note that signals above 10kHz should not exceed -38dB (relative to 775mVrms), to avoid aliasing.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

5.3 Block Diagram Description

Amplifier
The input signal is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at ½V_{DD}.

Signal Analyser
The frequency range, quality and consistency of the input signal is analysed by this functional block. To be classified as a Call Progress signal the input signal frequencies must lie between 315 and 650 Hz, and the signal to noise ratio must be 16dB or greater. The signal must have a minimum rms amplitude of about -60dB (relative to 775mVrms) and the signal must be consistent over a period of about 80ms. These decode criteria are continuously monitored and the assessment is updated every 6ms. To be classified as a Non Call Progress ("Voice") signal the input signal frequencies must lie between 190 and 895 Hz and the frequencies must not match the predefined profiles for DTMF or Call Progress signals. The signal must have a minimum rms amplitude of about -60dB (relative to 775mVrms) and the signal must show activity over a period of about 145ms (fast response) or 500ms (slow response).

Control and Output Logic
This block categorises the nature of the signal into Call Progress and Non Call Progress output states. A Non Call Progress output is further checked for activity over a longer detection period, resulting in a VOICE FAST output responding to speech/music in around 145ms and a VOICE SLOW output (with a more consistent detection) responding in around 500ms. If the VOICE FAST output is at logic 1 for more than 51% of the previous 728ms then the VOICE SLOW output will change to a logic 1. If the VOICE FAST output is at logic 1 for less than 10% of the previous 728ms then the VOICE SLOW output will change to a logic 0. The Decode Output Truth Table on the following page gives further details. Also refer to the timing diagram in Figure 4.

Level Detector
The Level Detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold, which has a nominal value of -42dB (relative to 775mVrms). The Level Detector output goes to the Control and Output Logic block, where the Call Progress signal and Voice detector outputs are gated with the Level Detector output. The CP DETECT, VOICE FAST and VOICE SLOW outputs are valid only if the input signal level is above this preset threshold.

Xtal Oscillator
If the on-chip Xtal oscillator is to be used, an external 3.58MHz crystal (X1) only is required and the CONFIG pin should be left unconnected. If an external clock source is to be used, the clock should be connected to the CLOCK IN input pin and the XTAL pin should be connected to V_{SS}. The XTALN pin should be left unconnected and the CONFIG pin must be connected to V_{DD}. Note that this external clock option is not available with the P1 package.

5.4 Decode Output Truth Table

In the following Truth Table it should be noted that it is possible to get both CP DETECT and VOICE FAST or VOICE SLOW outputs simultaneously at logic 1. If the activity is initially consistent with and meets the Call Progress signal profile, the CP DETECT output will go to logic 1. If the activity subsequently meets the Non Call Progress signal profile, the VOICE FAST output (and, eventually, the VOICE SLOW output) will go to a logic 1 without changing the CP DETECT output. The host µC must then use cadence information to decide what signal is present.

Note that CP DETECT responds to the whole range of Call Progress tones from 315 to 650 Hz.

CONDITIONS	CP DETECT	"VOICE" FAST/SLOW
No Signal	0	0
Call Progress Signal: Will detect 350+440, 400+450, 440+480, 400, 425, 440, 450, 480+620, 600 and 620Hz tones	1	0
DTMF Signal	0	0
Non Call Progress Signal (eg voice)	0	1
FAX/Modem or other out-of-band signals	0	0

Table 1 Decode Output Truth Table

6. Application Notes

On power-up, it will take no more than 15ms to initialise the internal state. This delay should be accounted for before the CP DETECT, VOICE SLOW and VOICE FAST outputs are valid.

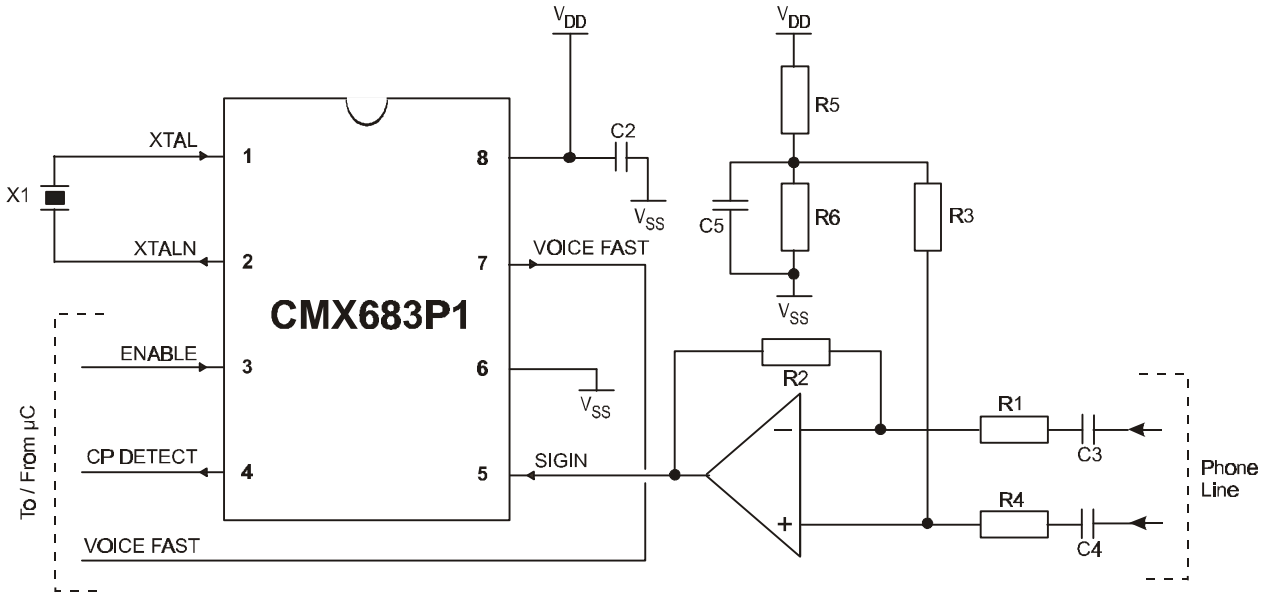


Figure 3 A typical Telephone Line Circuit Application

R1	470kΩ	R4	470kΩ	C2	0.1µF
R2	470kΩ	R5	100kΩ	C3	0.01µF 250V
R3	470kΩ	R6	100kΩ	C4	0.01µF 250V
				C5	0.1µF

Note: 1. Resistors ±1%, Capacitors ±20%, unless otherwise stated.
2. A low offset opamp is needed. The decoupling capacitor C1 is not required if the quiescent dc
level at the opamp output is the same as VREF.

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

P1 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

E4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		300	mW
... Derating		5.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Xtal Frequency		3.57	3.59	MHz

7.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

Xtal Frequency = 3.579545MHz, S/N = 16dB, Noise Bandwidth = 5kHz,
V_{DD} = 3.0V to 5.0V, Tamb = -40°C to +85°C. 0dB = 775mVrms.

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD} (ENABLE = 0)	(V_{DD} = 5.0V)	1	–	250	–	µA
I_{DD} (ENABLE = 1)	(V_{DD} = 5.0V)	1	–	1.0	1.5	mA
I_{DD} (ENABLE = 1)	(V_{DD} = 3.0V)	1	–	0.6	1.0	mA
V_{REF} Output		8	45%	50%	55%	V_{DD}
AC Parameters						
SIGIN pin						
Input Impedance		2	–	0.1	–	MΩ
Minimum Input Signal Level			–	-38.0	–	dB
Input Signal Dynamic Range			40.0	–	–	dB
Signal to Noise Ratio			16.0	–	–	
Clock Input						
'High' Pulse Width		3	100	–	–	ns
'Low' Pulse Width		3	100	–	–	ns
Gain (I/P = 1mVrms at 100Hz)			20.0	–	–	dB
Level Detector						
Must Detect Signal Level		4	-38.0	–	–	dB
Must Not Detect Signal Level		4	–	–	-50.0	dB
Call Progress Band		7				
Must Detect Range			315	–	650	Hz
Must Not Detect Range			750	–	250	Hz
Logic Interface						
Input Logic 1 Level		5	80%	–	–	V_{DD}
Input logic 0 level		5	–	–	20%	V_{DD}
Input leakage current (Vin = 0 to V_{DD})		5	-5.0	–	+5.0	µA
Input Capacitance		5	–	7.5	–	pF
Output logic 1 level (I_{OH} = 120µA)		6	90%	–	–	V_{DD}
Output logic 0 level (I_{OL} = 360µA)		6	–	–	10%	V_{DD}

Notes:
1. Not including any current drawn from the CMX683 pins by external circuitry.
2. Small signal impedance over the frequency range 100Hz to 2000Hz and at V_{DD} = 5.0V.
3. Timing for an external input to the CLOCK IN pin.
4. Input signal level at V_{DD} = 5.0V, scale signal for different V_{DD}.
5. ENABLE and CONFIG pins.
6. CP DETECT, VOICE FAST and VOICE SLOW pins.
7. Nominal values which are subject to dynamic tolerances within the signal analysis process, as a result of using stochastic signal processing techniques.
8. Load impedance on this output must exceed 330kΩ.

Electrical Performance (continued)

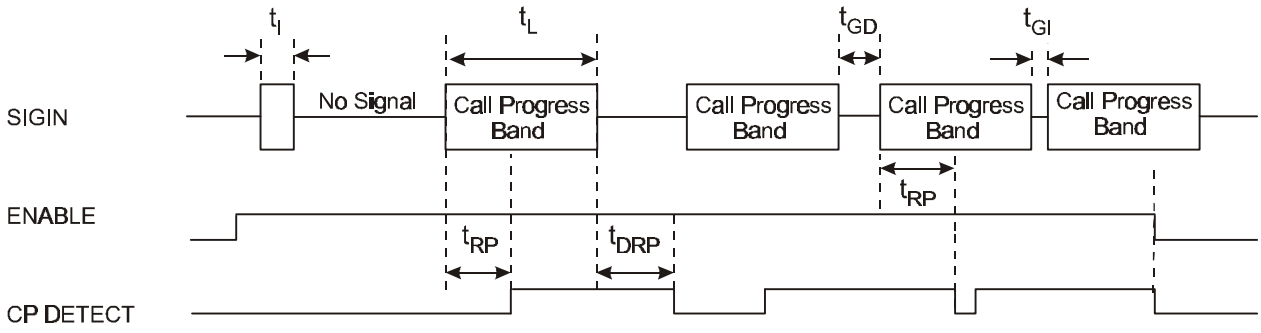


Figure 4 µC Parallel Interface Timings

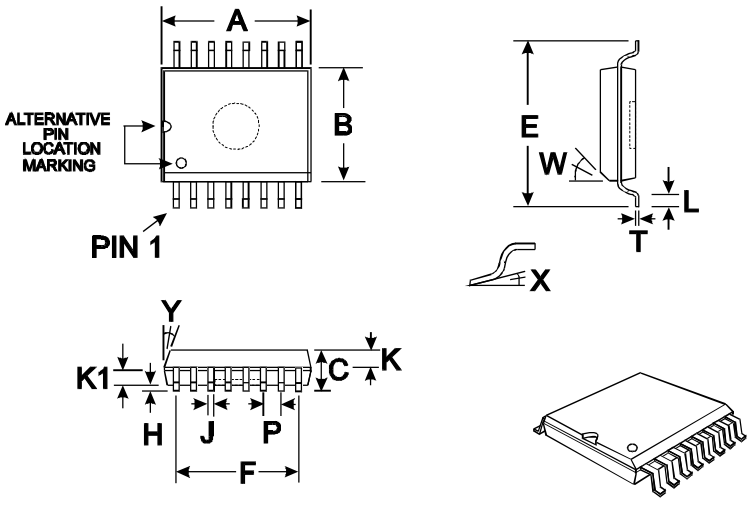
For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, V_{DD} = 3.0V to 5.0V, Tamb = -40°C to +85°C, S/N = 20dB.

		Notes	Min.	Typ.	Max.	Units
Signal Timings (ref. Figure 4)						
t_I	Burst Length Ignored				40.0	ms
t_L	Burst Length Detected		80.0			ms
t_{GI}	Call Progress Tone Gap Length Ignored	9			20.0	ms
t_{GD}	Call Progress Tone Gap Length Detected	9	40.0			ms
t_{RP}	Call Progress Tone Response Time	10			80.0	ms
t_{DRP}	Call Progress Tone De-Response Time	10			80.0	ms

Notes: 9. Only applies to bursts of the same frequency.
10. Measured with 350 + 440 Hz tone pair.

7.2 Packaging



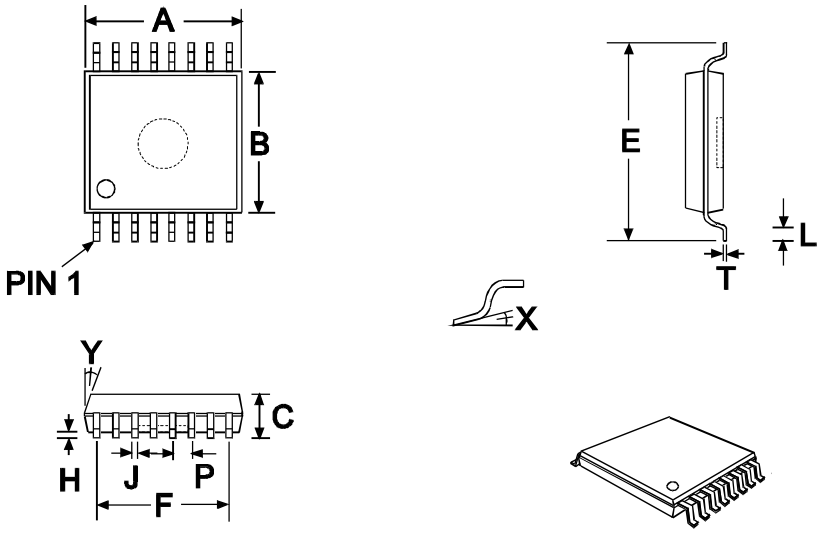
DIM.	MIN.	TYP.	MAX.
* A	0.395 (10.03)		0.413 (10.49)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.350 (8.89)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 5 SOIC Mechanical Outline: ***Order as part no. CMX683D4***



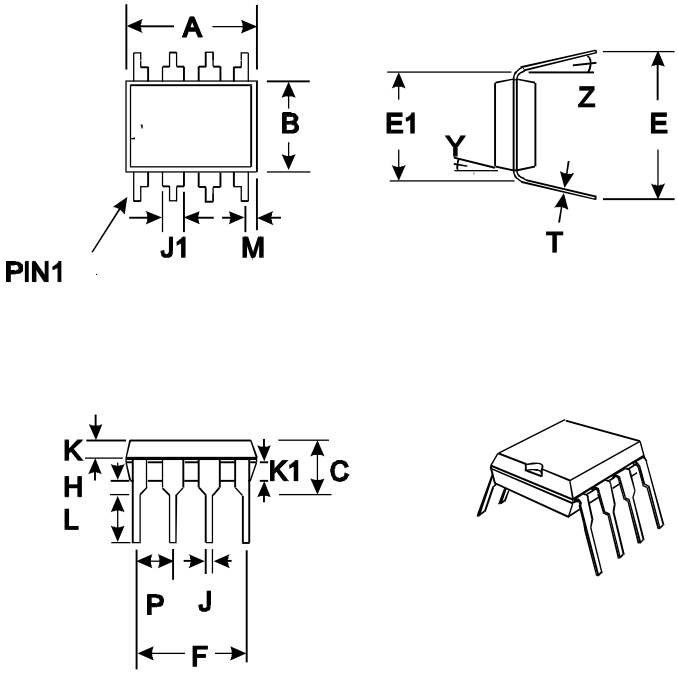
DIM.	MIN.	TYP.	MAX.
* A	0.193 (4.90)		0.201 (5.10)
* B	0.169 (4.30)		0.177 (4.50)
C	-------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.179 (4.55)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6 TSSOP Mechanical Outline: ***Order as part no. CMX683E4***



DIM.	MIN.	TYP.	MAX.
* A	0.346 (8.790)		0.400 (10.16)
* B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.08)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.25)
F		0.30 (7.62)	
H		0.030 (0.76)	
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.062 (1.58)	
K1		0.062 (1.58)	
L	0.121 (3.07)		0.150 (3.81)
M		0.029 (0.74)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 7 DIP Mechanical Outline: *Order as part no. CMX683P1*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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