Semiconductor Corporation

CS6152

Low Power T1 Analog Interface

Features

- Provides Analog T1 Line Interface
- Low Power Consumption (normally 180 mW)
- SMART *Analog* ™ Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer Which Compliments Digital Gate Array Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components

General Description

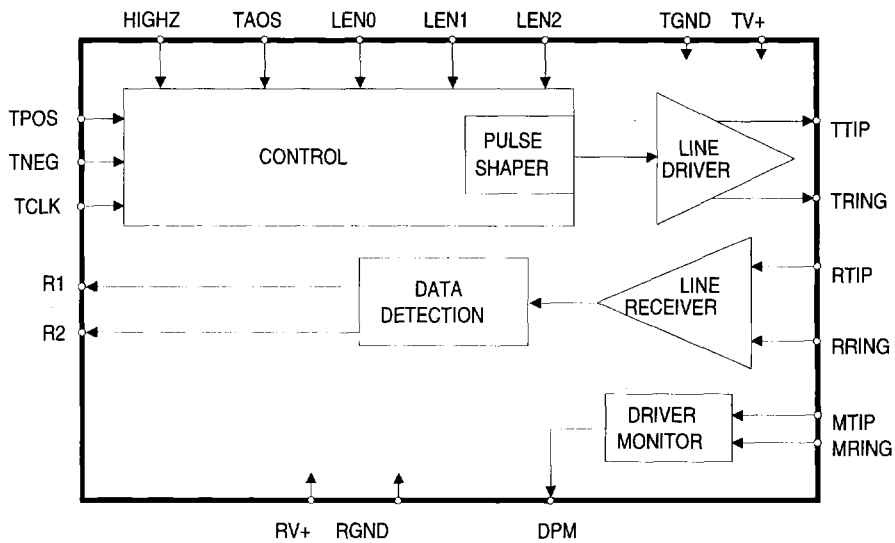
The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

Applications

- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexors, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152A-IP - 24 Pin Plastic, 300 mil DIP
CS6152-IL - 28 Pin J-lead PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	(RGND) - 0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, MTIP, and MRING, which must stay within a range of -6V to (RV+)+0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Notes 4 and 5) 100% ones density & max. line length @ 5.25V	P_D	-	-	350	mW
Normal Power Dissipation (Notes 4 and 5) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	180	-	mW
Normal Power Dissipation (Notes 5 and 6) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	145	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 54 Ω load over operating temperature range. Includes CS6152 and load.
5. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
6. Power dissipation internal to CS6152 while driving 54 Ω load over operating temperature range.

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 7) I_{OUT} = ±4 mA; PINS: R1, R2, DPM	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 7) I_{OUT} = ±4 mA; PINS: R1, R2, DPM	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	µA
3-State Leakage Current PINS: R1, R2, DPM	I_{OZ}	-	-	±10	µA

Notes: 7. Output drivers are high speed CMOS compatible.

ANALOG SPECIFICATIONS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes Line Length Selections LEN2/1/0 = 0/0/0 (Measured at transformer output)		2.7	3.0	3.3	V
All line length settings except, LEN2/1/0 = 0/0/0; 0/0/1; 0/1/0 (Measured at the DSX; Nomalization factor for Figure 4)		2.4	3.0	3.6	V
Load Presented to Transmitter Output		-	54	-	Ω
Jitter Added by the Transmitter (Note 8) 10Hz - 8kHz		-	0.005	-	UI
8kHz - 10kHz		-	0.008	-	UI
10HZ - 40kHz		-	0.010	-	UI
Broad Band		-	0.015	-	UI
Power in 2kHz band at 772kHz (Note 9)		12.6	15	17.9	dBm
Difference in power in 2kHz band at 1.544MHz to power in 2 kHz band at 772kHz (Note 9)		-29	-40	-	dB
Positive to Negative Pulse Imbalance (Note 9)		-	0.2	0.5	dB
Receiver					
Input Signal Squelch Level (Note 10)		-	0.5	-	mV
Data Decision Threshold Squelch Level < RTIP/RRING < 4.14 V		65	70	75	% of peak

Notes: 8. Input signal to TCLK is jitter free.
9. Measured with a nonpolarized 0.47 µF capacitor in series with the primary of the transmit transformer. Not production tested. Parameters guaranteed by design and characterization.
10. The squelch circuit operates when the DSX-1 receiver input signal amplitude falls below approximately 500 mVp, Operation of the squelch circuit causes R1 and R2 to remain low.

T1 SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Frequency	f_{in}	-	1.544	-	MHz
RTIP/RRING Rising to R1/R2 Rising (Note 11)	t_{dr}	20	45	150	ns
RTIP/RRING Falling to R1/R2 Falling (Note 11)	t_{df}	60	135	370	ns
Rise Time, All Digital Outputs (Note 12)	t_r	-	-	30	ns
Fall Time, All Digital Outputs (Note 12)	t_f	-	-	30	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_h	50	-	-	ns

Notes: 11. Both rising and falling delays will exhibit similiar tendencies, that is, for fast process, times will tend towards minimum delay times; slower process results in longer delays.
12. At max load of 4.0 mA and 50 pF.

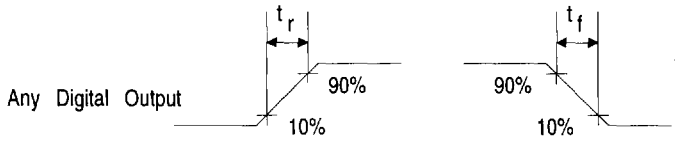


Figure 1. - Signal Rise and Fall Characteristics

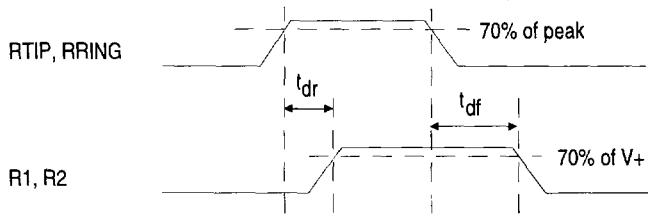


Figure 2. - Receiver Switching Characteristics

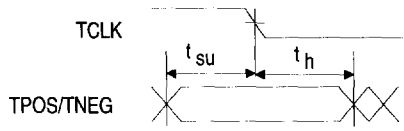


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS6152 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 Volt supply, a 1:1.36, step-up transformer is required. The line driver is designed to drive a 54 Ω equivalent load.

When any transmit control pin (TAOS or LEN0/1/2) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter options are: HIGHZ which places TTIP, TRING, R1, and R2 in a high impedance state, and TAOS which transmits an AMI-encoded all ones on TTIP/TRING.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. These phases are then used to trigger different portions of the output waveform. The line length selection offers a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS6152 modifies the output pulse to meet the requirements of Compatibility Bulletin 119. The exact pulse shape achieved at the DSX-1 can be effected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	APPLICATION
0	1	1	0-133	DSX-1 ABAM (AT&T 600B Or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	1		Reserved
0	1	0		
0	0	0	Part 68, Option A	CSU
0	1	1	T1C1.2	

Table 1 - Line Length Selection

The T1 CSU pulse shapes meet FCC Part 68 for 0dB line build out and future ECSA T1C1.2 pulse shapes as shown in Table 1.

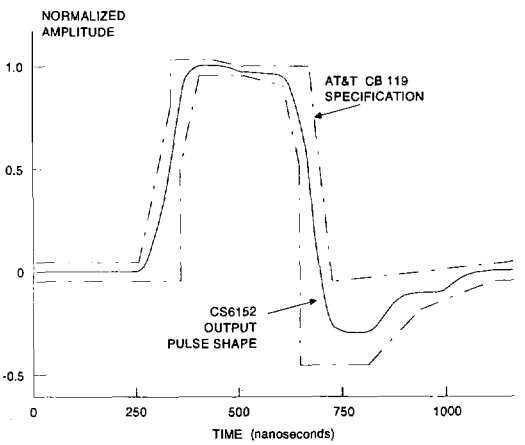


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6152 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will transition high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV within 64±2 TCLK cycles. If TCLK stops, DPM can not change state. The driver performance monitor is not designed to detect transmitted bipolar violations or broken printed circuit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING. DPM should be averaged externally in hardware or software for approximately 500 ms to filter short events caused by very low ones density.

Whenever more than one CS6152 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS6152 monitor performance of a neighboring CS6152 device, rather than having it monitor its own performance.

Receiver

The receiver converts AMI (Alternate Mark Inversion) coded signals to binary (dual unipolar) data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators detect pulses on RTIP and RRING. The comparators switching threshold is dynamically established to be approximately 70% of the peak signal level. The comparator outputs are output on R1 and R2 respectively. A positive pulse on RTIP results in a positive pulse on R1. A positive pulse on RRING results in a positive pulse on R2. The pulses are stretched by approximately 90 ns before being output on R1 and R2.

Squelch control in the receiver will force R1 and R2 low if the inputs on RTIP and RRING are below the squelch level of approximately 0.5 Volts.

Power On Reset

Upon power-up, the CS6152 is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this happens, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay line used in the transmit section commences. The delay line can be calibrated only if the transmit clock is present. The initial calibration should take less than 20 ms after TCLK is applied.

In operation, the delay line is continuously calibrated, making the performance of the device independent of power supply or temperature variations, and eliminating the need to reset a CS6152 when in operation.

Power Supply

The device operates from a single 5 Volt supply. Decoupling and filtering of the power supplies is crucial for proper operation of the analog circuits in the transmit and receive paths. Separate pins for transmit and receive supplies provide internal isolation. TV+ should be connected to RV+ externally and each power supply pin should be

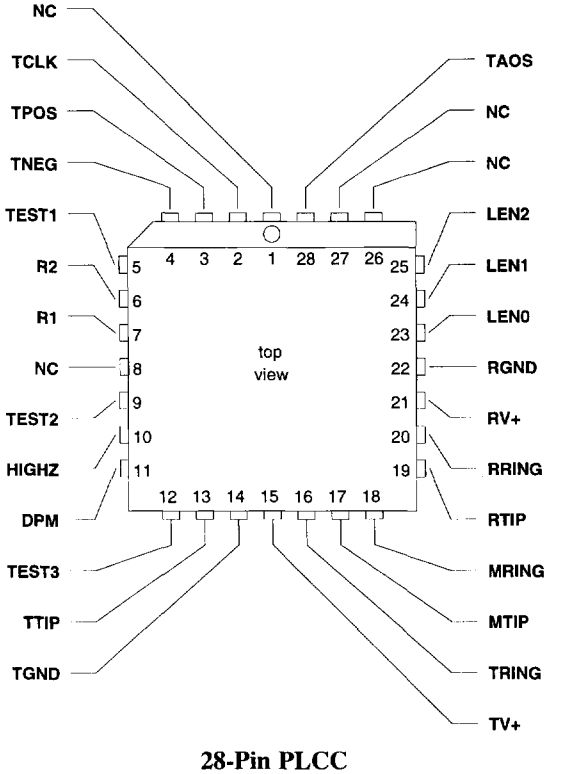
decoupled to its respective ground. TV+ must not exceed RV+ by more than 0.3V.

A 1µF capacitor should be connected between TV+ and TGND, and a 0.1µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire wrap bread-boarding of the CS6152 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

TRANSMIT CLOCK	**TCLK**	1	24	**TAOS**	TRANSMIT ALL ONES SELECT
TRANSMIT POSITIVE PULSE	**TPOS**	2	23	**LEN2**	BIT 2 OF LINE LENGTH SELECT
TRANSMIT NEGATIVE PULSE	**TNEG**	3	22	**LEN1**	BIT 1 OF LINE LENGTH SELECT
FACTORY TEST1	**TEST1**	4	21	**LEN0**	BIT 0 OF LINE LENGTH SELECT
RECEIVED SIGNAL 2	**R2**	5	20	**RGND**	RECEIVE GROUND
RECEIVED SIGNAL 1	**R1**	6	19	**RV+**	RECEIVE V+ (+5VDC)
FACTORY TEST2	**TEST2**	7	18	**RRING**	RECEIVE RING
HIGH IMPEDANCE	**HIGHZ**	8	17	**RTIP**	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	**DPM**	9	16	**MRING**	MONITORED RING
FACTORY TEST3	**TEST3**	10	15	**MTIP**	MONITORED TIP
TRANSMIT TIP	**TTIP**	11	14	**TRING**	TRANSMIT RING
TRANSMIT GROUND	**TGND**	12	13	**TV+**	TRANSMIT V+ (+5VDC)

24-Pin DIP



28-Pin PLCC

Power Supplies

TV+ - Positive Power Supply, Transmit Drivers.
Positive power supply for the transmit drivers; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers.
Power supply ground for the transmit drivers; typically 0 Volts.

RV+ - Positive Power Supply.
Positive power supply for the device, except transmit drivers; typically +5 Volts.

RGND - Ground.
Power supply ground for the device, except transmit drivers; typically 0 Volts.

Control

HIGHZ - High Impedance.
Setting HIGHZ to a logic 1 causes TTIP, TRING, DPM, R1, and R2 to enter a high impedance state. This pin is internally pulled down, so the device will be in normal operating mode if this pin is left floating.

TAOS - Transmit All Ones Select.
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

LEN0, LEN1, LEN2 - Line Length Selection.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TEST1, TEST2, TEST3 - Factory Test1, 2, 3.
Reserved for factory testing, TEST1 must be tied low for normal operation. TEST2 and TEST3 should be left floating.

Inputs

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data.
Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted. If the clock signal is removed from TCLK, then TPOS and TNEG should both be logic low during last falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring.
The AMI receive signal is input to these pins. A center-tapped, center-grounded, 1:2, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data is buffered and output on R1 and R2.

MTIP, MRING - Monitored Tip, Monitored Ring.
These pins are normally connected to TTIP and TRING and monitor the output of a CS6152. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

DPM - Driver Performance Monitor.

If no signal is present on MTIP and MRING for between 31 to 63 clock cycles, DPM goes to a logic 1 until the first detected signal. If TCLK is static, DPM cannot change state.

Outputs

TTIP, TRING - Transmit Tip, Transmit Ring.

The AMI signal is driven to the line through these pins. This output is designed to drive a 54 Ω load. A 1.36:1 step-up transformer is required as shown in Figure A1.

R1, R2 - Received Signal 1, Received Signal 2.

RTIP and RRING inputs are buffered and stretched before being output digitally on R1 and R2 respectively.

Miscellaneous

NC - No Connection (PLCC package only) Pins, 1, 8, 26, 27.

APPLICATIONS

Line Interface

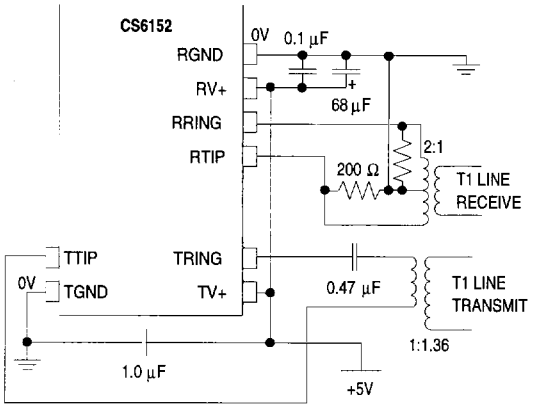


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS6152 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS6152 side. These resistors provide the 100 Ω termination for the T1 line.

To save on power consumption under normal operating conditions, the line driver outputs, TTIP and TRING, are forced into a high impedance state during the transmission of a space (zero) on to the line. Just prior to transmitting a mark (one), the driver outputs are enabled. The transformer interacting with the driver can cause a slight voltage difference (< 200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

Transformers

Transformers listed below have been found to be suitable for use with the CS6152. Receive transformer specifications are not as critical.

Manufacturer	Part#
Transmit + Receive	
Pulse Engineering	PE-64952
Bel Fuse	0553-0013-2J
Transmitter	
Schott	67130240
Midcom	671-5961
Pulse Engineering	PE-65586
Bel Fuse	0553-0013-YC
Receiver	
Pulse Engineering	PE-65351
Schott	67129300
Midcom	671-5832
Bel Fuse	0553-0013-HC

A 1:1.36 turns ratio transformer is required for the transmit side. The receiver side transformer is normally 1:2 turns ratio. However, the receiver side transformer can be 1:1.36 if it is necessary to have only 1 type of transformer, at the expense of a few dB of receive sensitivity. The input squelch level of the CS6152 is set at 0.5 V, with a 1:2 transformer. Using a 1:1.36 transformer will lower the effective squelch level.