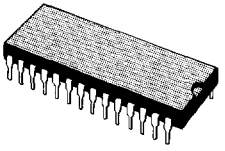
CMOS MICROCONTROLLERS

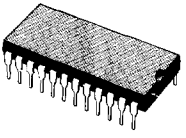
- LOWEST POWER DISSIPATION (50µW typical)
- POWER SAVING IDLE STATE AND HALT MODE
- FULLY STATIC (can turn off the clock)
- 2 K x 8 ROM, 128 x 4 RAM (ETC9444, C9445)
- 1 K x 8 ROM, 64 x 4 RAM (ETC9420, C9421, C9422)
- TRUE VECTORED INTERRUPT, PLUS RESTART
- 3-LEVEL SUBROUTINE STACK
- 4µSEC INSTRUCTION TIME, PLUS SOFTWARE SELECTABLE CLOCKS
- 23 I/O LINES (ETC9444, C9420)
- SINGLE SUPPLY OPERATION (2.4V to 5.5V)
- PROGRAMMABLE READ/WRITE 8-BIT TIMER/EVENT COUNTER
- INTERNAL BINARY COUNTER REGISTER WITH MICROWIRE® SERIAL I/O CAPABILITY
- GENERAL PURPOSE AND TRI-STATE® OUTPUTS
- LSTTL/C MOS COMPATIBLE
- MICROBUS® COMPATIBLE
- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF ET9400 FAMILY
- EXTENDED TEMPERATURE RANGE DEVICES ETC9320/ETC9321, ETC9322 AND ETC9344/ETC9345 (- 40°C to + 85°C)
- SOIC 20/24/28 AND PLCC 28 PACKAGES AVAILABLE

ETC9420/ETC9444
ETC9320/ETC9344



N
(Plastic Package)

ETC9421/ETC9344
ETC9321/ETC9345



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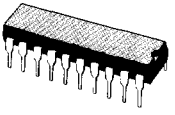
ETC9422/ETC9322



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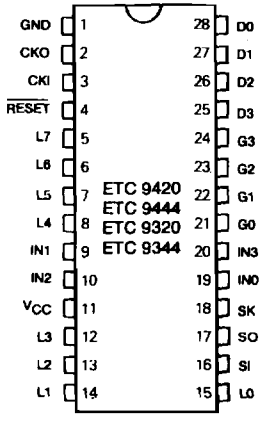
PIN CONNECTIONS



DESCRIPTION

The ETC9420/21/22, ETC9320/21/22, and ETC9444/45, ETC9344/45 fully static single-chip CMOS microcontrollers are fully compatible with the COPS® family, fabricated using double-poly, silicon gate complementary MOS technology. These Controller Oriented Processors are complete microcontrollers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications.

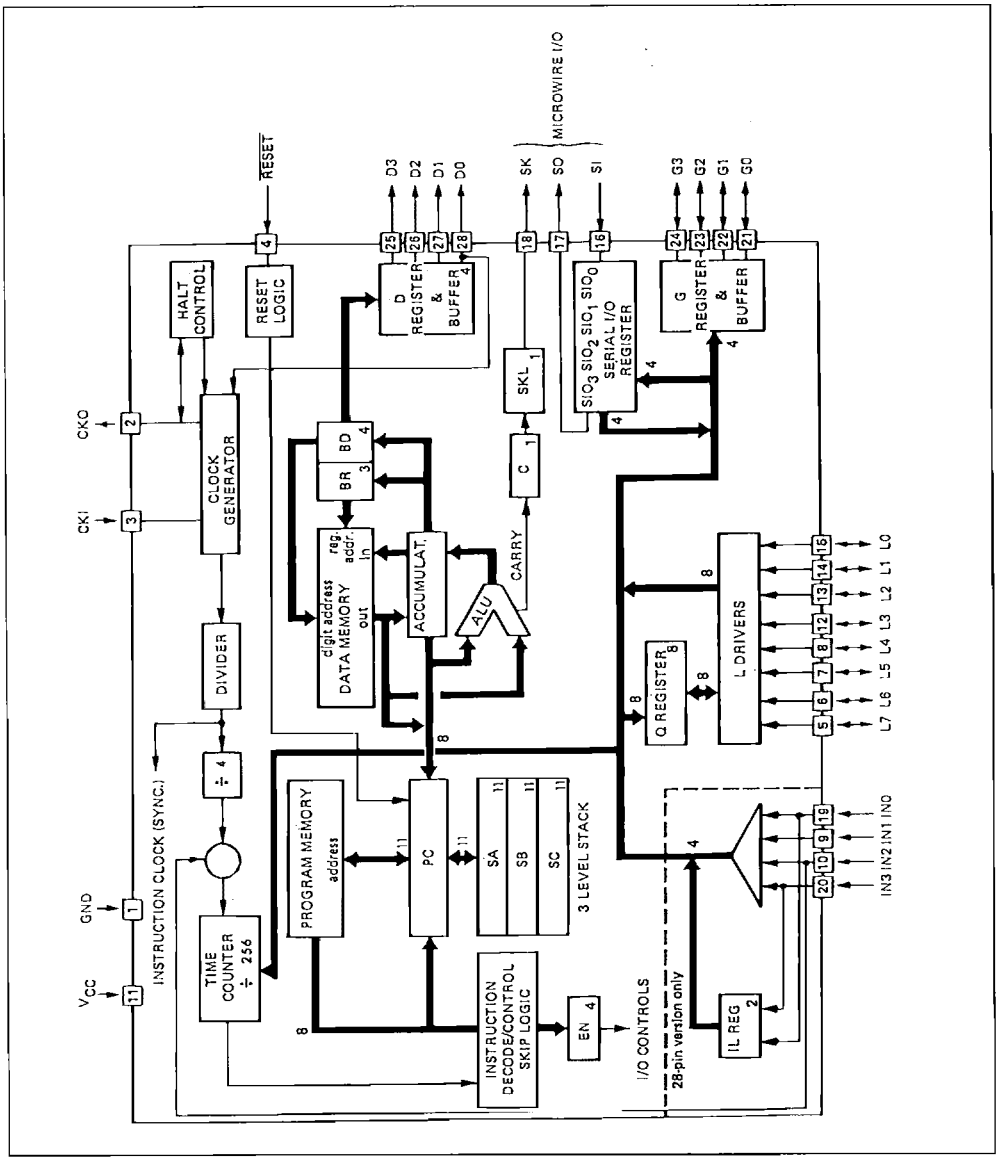
Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD

data manipulation. The ETC9420, C9444 are 28-pin chips. The ETC9421, C9445 are 24-pin versions (4 inputs removed) and C9422 is a 20-pin version with 15 I/O lines.

Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized microcontroller at a low end-product cost.

These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

Figure 1 : Block Diagram (28-pin version).



ETC9420/ETC9421/ETC9422/ET9444/ETC9445

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (V_{CC})	6	V
V_I	Voltage at any Pin	- 0.3 to V_{CC} + 0.3	V
	Total Allowable Source Current	25	mA
	Total Allowable Sink Current	25	mA
T_{op}	Operating Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C
T_L	Lead Temperature (soldering 10 seconds)	300	°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (note 5)	Peak to Peak		$0.1V_{CC}$	V
Supply Current (note 1)	V_{CC} = 2.4V, t_c = 64µs		120	µA
	V_{CC} = 5.0V, t_c = 16µs		700	µA
	V_{CC} = 5.0V, t_c = 4µs		3000	µA
	(tc = instruction cycle time)			
Halt Mode Current (note 2)	V_{CC} = 5.0V, Fin = 0kHz		40	µA
	V_{CC} = 2.4V, Fin = 0kHz		12	µA
Input Voltage Levels				
RESET, CKI (RC or crystal opt.)				
Do (clock input)				
Logic High		$0.9V_{CC}$		V
Logic Low			$0.1V_{CC}$	V
All Other Inputs				
Logic High		$0.7V_{CC}$		
Logic Low			$0.2V_{CC}$	V
Input Pull-up Current	V_{CC} = 4.5V, V_{IN} = 0	30	330	µA
Hi-Z Input Leakage		− 1	+ 1	µA
Input Capacitance (note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 5%			
Logic High	I_{OH} = − 100µA	2.7		V
Logic Low	I_{OL} = 400µA		0.4	V
CMOS Operation				
Logic High	I_{OH} = − 10µA	V_{CC}–0.2		V
Logic Low	I_{OL} = 10µA		0.2	V
Output Current Levels (except CKO)				
Sink (note 6)	V_{CC} = 4.5V, V_{out} = V_{CC}	1.2		mA
	V_{CC} = 2.4V, V_{out} = V_{CC}	0.2		mA
Source (standard option)	V_{CC} = 4.5V, V_{out} = 0V	0.5		mA
	V_{CC} = 2.4V, V_{out} = 0V	0.1		mA
Source (low current option)	V_{CC} = 4.5V, V_{out} = 0V	30	330	µA
	V_{CC} = 2.4V, V_{out} = 0V	6	80	µA
CKO Current Level (as clock out)				
Sink ÷ 4	V_{CC} = 4.5V, CKI = V_{CC}, V_{OUT} = V_{CC}	0.3		mA
÷ 8		0.6		mA
÷ 16		1.2		mA
Source ÷ 4	V_{CC} = 4.5V, CKI = 0V, V_{OUT} = 0	0.3		mA
÷ 8		0.6		mA
÷ 16		1.2		mA
Allowable Sink Source Current Per Pin (note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current needed to over-ride HALT (note 3) To continue	V_{CC} = 4.5V, Vin = $0.2V_{CC}$		0.7	mA
To halt	V_{CC} = 4.5V, Vin = $0.7V_{CC}$		1.6	mA
TRI-STATE or Open Drain Leakage Current		− 2.5	+ 2.5	µA

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Instruction Cycle Time (tc)	$V_{CC} \geq 4.5V$	4	DC	µs
	$4.5V > V_{CC} \geq 2.4V$	16	DC	µs
Operating CKI Frequency ÷ 4 Mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷ 8 Mode		DC	2.0	MHz
÷ 16 Mode		DC	4.0	MHz
÷ 4 Mode	$4.5V > V_{CC} \geq 2.4V$	DC	250	kHz
÷ 8 Mode		DC	500	kHz
÷ 16 Mode		DC	1.0	MHz
Duty Cycle (note 4)	F1 = 4MHz	40	60	%
Rise Time (note 4)	F1 = 4MHz Ext. Dock		60	ns
Fall Time (note 4)	F1 = 4MHz Ext. Dock		40	ns
Instruction Cycle Time (RC oscillator) (note 4)	R = 30k, V_{CC} = 5V C = 82pF (÷ 4 mode)	8	16	µs
INPUTS (fig. 3)				
t_{SETUP}	G Inputs	tc/4 = + 0.7		µs
	SI Input ($V_{CC} \geq 4.5V$)	0.3		µs
	All Others	1.7		µs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		µs
	$4.5V > V_{CC} \geq 2.4V$	1.0		µs
OUTPUT PROPAGATION DELAY	V_{out} = 1.5V, CL = 100pF, R_L = 5K			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	µs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \geq 2.4V$		4.0	µs
MICROBUS® TIMING	CL = 50pF, V_{CC} = 5V ± 5%			µs
Read Operation (fig. 4)				
Chip select stable before $\overline{RD}$ - t_{CSR}		65		ns
Chip select hold time for $\overline{RD}$ - t_{RCS}		20		ns
$\overline{RD}$ pulse width - t_{RR}		400		ns
Data Delay from $\overline{RD}$ - t_{RD}			375	ns
$\overline{RD}$ to data floating - t_{DF} (note 4)			250	ns
Write Operation (fig. 5)				
Chip select stable before $\overline{WR}$ - t_{CSW}		65		ns
Chip select hold time for $\overline{WR}$ - t_{WCS}		20		ns
$\overline{WR}$ pulse width - t_{WW}		400		ns
Data set-up time for $\overline{WR}$ - t_{DW}		320		ns
Data Hold Time for $\overline{WR}$ - t_{WD}		100		ns
INTR Transition Time for $\overline{WR}$ - t_{WI}			700	ns

Notes :
1. Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17.
2. The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.
3. When forcing HALT, current is only needed for a short time (approx. 200ns) to flip the HALT flip-flop.
4. This parameter is only sampled and not 100% tested.
5. Voltage change must be less than 0.5V in a 1ms period.
6. SO output sink current must be limited to keep V_{OL} below $0.2V_{CC}$ when port is running in order to prevent entering test mode

ETC9320, ETC9321, ETC9322–ETC9344, ETC9345

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (V_{CC})	6	V
V_i	Voltage at any Pin	– 0.3 to V_{CC} + 0.3	V
	Total Allowable Source Current	25	mA
	Total Allowable Sink Current	25	mA
T_{op}	Operating Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature (soldering 10 seconds)	300	°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are note insured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C (unless otherwise specified)

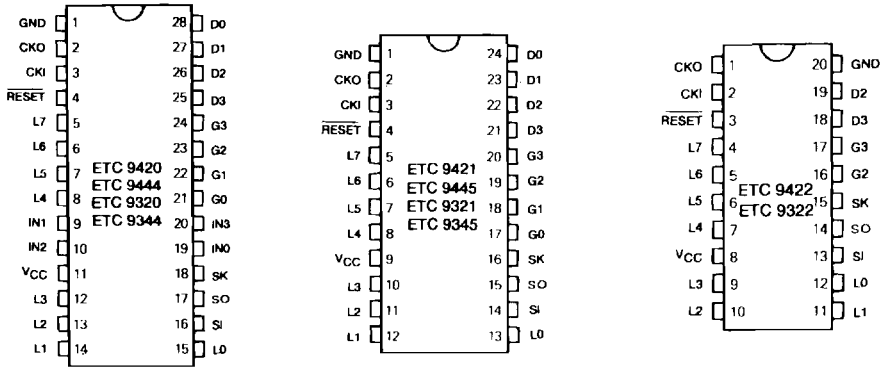
Parameter	Test Conditions	Min.	Max.	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple (note 5)	Peak to Peak		$0.1V_{CC}$	V
Supply Current (note 1)	V_{CC} = 3.0V, t_c = 64µs		180	µA
	V_{CC} = 5.0V, t_c = 16µs		800	µA
	V_{CC} = 5.0V, t_c = 4µs		3600	µA
	(tc = instruction cycle time)			
Halt Mode Current (note 2)	V_{CC} = 5.0V, Fin = 0kHz		60	µA
	V_{CC} = 3.0V, Fin = 0kHz		30	µA
Input Voltage Levels				
$\overline{RESET}$, CKI (RC or crystal opt.)				
Do (clock input)				
Logic High		$0.9V_{CC}$		V
Logic Low			$0.1V_{CC}$	V
All Other Inputs				
Logic High		0.7		
Logic Low			$0.2V_{CC}$	V
Input Pull-up Current	V_{CC} = 4.5V, V_{IN} = 0	30	440	µA
Hi-Z Input Leakage		– 2	+ 2	µA
Input Capacitance (note 4)			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 5%			
Logic High	I_{OH} = – 100µA	2.7		V
Logic Low	I_{OL} = 400µA		0.4	V
CMOS Operation				
Logic High	I_{OH} = – 10µA	V_{CC}–0.2		V
Logic Low	I_{OL} = 10µA		0.2	V
Output Current Levels (except CKO)				
Sink (note 6)	V_{CC} = 4.5V, V_{out} = V_{CC}	1.2		mA
	V_{CC} = 3.0V, V_{out} = V_{CC}	0.2		mA
Source (standard option)	V_{CC} = 4.5V, V_{out} = 0V	0.5		mA
	V_{CC} = 3.0V, V_{out} = 0V	0.1		mA
Source (low current option)	V_{CC} = 4.5V, V_{out} = 0V	30	440	µA
	V_{CC} = 3.0V, V_{out} = 0V	8	200	µA
CKO Current Level (as clock out)				
Sink ÷ 4	V_{CC} = 4.5V, CKI = V_{CC}, V_{out} = V_{CC}	0.3		mA
÷ 8		0.6		mA
÷ 16		1.2		mA
Source ÷ 4	V_{CC} = 4.5V, CKI = 0V, V_{out} = 0V	0.3		mA
÷ 8		0.6		mA
÷ 16		1.2		mA
Allowable Sink/source Current Per Pin (note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current needed to over-ride HALT (note 3) To continue	V_{CC} = 4.5V, Vin = $0.2V_{CC}$		0.9	mA
To halt	V_{CC} = 4.5V, Vin = $0.7V_{CC}$		2.1	mA
TRI-STATE or Open Drain Leakage Current		– 5	+ 5	µA

AC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Units
Instruction Cycle Time (tc)	$V_{CC} \geq 4.5V$	4	DC	µs
	$4.5V > V_{CC} \geq 3.0V$	16	DC	µs
Operating CKI Frequency ÷ 4 Mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷ 8 Mode		DC	2.0	MHz
÷ 16 Mode		DC	4.0	MHz
÷ 4 Mode	$4.5V > V_{CC} \geq 3.0V$	DC	250	kHz
÷ 8 Mode		DC	500	kHz
÷ 16 Mode		DC	1.0	MHz
Duty Cycle (note 4)	F1 = 4MHz	40	60	%
Rise Time (note 4)	F1 = 4MHz Ext. Clock		60	ns
Fall Time (note 4)	F1 = 4MHz Ext. Clock		40	ns
Instruction Cycle Time (RC oscillator) (note 4)	R = 30k, V_{CC} = 5V, C = 82pF (÷ 4 mode)	8	16	µs
INPUTS (fig. 3)				
t_{SETUP} G Inputs	$V_{CC} \geq 4.5V$	(tc/4) + .7		µs
t_{SETUP} SI Input	$V_{CC} \geq 4.5V$	0.3		µs
t_{SETUP} All Others	$V_{CC} \geq 4.5V$	1.7		µs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		µs
t_{HOLD}	$4.5V > V_{CC} \geq 3.0V$	1.0		µs
OUTPUT PROPAGATION DELAY	V_{out} = 1.5V, CL = 100pF, RL = 5k			
t_{pD1}, t_{pD0}	$V_{CC} \geq 4.5V$		1.0	µs
t_{pD1}, t_{pD0}	$4.5V > V_{CC} \geq 3.0V$		4.0	µs
MICROBUS® TIMING	C_L = 50pF, V_{CC} = 5V ± 5%			
Read Operation (fig. 4)				
Chip select stable before $\overline{RD}$ - t_{CSR}		65		ns
Chip select hold time for $\overline{RD}$ - t_{RCS}		20		ns
$\overline{RD}$ pulse width - t_{RR}		400		ns
Data Delay from $\overline{RD}$ - t_{RD}			375	ns
$\overline{RD}$ to data floating - t_{DF} (note 4)			250	ns
Write Operation (fig. 5)				
Chip select stable before $\overline{WR}$ - t_{CSW}		65		ns
Chip select hold time for $\overline{WR}$ - t_{WCS}		20		ns
$\overline{WR}$ pulse width - t_{WW}		400		ns
Data set-up time for $\overline{WR}$ - t_{DW}		320		ns
Data Hold Time for $\overline{WR}$ - t_{WD}		100		ns
INTR Transition Time for $\overline{WR}$ - t_{WI}			700	ns

Notes :
1. Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17.
2. The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions : all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all output low and tied to ground.
3. When forcing HALT, current is only needed for a short time (approx. 200ns) to flip the HALT flip-flop.
4. This parameter is only sampled and not 100% tested.
5. Voltage change must be less than 0.5 volt in a 1ms period.
6. SO output sink current must be limited to keep V_{OL} below 0.2V_{CC} when port is running in order to prevent entering test mode.

Figure 2 : Pins Connections.



Pin	Description
L_7-L_0	8 Bit Bidirectional I/O Ports with TRI-STATE®
G_3-G_0	4 Bit Bidirectional I/O Ports
D_3-D_1	3 Bit General Purpose Outputs
D_0	General Purpose Output or Oscillator Input
IN_3-IN_0	4-bit Input Port (ETC9420 or 9444 only)
SI	Serial Input
SO	Serial Output
SK	Logic-controlled Clock or general purpose output
CKI	System Oscillator Input
CKO	Crystal Oscillator Output (or general purpose input or halt I/O port)
$\overline{\text{RESET}}$	System Reset Input
V_{CC}	Power Supply
GND	Ground

FUNCTIONAL DESCRIPTION

For ease of reading only theETC9420/9421/9422/ 9444/9445 are referenced. However, all such references apply equally to ETC9320/9321/9322/ 9344/9345.

The internal structure is shown in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" when it is reset, it is a logic "0".

PROGRAM MEMORY

Program Memory consists of ROM, 1024 bytes for the ETC9420/C9421, C9422 and 2048 bytes for the ETC9444/C9445. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC

register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the ETC9444/C9445 organized as 8 data registers of 16 x 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the ETC9420/C9421/C9422, organized as 4 data registers of 16 x 4 bits digits. The B register is 6 bits long. Upper 2 bis (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch, to input 4 bits of a ROM word. L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes depending on a mask-programmable option : as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *figure 10a.*

Four general-purpose inputs, IN3-IN0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode, D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for MICROBUS applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (see LEI instruction). With the MICROBUS® option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS® option allows L I/O port data to be latched into the Q register.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS Instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL ; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "O".

The "EN register is an internal 4-bit register loaded under programm control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

0. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN_0 set, SIO is as asynchronous binary counter, DECREMENTING its value by one upon each low going pulse ("1" to "0") occuring on the SI input. Each pulse must be at least 2 (two) instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant

bit of SIO, SO can be enabled to output the most significant bit of SIO each instruction cycle time. The SK output SKL ANDed with the instruction cycle clock.

1. With EN_1 set interrupt is enabled. Immediatly following an interrupt, EN_1 is reset to disable further interrupts.
2. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high impedance input state.
3. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected), SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected, disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

Figure 3 : Input/Output Timing Diagrams (divide-by-8 mode).

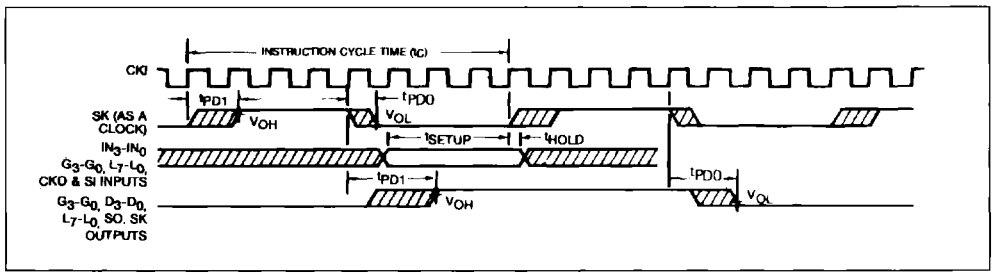


Figure 4 : Microbus Read Operation Timing.

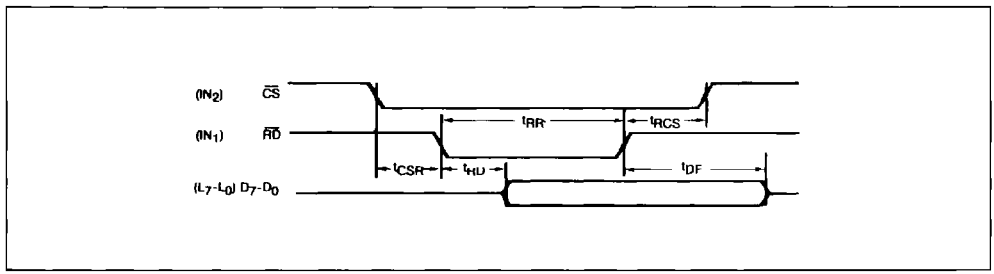
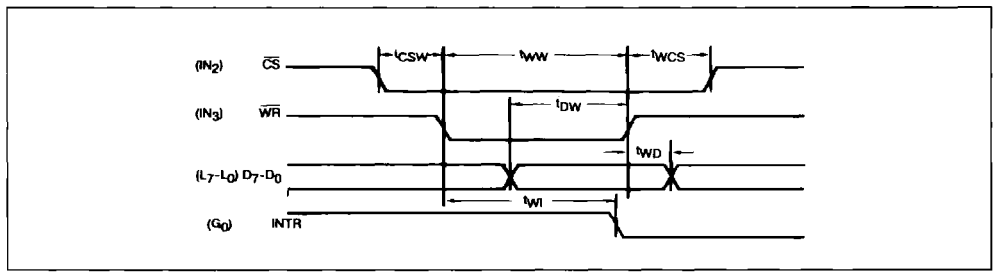


Figure 5 : Microbus Write Operation Timing.



FUNCTIONAL DESCRIPTION (continued)

Table 1 : Enable Register Modes - Bits EN_0 AND EN_3

EN_0	EN_3	SIO	SI	SO	SK after XAS
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 1, SK = 0
0	1	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = clock If SKL = 1, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address OFF (the last word of page 3) and EN_1 is reset.

b. An interrupt will be acknowledged only after the following conditions are met :

   1. EN_1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. ALL successive transfer of control instructions and successive LBI_s have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon "popping" of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address OFF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. **Subroutines should not be nested within the interrupt servicing routine** since their "popping" of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The first instruction at hex address OFF must be a NOP.

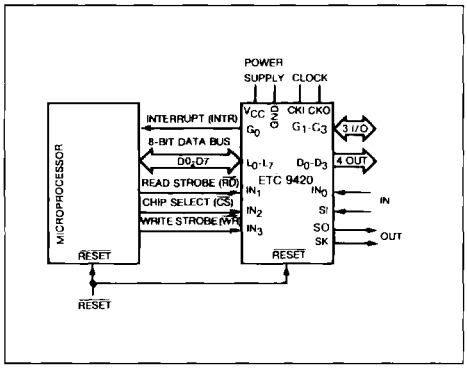
e. A LEI instruction may be put immediately before the RET to re-enable interrupts.

MICROBUS INTERFACE

The ETC9420/C9444 has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (µP). IN_1, IN_2 and IN_3 general purposes input become **MICROBUS INTERFACE** read-strobe, chip-select, and write-strobe lines, respectively IN_1 become $\overline{RD}$ - a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the µP becomes $\overline{CS}$ - a logic "0" on this line selects the ETC9420/C9444 as the µP IN_2 peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components IN_3 becomes $\overline{WR}$ - a logic "0" on this line will write bus data from the L ports to the Q latches for input to the ETC9420/C9444 G_0 becomes INTR, a "ready" output, reset by a write pulse from the µP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the ETC9420/C9444.

This option has been designed for compatibility with MICROBUS a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication). The functioning and timing relationships between the signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (figure 4 and 5). Connection of the ETC9420/C9444 to the MICROBUS is shown in figure 6.

Figure 6 : Microbus ® Option Interconnect.

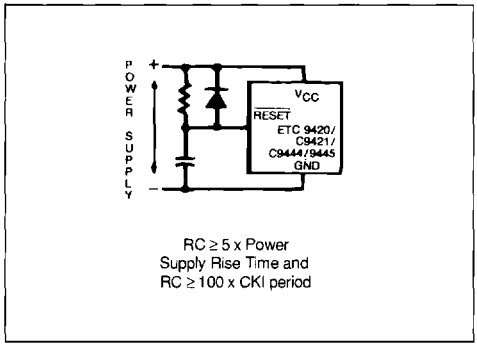


INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1ms and if the operating frequency at CKI is greater than 32kHz, otherwise the external RC network shown in figure 7 must be connected to the RESET pin. The RESET pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, providing it stays low for at least three instruction cycle times.

Note : If CKI clock is less than 32kHz, the internal-reset logic (option = 29 = 1) must be disabled and the external RC circuit must be used.

Figure 7 : Power-up Clear Circuit.



Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL Latch is set, this enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

TIMER

There are two modes selected by mask option :

a. Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset.

   For example, using a 4MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250kHz increments the 10-bit timer every 4µs. By presetting the counter and detecting overflow, accurate timeouts between 16µs (4 counts) and 4.096ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

b. External event counter. In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

   Note : The IT instruction is not allowed in this mode.

HALT MODE

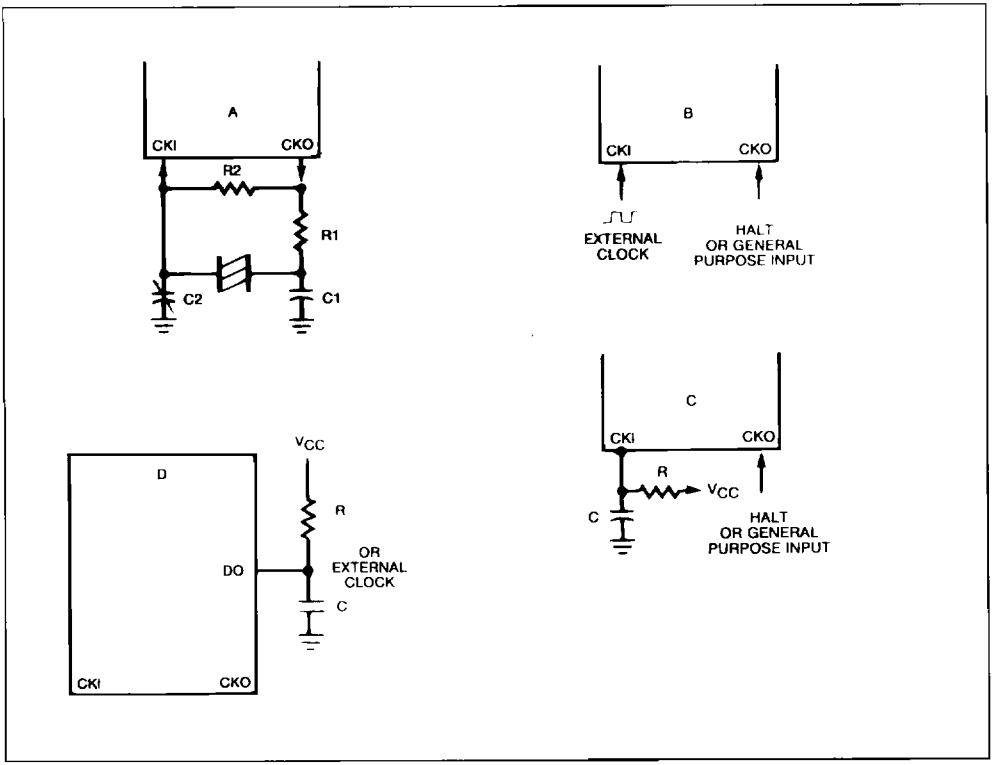
The ETC9420/9421/C9422/C9444/C9445 is a FULLY STATIC circuit ; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may be also halted by the HALT instruction or by forcing CKO high when it is used as an HALT/I/O port. Once in the HALT mode, the internal circuitry does not receive any clocksignal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of the two different methods.

1. Continue function - by forcing CKO low, if it is mask-programmed as an HALT I/O port, the system clock is reenabled and the circuit continues to operate from the point where it was stopped.
2. Restart - by forcing the RESET pin low (see initialization).

The HALT mode is the minimum power dissipation state.

Note : If the user has selected dual clock with D0 as external oscillator (option 30 = 2) AND the ETC9444/C9420 is running with the D0 clock, the HALT mode - either hardware or software - will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.

Figure 8 : Oscillator Components Values.



R/C CONTROLLED OSCILLATOR

R	C	Cycle Time	V_{CC}
15k	82pF	4 to 9µs	≥ 4.5V
30k	82pF	8 to 16µs	≥ 4.5V
60k	100pF	16 to 32µs	2.4 to 4.5V

Note : 15k ≤ R ≤ 150k ; 50pF ≤ C ≤ 150pF

CRYSTAL OR RESONATOR

Crystal Value	Component Values			
	R1	R2	C1(pF)	C2(pF)
32kHz	220k	20M	30	6.36
455kHz	5k	10M	80	40
2.086MHz	2k	1M	30	6.36
4.0MHz	1k	1M	30	6.36

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

BLOCK DIAGRAMS

Figure 9a : Halt Mode -Two Pin Oscillator.

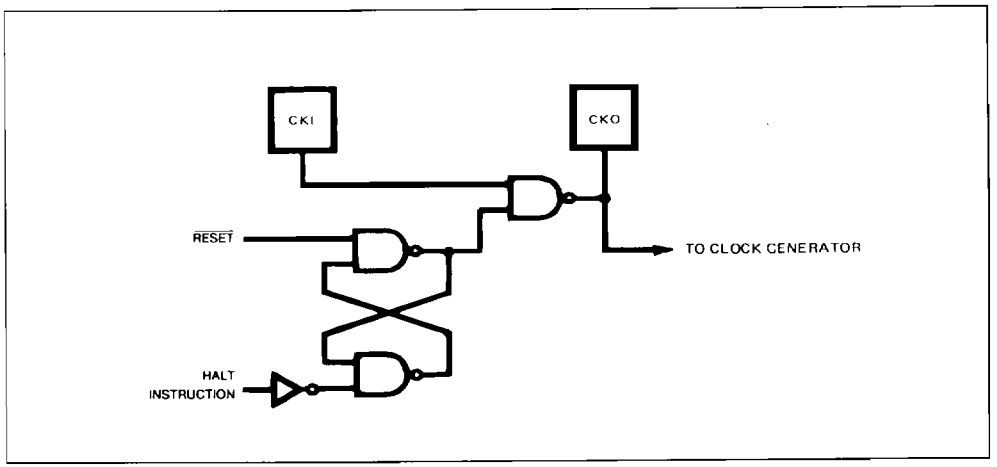
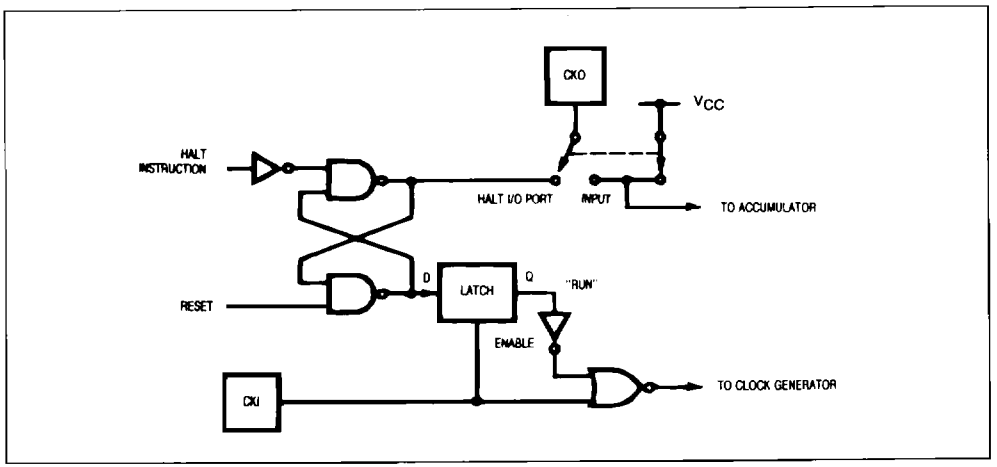


Figure 9b : Halt Mode - One Pin Oscillator.



BLOCK DIAGRAMS

Figure 9a : Halt Mode -Two Pin Oscillator.

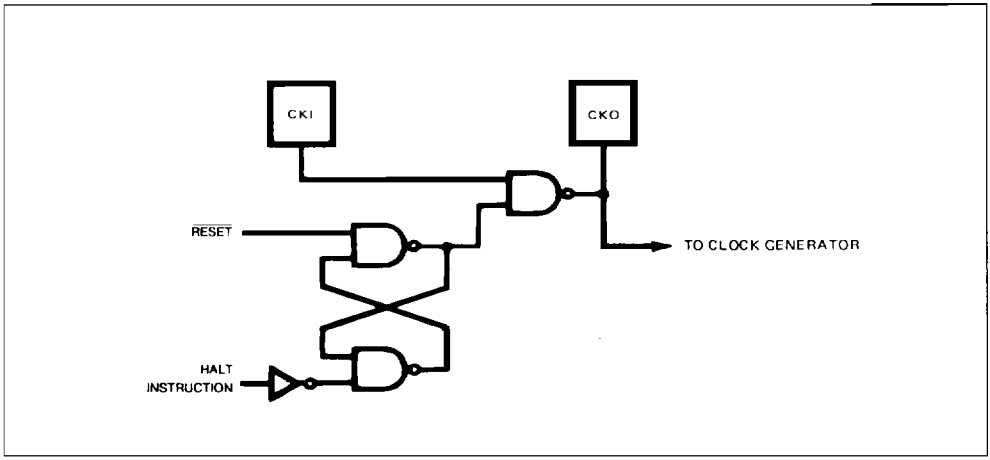


Figure 9b : Halt Mode - One Pin Oscillator.

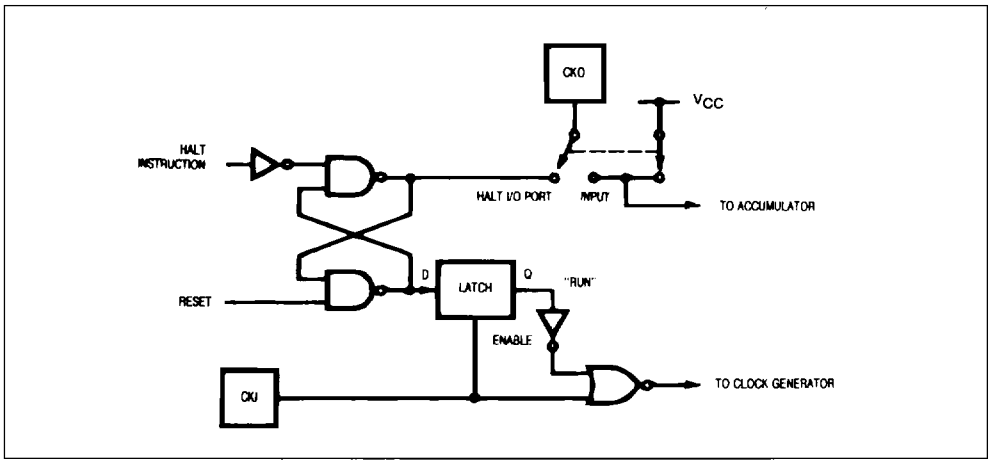


Figure 10a : Clock and Timer Block Diagram without Dual-clock.

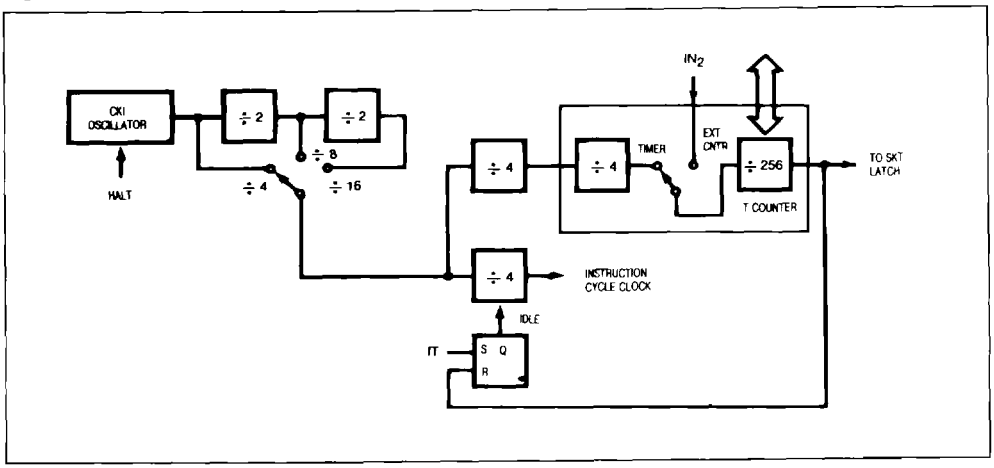
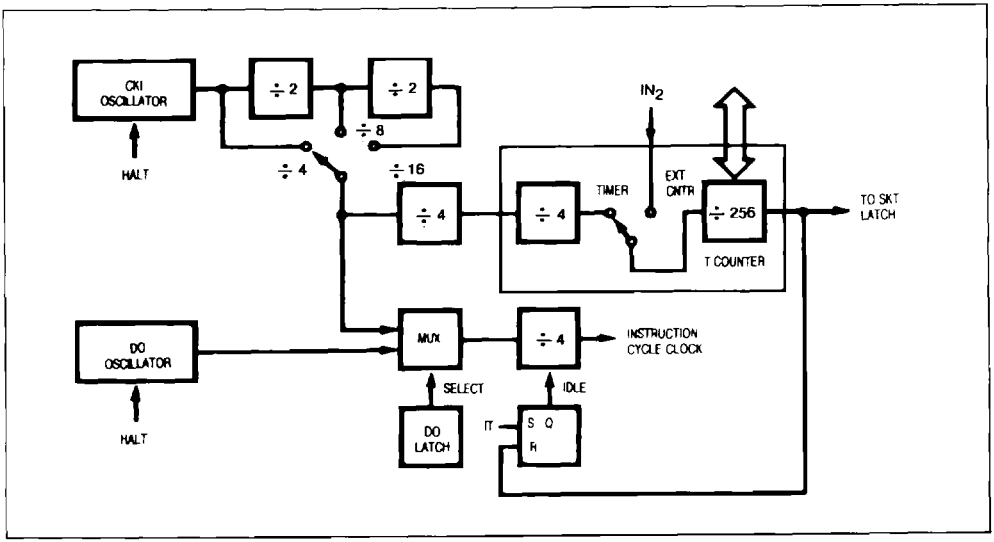


Figure 10b : Clock and Timer Block Diagram without Dual-clock.



INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

Table 2 : Instruction Set Table Symbols.

INTERNAL ARCHITECTURE SYMBOLS

Symbol	Definition
A	4-bit Accumulator
B	7-bit RAM Address Register (6-bit for ETC9420)
Br	Upper 3 Bits of B (register address) (2-bit for ETC9420)
Bd	Lower 4 Bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit General Purpose I/O Port
IL	Two 1-Bit (IN_0 and IN_3) latches.
IN	4-bit Input Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM addressed by B.
PC	11-bit ROM address program counter.
Q	8-bit latch for L port.
SA, SB, SC	11-bit 3-level subroutine stack.
SIO	4-bit Shift Register and Counter
SK	Logic-controlled Clock Output
SKL	1-bit lach for SK output.
T	8-bit Timer

INSTRUCTION OPERAND SYMBOLS

Symbol	Definition
d	4-bit Operand Field, 0-15 Binary (RAM digit select)
r	3(2)-bit Operand Field, 0-7(3) Binary (RAM register select)
a	11-bit Operand Field, 0-2047 (1023)
y	4-bit Operand Field, 0-15 (immediate data)
RAM(x)	RAM addressed by variable x.
ROM(x)	ROM addressed by variable x.

OPERATIONAL SYMBOLS

Symbol	Definition
+	Plus
–	Minus
→	Replaces
‹ ›	Is exchanged with.
=	Is equal to.
$\overline{A}$	One's complement of A.
⊕	Exclusive-or
:	Range of Values

Table 3 : ETC9444/C9420 Instruction Set.

ARITHMETIC INSTRUCTIONS

Mnem	Operand	Hx Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ASC		30	0011 0000	A + C RAM(B) → A Carry → C	Carry	Add with CARRY Skip on Carry
ADD		31	0011 0001	A + RAM(B) → A	None	Add RAM to A
ADT		4A	0100 1010	A + 10_{10} → A	None	Add TEN TO A
AISC	y	5-	0101 y	A + y → A	Carry	Add Immediate Skip on Carry (y ≠ 0)
CASC		10	0001 0000	$\overline{A}$ + RAM(B) + C → A	Carry	Complement and Add with
				Carry → C		Carry Skip on Carry
CLRA		00	0000 0000	0 → A	None	Clear A
COMP		40	0100 0000	$\overline{A}$ → A	None	Ones Complement of A to A
NOP		44	0100 0100	None	None	No Operation
RC		32	0011 0010	0 → C	None	Reset C
SC		22	0010 0010	1 → C	None	Set C
XOR		02	0000 0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

TRANSFER OF CONTROL INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
JID		FF	1111 1111	ROM ($PC_{10:8}$ A, M) → $PC_{7:0}$	None	Jump Indirect (note 3)
JMP	a	6–	0110 0 $a_{10:8}$ $a_{7:0}$	a → PC	None	Jump
JP	a		1 $a_{6:0}$ (pages 2,3 only) or 11 $a_{5:0}$ (all other pages)	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (note 4)
JSRP	a		10 $a_{5:0}$	PC + 1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (note 5)
JSR	a	6–	0110 1 $a_{10:8}$ $a_{7:0}$	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	0100 1000	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 1001	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 38	0011 0011 0011 1000		None	HALT Processor
IT		33 39	0011 0011 0011 1001		None	IDLE Till Timer Overflows then continues.

MEMORY REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAMT		33 3F	0011 0011 0011 1111	A → $T_{7:4}$ RAM (B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33 2F	0011 0011 0010 1111	$T_{7:4}$ → RAM (B) $T_{3:0}$ → A	None	Copy T to RAM, A (note 9)
CAMQ		33 3C	0011 0011 0011 1100	A → $Q_{7:4}$ RAM (B) → $Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0011 0011 0010 1100	$Q_{7:4}$ → RAM (B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
LD	r	-5	00 r 0101 (r – 0:3)	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r.d	23	0010 0011 0 r d	RAM (r.d) → A	None	Load A with RAM pointed to directly by r.d.
LQID		BF	1011 1111	ROM ($PC_{10:8A:M}$) → Q SA → SB	None	Load Q Indirect (note 3)
RMB	0 1 2 3	4C 45 42 43	0100 1100 0100 0101 0100 0010 0100 0011	0 → RAM $(B)_0$ 0 → RAM $(B)_1$ 0 → RAM $(B)_2$ 0 → RAM $(B)_3$	None	Reset RAM Bit

MEMORY REFERENCE INSTRUCTIONS (continued)

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SMB	0 1 2 3	4D 47 46 4B	0 1 0 0 | 1 1 0 1 0 1 0 0 | 0 1 1 1 0 1 0 0 | 0 1 1 0 0 1 0 0 | 1 0 1 1	$1 \rightarrow RAM\ (B)_0$ $1 \rightarrow RAM\ (B)_1$ $1 \rightarrow RAM\ (B)_2$ $1 \rightarrow RAM\ (B)_3$	None	Set RAM Bit
STII	y	7-	0 1 1 1 | y	$y \rightarrow RAM\ (B)$ $Bd \oplus 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	-6	0 0 | r | 0 1 1 0 (r = 0:3)	$RAM\ (B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r.d	23	0 0 1 0 | 0 0 1 1 1 | r | d	$RAM\ (r.d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r.d
XDS	r	–7	0 0 | r | 0 1 1 1 (r = 0:3)	$RAM\ (B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus \rightarrow Br$	Bd Decrements Past 0	Exchange RAM with A and Decrement Bd, Exclusive-Or Br with r
XIS	r	–4	0 0 | r | 0 1 0 0 (r = 0:3)	$RAM\ (B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd Increments Past 15	Exchange RAM with A and Increment Bd, Exclusive-Or Br with r

REGISTER REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAB		50	0 1 0 1 | 0 0 0 0	$A \rightarrow Bd$	None	Copy A to Bd
CBA		4E	0 1 0 0 | 1 1 1 0	$Bd \rightarrow A$	None	Copy Bd to A
LBI	r.d	33	0 0 | r | (d-1) (r = 0:3) (d = 0.9:15) or 0 0 1 1 | 0 0 1 1 1 | r | d (any r, any d)	$r.d \rightarrow B$	Skip until not a LBI	Load B Immediate with r.d (note 6)
LEI	y	33 6-	0 0 1 1 | 0 0 1 1 0 1 1 0 | y	$y \rightarrow EN$	None	Load EN Immediate (note 7)
XABR		12	0 0 0 1 | 0 0 1 0	$A \leftrightarrow Br$	None	Exchange A with Br (note 8)

TEST INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SKC		20	0010|0000		C = "1"	Skip if C is true.
SKE		21	0010|0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011|0011 0010|0001		$G_{3:0} = 0$	Skip if G is zero (all 4 bits).
SKGBZ		33	0011|0011	1st Byte		Skip if G Bit is zero.
	0	01	0000|0001	2nd Byte	$G_0 = 0$	
	1	11	0001|0001		$G_1 = 0$	
	2	03	0000|0011		$G_2 = 0$	
	3	13	0001|0011		$G_3 = 0$	

TEST INSTRUCTIONS (continued)

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SKMBZ	0	01	0000|0001		$RAM(B)_0 = 0$	Skip if RAM Bit is zero.
	1	11	0001|0001		$RAM(B)_1 = 0$	
	2	03	0000|0011		$RAM(B)_2 = 0$	
	3	13	0001|0011		$RAM(B)_3 = 0$	
SKT		41	0100|0001		A time-base counter carry has occured since last test.	Skip on Timer (note 3)

INPUT/OUTPUT INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ING		33 2A	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 1 0	G → A	None	Input G Ports to A
ININ		33 28	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 0 0	IN → A	None	Input IN Inputs to A (note 2)
INIL		33 29	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 0 0 1	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (note 3)
INL		33 2E	0 0 1 1 | 0 0 1 1 0 0 1 0 | 1 1 1 0	$L_{7:4}$ → RAMB(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 1 1 0	Bd → D	None	Output Bd to D Outputs
OGI	y	33 5–	0 0 1 1 | 0 0 1 1 0 1 0 1 | y	y → G	None	Output to G Ports Immediate
OMG		33 3A	0 0 1 1 | 0 0 1 1 0 0 1 1 | 1 0 1 0	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0 1 0 0 | 1 1 1 1	A ↔ SIO, C → SKL	None	Exchange A with SIO (note 3)

Notes :

1. All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g. Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register
2. The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.
3. For additional on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.
4. The JP instruction allows a jump, while in subroutine page 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3.The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.
5. A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4-bits of P). A JSRP may not be used when in pages 2 or 3 JSRP may not jump to the last word in page 2.
6. LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).
7. Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit (See Functional Description, EN Register).
8. For 2K ROM devices A→Br (0→A3) For 1K ROM devices A→Br (0.0→A3, A2)
9. Do not use CTMA instruction when dual - option is selected and part is running from D0 Clocks.

DESCRIPTION OF SELECTED INSTRUCTIONS

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1→SA→SB→SC) and replaces the least significant 8 bits of the PC as follows : A→PC (7:4), RAM(B)→PC (3:0), leaving PC (10), PC (9) and PC (8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC→SB→SA→PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB→SC, the previous contents of SC are lost.

Note : LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10, PC9 and PC8 are not affected by JID.

Note : JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note : If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter :

CAMT : load T counter

SKT : skip if overflow flag is set and reset it

NOP

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. Upon overflow, the processor will restart with a delay shorter than one cycle time. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is mask-programmed as an external event counter (option # 31 = 1).

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occured on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO INTO A2. If CKO has not been so programmed, a "1" will be placed in A2. A0 is input into A1. IL latches are cleared on reset. IL latches are not available on the ETC9445/C9421.

INSTRUCTION SET NOTES

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example : a JP Located in the last word of a

page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note : The ETC9420/C9421/C9422 needs only 10 bits to address its ROM. Therefore, the eleventh bit (10) is ignored.

POWER DISSIPATION

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, a 500kHz crystal input will typical draw 100µA more than a square-wave input. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the ETC9444/C9445 operating current drain.

$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$

where I_{CO} = chip operating current drain in microamps

I_Q = quiescent leakage current (from curve)

Fi = CKI frequency in MegaHertz

V = Chip V_{CC} in volts

Dv = divide by option selected

For example at 5 volts V_{CC} and 400kHz (divide by 4)

$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$

$I_{CO} = 20 + 80 + 700 = 800\mu A$

At 2.4 volts V_{CC} and 30kHz (divide by 4)

$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$

$I_{CO} = 6 + 2.88 + 25.2 = 34.08\mu A$

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation :

$I_{ci} = I_Q + V \times 40 \times Fi$

For example, at 5 volts V_{CC} and 400kHz

$I_{ci} = 20 + 5 \times 40 \times 0.4 = 100\mu A$

The total average current will then be the weighted average of the operation current and the idle current :

$$I_{ta} = I_{CO} \times \frac{To}{To + Ti} + I_{ci} \times \frac{Ti}{To + Ti}$$

where I_{ta} = total average current

I_{CO} = operating current

I_{ci} = idle current

To = operating time

Ti = idle time

I/O OPTIONS

ETC9444/C9445 outputs have the following optional configurations, illustrated in *figure 11* :

a. Standard - A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current - This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain - An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Output - A CMOS output buffer similar to a. witch may be disabled by program control.

e. Low-Current TRI-STATE L Output - This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output - This has the N-channel device to ground only.

All inputs have the following options :

g. Input with on chip load device to V_{CC}.

h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available : Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given *in figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.

Figure 11 : Input/Output Configurations.

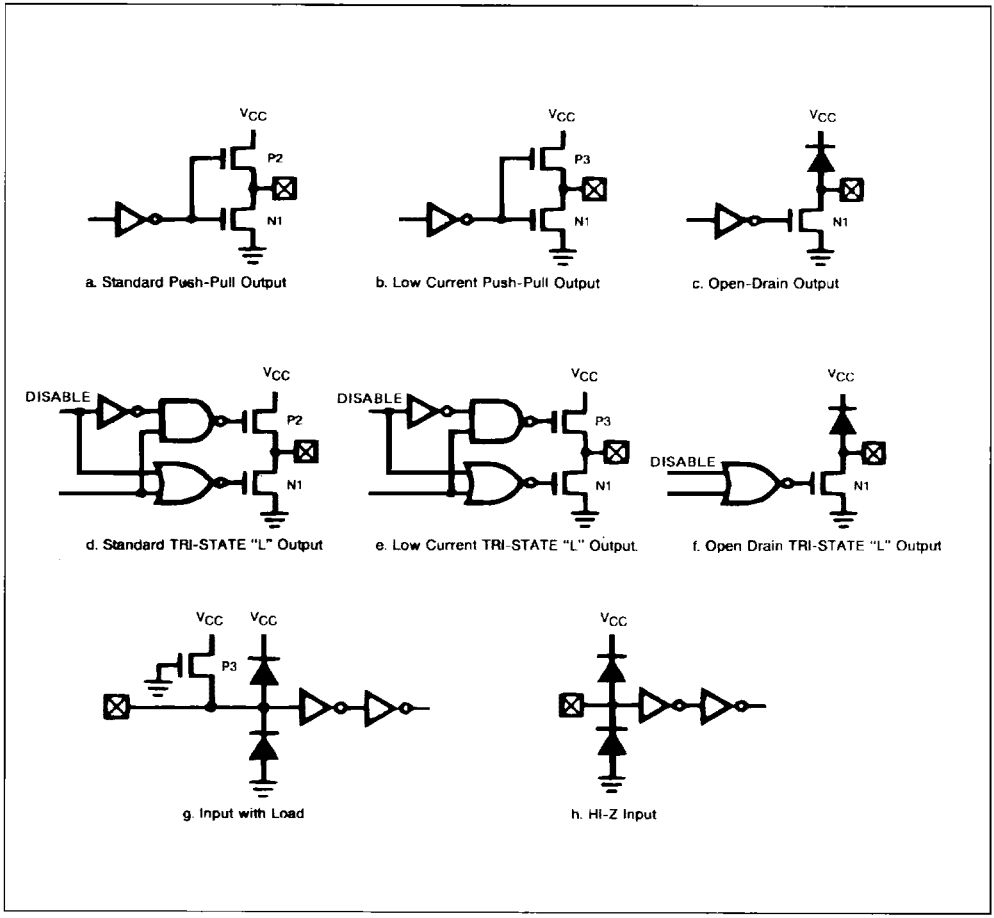
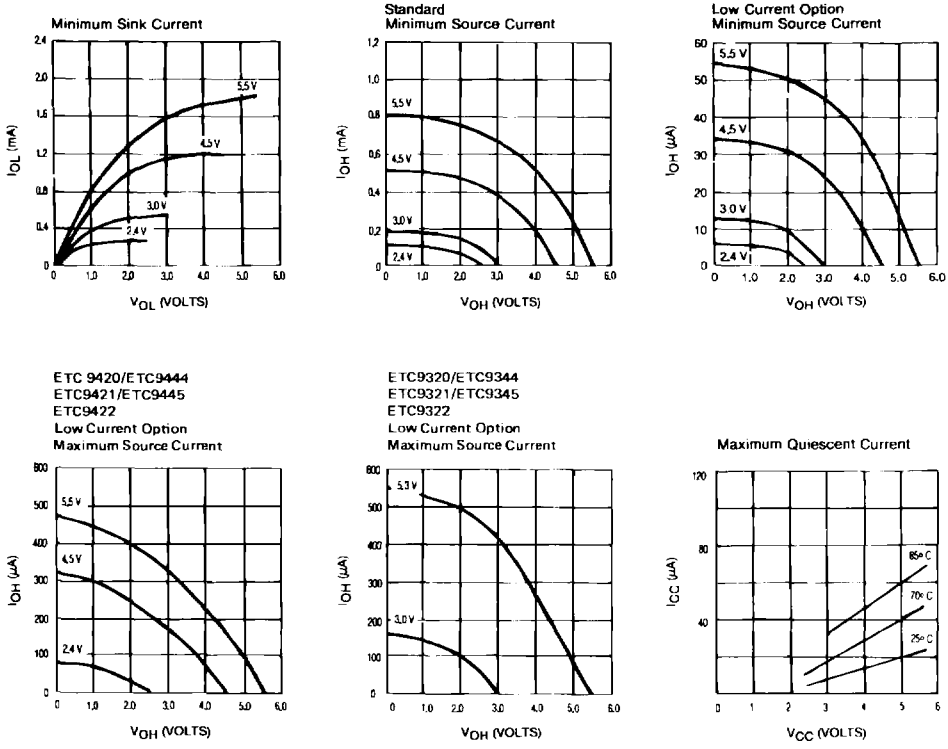


Figure 12 : Input/Output Characteristics.



OPTION LIST

The ETC9444/C9420/C9445/C9421/C9422 mask-programmable options are assigned numbers which correspond with the ETC9344/C9320/C9345/ C9321/C9322 pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0 : Ground Pin - no option available.

Option 2 : CKO Pin
- = 0 : clock generator output to crystal/resonator
- = 1 : HALT I/O port
- = 2 : general purpose input with load device to V_{CC}
- = 3 : general purpose input, high-Z

Option 3 : CKI input
- = 0 : Crystal controlled oscillator input divide by 4
- = 1 : Crystal controlled oscillator input divide by 8
- = 2 : Crystal controlled oscillator input divide by 16
- = 4 : Single-pin RC controlled oscillator (divide by 4)
- = 5 : External oscillator input divide by 4
- = 6 : External oscillator input divide by 8
- = 7 : External oscillator input divide by 16

Option 4 : $\overline{\text{RESET}}$ input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 5 : L7 Driver
- = 0 : Standard TRI-STATE push-pull output
- = 1 : Low-current TRI-STATE push-pull output
- = 2 : Open-drain TRI-STATE output

Option 6 : L6 Driver - (same as option 5)

Option 7 : L5 Driver - (same as option 5)

Option 8 : L4 Driver - (same as option 5)

Option 9 : IN1 input
- = 0 : load device to V_{CC}
- = 1 : Hi-Z input

Option 10 : IN2 input - (same as option 9)

Option 11 = 0 : V_{CC} Pin - no option available

Option 12 : L3 Driver - (same as option 5)

Option 13 : L2 Driver - (same as option 5)

Option 14 : L1 Driver - (same as option 5)

Option 15 : L0 Driver - (same as option 5)

Option 16 : SI Input - (same as option 9)

Option 17 : SO Driver
- = 0 : Standard push-pull output
- = 1 : Low-current push-pull output
- = 2 : Open-Drain output

Option 18 : SK Driver - (same as option 17)

Option 19 : IN0 Input - (same as option 9)

Option 20 : IN3 Input - (same as option 9)

Option 21 : G0 I/O Port - (same as option 17)

Option 22 : G1 I/O Port - (same as option 17)

Option 23 : G2 I/O Port - (same as option 17)

Option 24 : G3 I/O Port - (same as option 17)

Option 25 : D3 Output - (same as option 17)

Option 26 : D2 Output - (same as option 17)

Option 27 : D1 Output - (same as option 17)

Option 28 : D0 Output - (same as option 17)

Option 29 : Internal Initialization Logic
- = 0 : Normal operation
- = 1 : No internal initialization logic

Option 30 : Dual Clock
- = 0 : Normal operation
- = 1 : Dual Clock. D0 RC oscillator (opt. # 28 must = 2)
- = 2 : Dual Clock. D0 ext. clock input

Option 31 : Timer
- = 0 : Time-base counter
- = 1 : External event counter

Option 32 : MICROBUS
- = 0 : Normal
- = 1 : MICROBUS (opt. #31 must = 0)

Option 33 : Chip bonding
(1K and 2K Microcontroller)
- = 0 : 28 - pin package
- = 1 : 24 - pin package
- = 2 : Same die purchased in both 24 and 28 pin version

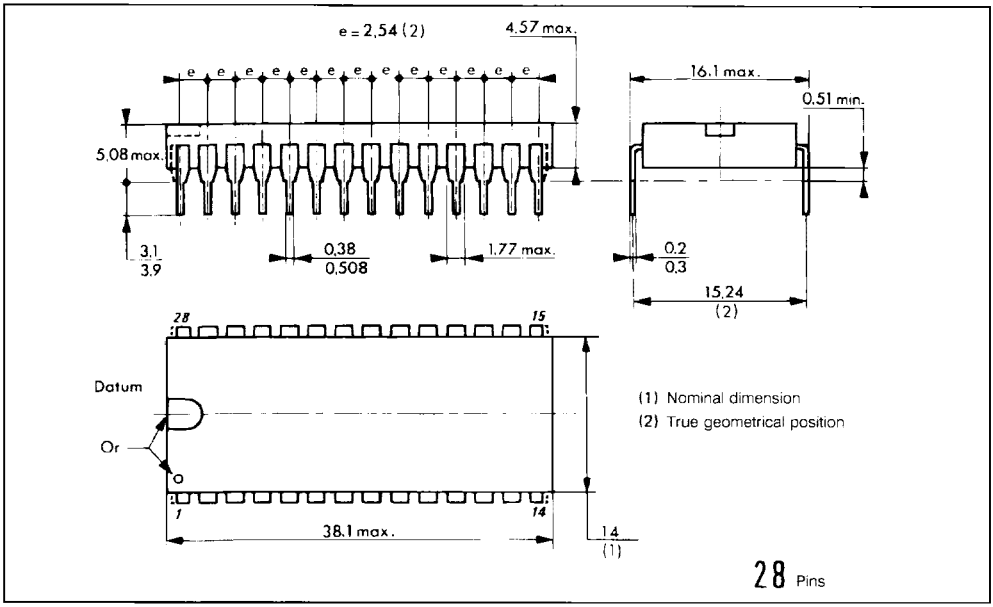
(1K Microcontroller only)
- = 3 : 20 - pin package
- = 4 : 28- and 20- pin package
- = 5 : 24- and 20- pin package
- = 6 : 28-, 24- and 20- pin package

Note : If opt # 33 = 2 then opt # 9, 10, 19, 20 and 32 must = 0

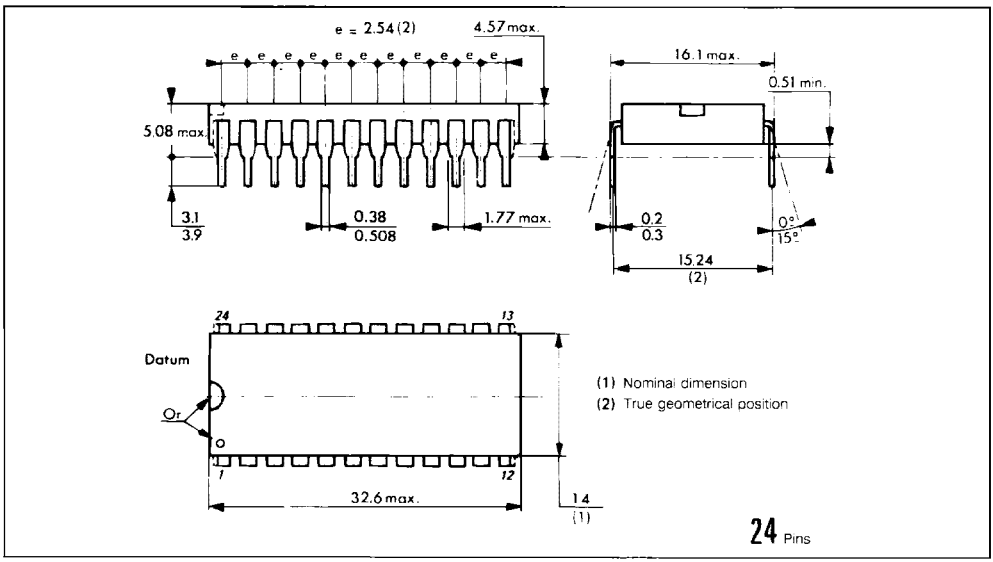
If opt # 33 = 3, 4, 5 or 6 then opt # 9, 10, 19, 20, 21, 22, 30 and 32 must = 0.

PACKAGE DIMENSIONS

28 PINS – PLASTIC PACKAGE



24–PINS – PLASTIC PACKAGE



PACKAGE DIMENSIONS (continued)

20 PINS – PLASTIC PACKAGE