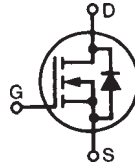


Polar™ Power MOSFET IXFP12N50PM

HiPerFET™

(Electrically Isolated Tab)

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



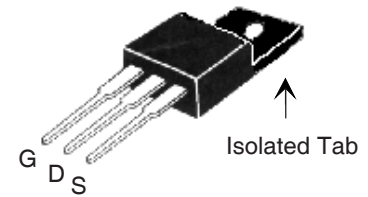
$$V_{DSS} = 500V$$

$$I_{D25} = 6A$$

$$R_{DS(on)} \leq 500m\Omega$$

$$t_{rr} \leq 300ns$$

OVERMOLDED TO-220
(IXFP...M) OUTLINE



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$; $R_{GS} = 1 M\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	6	A
I_{DM}	$T_C = 25^\circ C$, pulse width limited by T_{JM}	30	A
I_A	$T_C = 25^\circ C$	12	A
E_{AS}	$T_C = 25^\circ C$	600	mJ
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J = 150^\circ C$	10	V/ns
P_D	$T_C = 25^\circ C$	50	W
T_J		- 55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		- 55 ... +150	$^\circ C$
T_L	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ C$
T_{SOLD}	Plastic body for 10 s	260	$^\circ C$
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		2.5	g

Features

- Plastic overmolded tab for electrical isolation
- International standard package
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect

Advantages

- Easy to mount
- Space savings

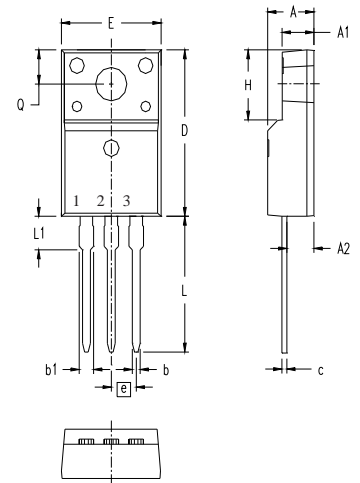
Symbol	Test Conditions ($T_J = 25^\circ C$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1mA$	3.0		5.5 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$ $T_J = 125^\circ C$			5 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 6A$, Note 1			500 m Ω

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 6\text{A}$, Note 1	7.5	13	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		1830	pF
C_{oss}			182	pF
C_{rss}			16	pF
$t_{d(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 6\text{A}$ $R_G = 10\Omega$ (External)		22	ns
t_r			27	ns
$t_{d(off)}$			65	ns
t_f			20	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 6\text{A}$		29	nC
Q_{gs}			11	nC
Q_{gd}			10	nC
R_{thJC}				2.5 $^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified)		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			12 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			48 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 6\text{A}$, $-di/dt = 150\text{A}/\mu\text{s}$, $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$			300 ns
Q_{RM}			2.8	μC
I_{RM}			18.2	A

ISOLATED TO-220 (IXFP...M)



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
$\varnothing P$.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

Notes: 1. Pulse test, $t \leq 300 \mu\text{s}$; duty cycle, $d \leq 2\%$.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics
@ 25°C

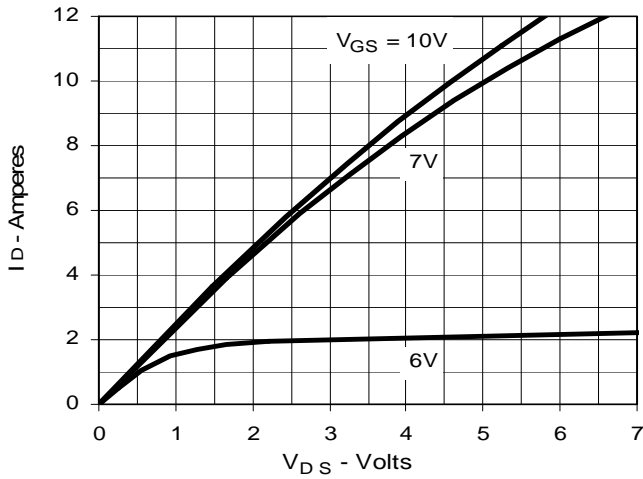


Fig. 2. Extended Output Characteristics
@ 25°C

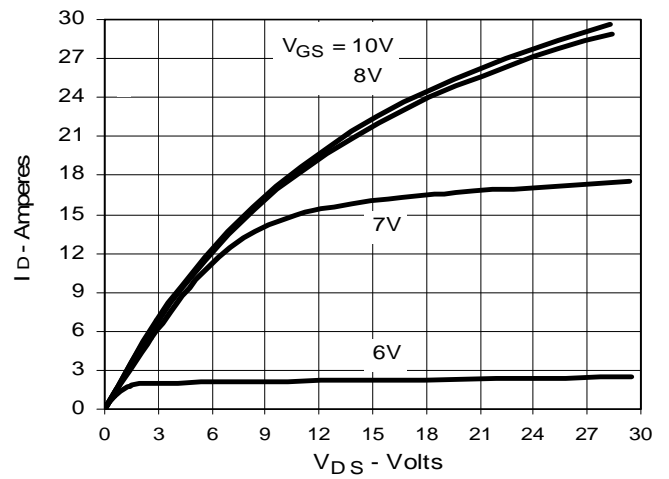


Fig. 3. Output Characteristics
@ 125°C

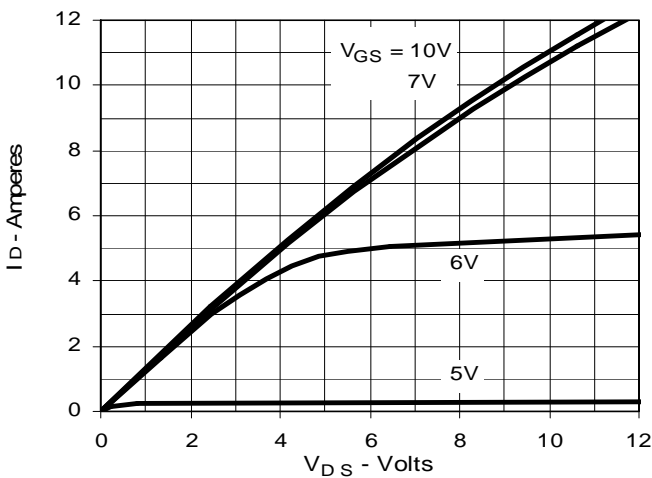


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 6A$ Value vs. Junction Temperature

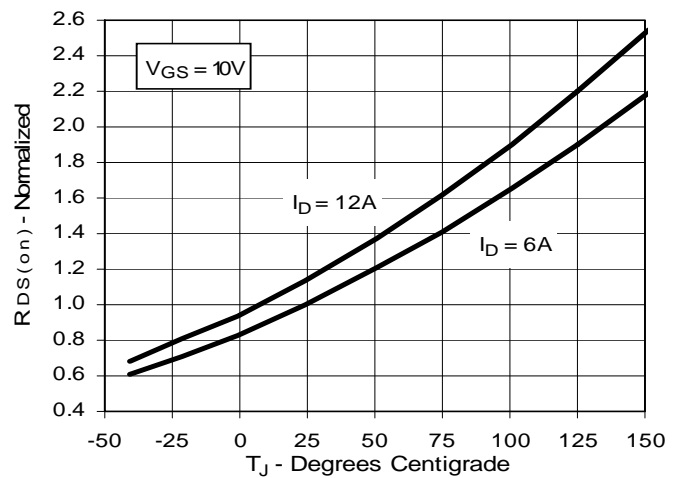


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 6A$ Value vs. Drain Current

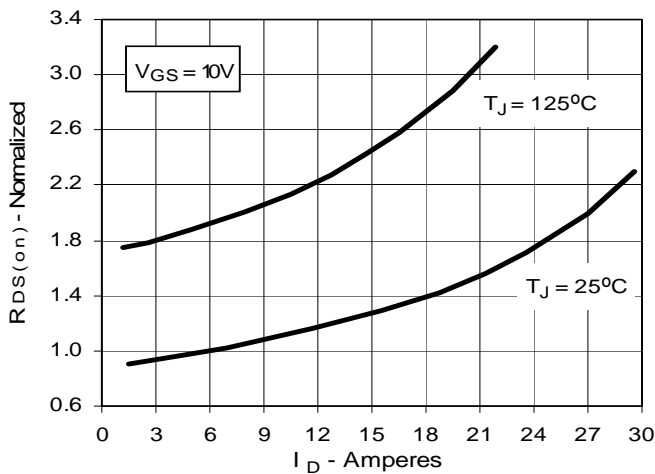


Fig. 6. Drain Current vs. Case Temperature

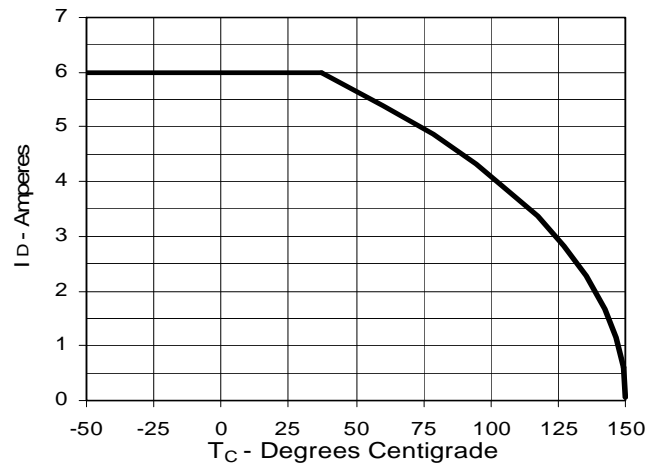


Fig. 7. Input Admittance

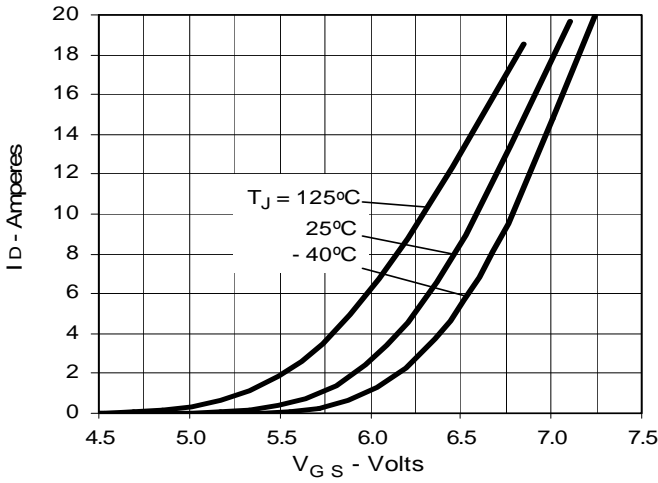


Fig. 8. Transconductance

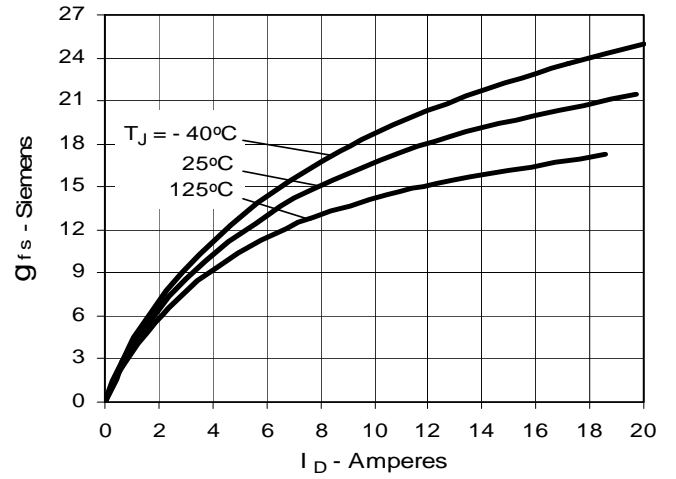


Fig. 9. Source Current vs. Source-To-Drain Voltage

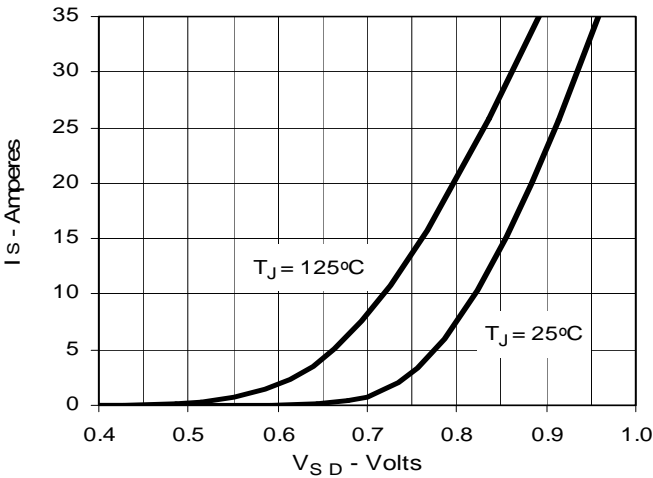


Fig. 10. Gate Charge

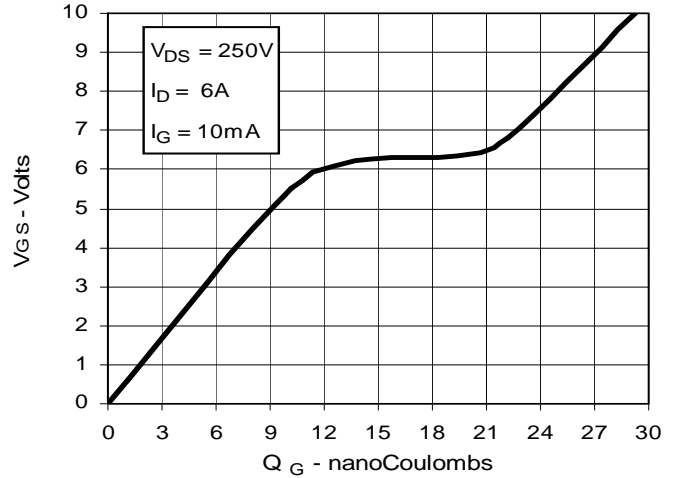


Fig. 11. Capacitance

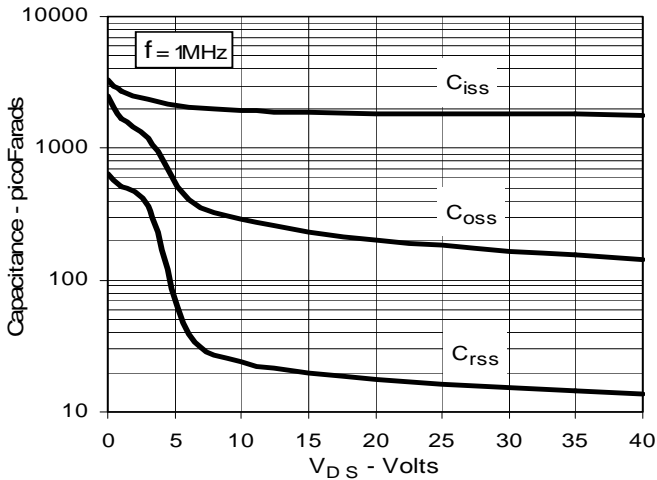


Fig. 12. Forward-Bias Safe Operating Area

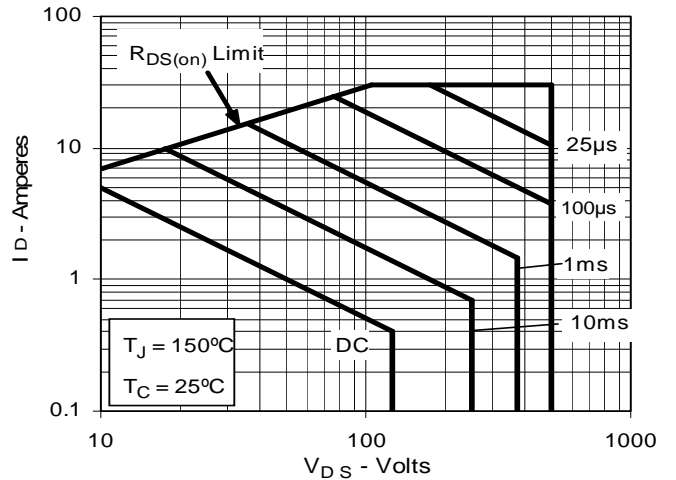


Fig. 13. Maximum Transient Thermal Impedance

