MP04xxx590

Dual Thyristor, Thyristor/Diode Module

Replaces October 2001 version, DS5371-3.1

DS5371-4.0 August 2003

FEATURES

- Dual Device Module
- Electrically Isolated Package
- Pressure Contact Construction
- International Standard Footprint
- Alumina (Non Toxic) Isolation Medium
- Integral Water Cooled Heatsink

APPLICATIONS

- Motor Control
- Controlled Rectifier Bridges
- Heater Control
- AC Phase Control

VOLTAGE RATINGS

Type Number	Repetitive Peak Voltages V_{DRM} V_{RRM} V_{DSM} V	Conditions
MP04xxx590-18 MP04xxx590-16 MP04xxx590-14	1800 1600 1400	T_{vj} = –40˚ to 125˚C, I_{DRM} = I_{RRM} = 50mA V_{DRM} = V_{RRM} = V_{DSM} V_{RSM} = V_{DRM} + 100V

Lower voltage grades available.

ORDERING INFORMATION

Order As:

MP04HBT590-18 or **MP04HBT-16** or **MP04HBT14**

MP04HBP590-18 or **MP04HBP-16** or **MP04HBP14**

MP04HBN590-18 or **MP04HBN-16** or **MP04HBN14**

Note: When ordering, please use the whole part number.

KEY PARAMETERS

V_{DRM}	**1800V**
$I_{T(AV)}$	**595A**
$I_{TSM(per\ arm)}$	**16800A**
V_{isol}	**3000V**

Code	Circuit
HBT	
HBP	
HBN	

Fig.1 Circuit diagrams

Module type code: MP04.
For further information see Package Details.

Fig. 2 Module outline

ABSOLUTE MAXIMUM RATINGS - PER ARM

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

Symbol	Parameter	Test Conditions		Max.	Units
V_{DRM}	Repetitive peak on-state voltage	T_{vj} = –40˚C to 125˚C		1800	V
V_{RRM}	Repetitive peak reverse voltage	T_{vj} = –40˚C to 125˚C		1800	V
V_{RSM}	Non-repetitive peak on-state voltage	T_{vj} = –40˚C to 125˚C		1800	V
V_{DSM}	Non-repetitive peak reverse voltage	T_{vj} = +25˚C to 125˚C		1900	V
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	T_{case} = 75˚C	595	A
			T_{case} = 85˚C	505	A
$I_{T(RMS}$	RMS value	T_{case} = 75˚C		935	A
I_{TSM}	Surge (non-repetitive) on-current	8.3ms half sine, T_j = 125˚C		16.8	kA
I^2t	I^2t for fusing	V_R = 0		1411 X 10^3	A^2s
I_{TSM}	Surge (non-repetitive) on-current	8.3ms half sine, T_j = 125˚C		13.5	kA
I^2t	I^2t for fusing	V_R = 50% V_{DRM}		911 X 10^3	A^2s
I_{TSM}	Surge (non-repetitive) on-current	10ms half sine, T_j = 125˚C		15.7	kA
I^2t	I^2t for fusing	V_R = 0		1232 X 10^3	A^2s
I_{TSM}	Surge (non-repetitive) on-current	10ms half sine, T_j = 125˚C		12.6	kA
I^2t	I^2t for fusing	V_R = 50% V_{DRM}		794 X 10^3	A^2s
V_{isol}	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz		3000	V

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	dc	-	0.056	˚C/kW
	(per thyristor or diode)	Half wave	-	0.060	˚C/kW
		3 Phase	-	0.066	˚C/kW
$R_{th(c-hs)}$	Thermal resistance - case to heatsink (per thyristor or diode)	Mounting torque = 5Nm with mounting compound	-	0.02	˚C/kW
T_{vj}	Virtual junction temperature	Reverse (blocking)	-	125	˚C
T_{OP} / T_{stg}	Operating and storage temperature range	-	–40	125	˚C
-	Screw torque	Mounting - M6	-	6 (35)	Nm (lb.ins)
		Electrical connections - M10	-	12 (106)	Nm (lb.ins)
-	Weight (nominal)	-	-	1580	g

DYNAMIC CHARACTERISTICS - THYRISTOR

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_j = 125˚C	-	50	mA
dV/dt	Linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125˚C	-	1000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1500A, gate source 1.5A, t_r = 0.5µs, T_j = 125˚C	-	500	A/µs
$V_{T(TO)}$	Threshold voltage	At T_{vj} = 125˚C. See note 1	-	0.85	V
r_T	On-state slope resistance	At T_{vj} = 125˚C. See note 1	-	0.38	mΩ

Note 1: The data given in this datasheet with regard to forward voltage drop is for calculation of the power dissipation in the semiconductor elements only. Forward voltage drops measured at the power terminals of the module will be in excess of these figures due to the impedance of the busbar from the terminal to the semiconductor.

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	3.5	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	200	mA
V_{GD}	Gate non-trigger voltage	At V_{DRM}, T_{case} = 125°C	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage	-	5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	10	A
P_{GM}	Peak gate power	See table fig. 5	150	W
$P_{G(AV)}$	Mean gate power	-	10	W

CURVES

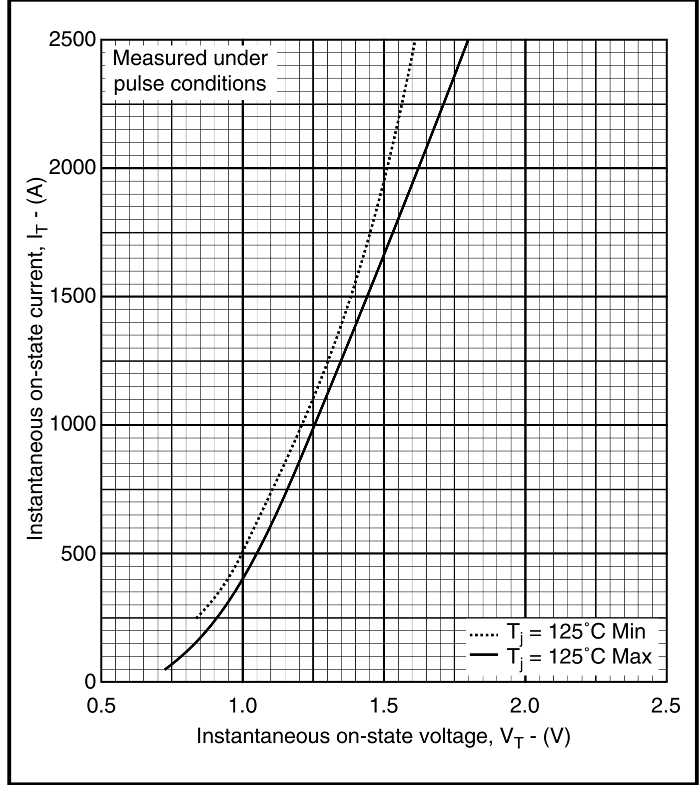

Fig. 3 Maximum (limit) on-state characteristics

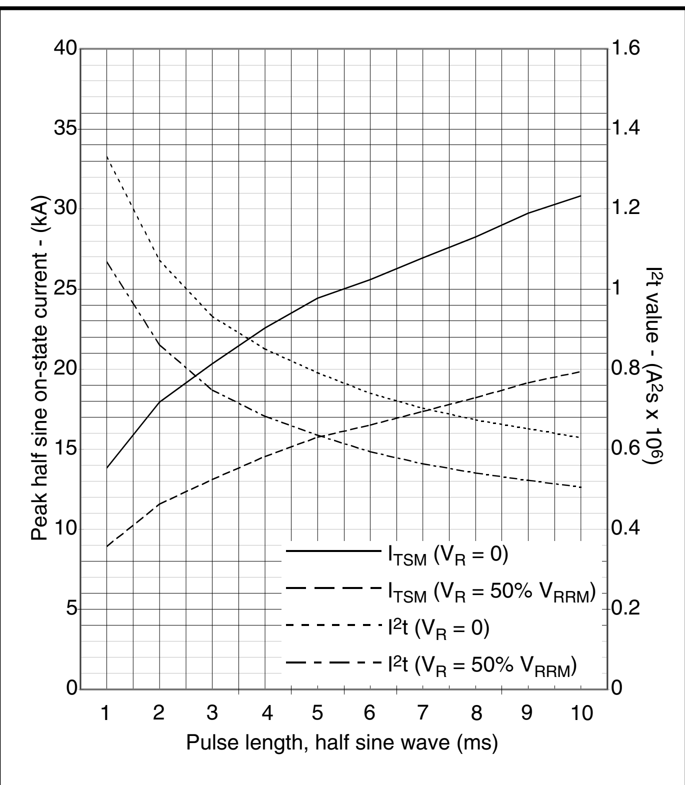

Fig. 4 Sub-cycle surge curves

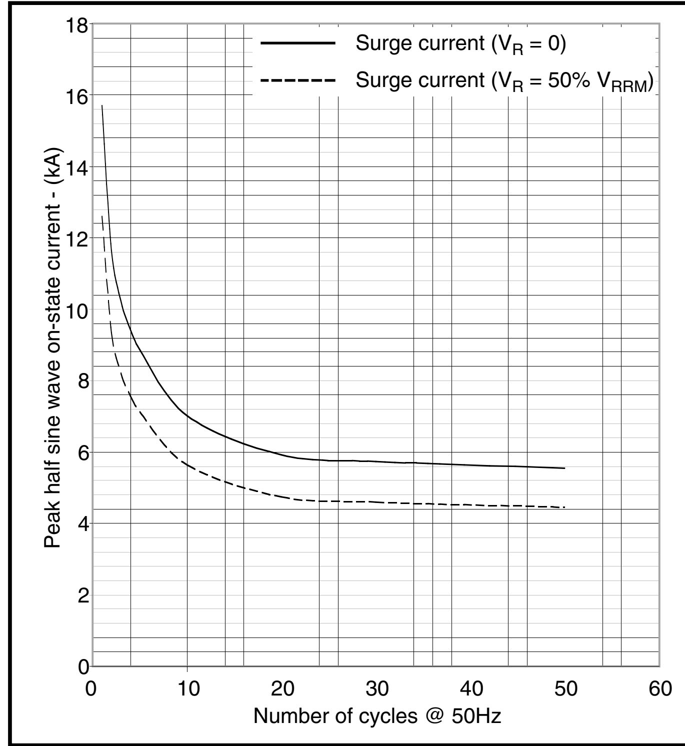

Fig. 5 Sub-cycle surge curves

Table gives pulse power P_{GM} in Watts

Pulse width µs	Frequency Hz 50	100	400
100	150	150	150
200	150	150	125
500	150	150	100
1ms	150	100	25
10ms	20	-	-

Gate trigger voltage, V_{GT} - (V)

Gate trigger current, I_{GT} - (A)

I_{FGM}

V_{GD}

Upper limit 99%

Lower limit 99%

T_j = 125°C

T_j = 25°C

T_j = -40°C

Region of certain triggering

5W 10W 20W 50W 100W

100 10 1 0.1

0.001 0.01 0.1 1 10

Fig. 6 Gate characteristics

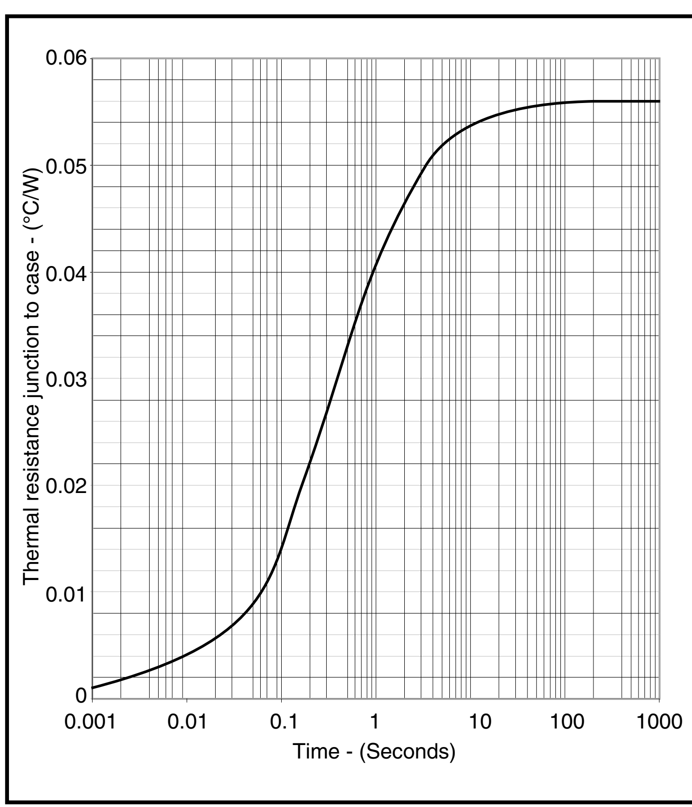

Fig. 7 Transient thermal impedance - dc

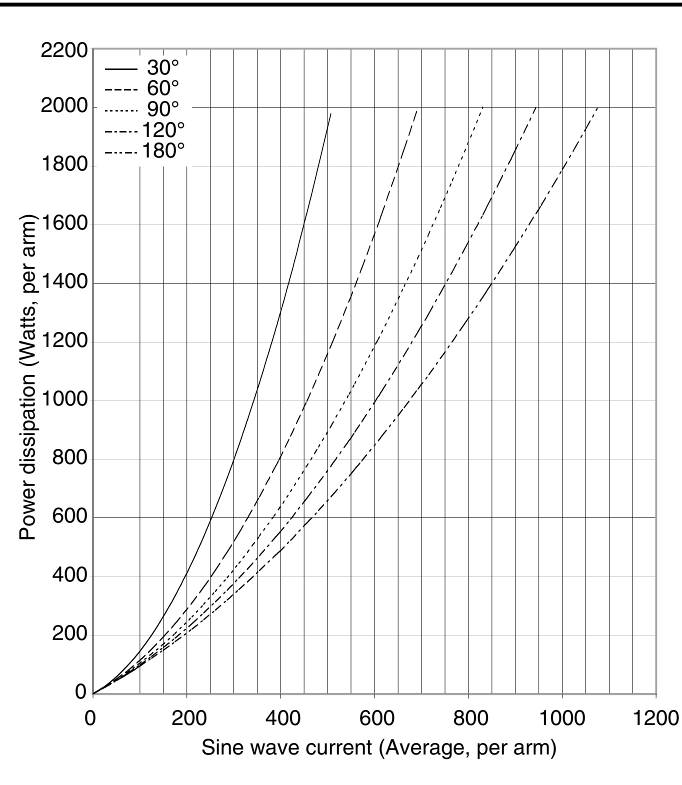

Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, sine wave 50/60Hz

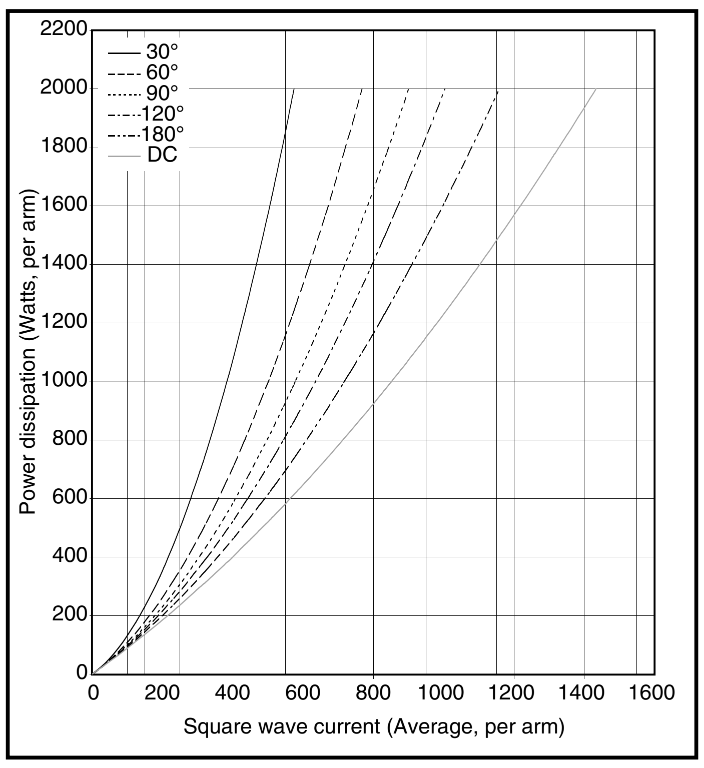

Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, square wave 50/60Hz

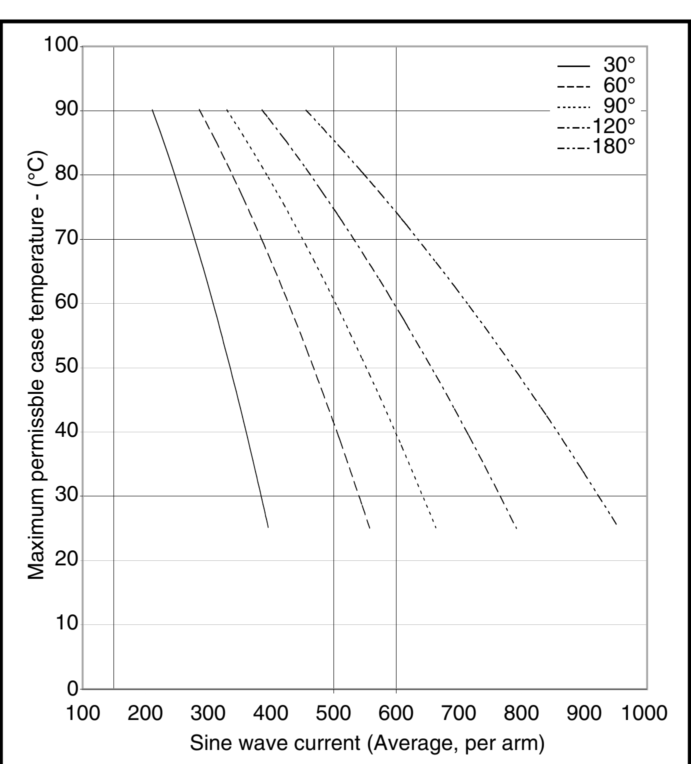

Fig. 9 Maximum permissible casetemperature vs on-state current at specified conduction angles, sine wave 50/60Hz

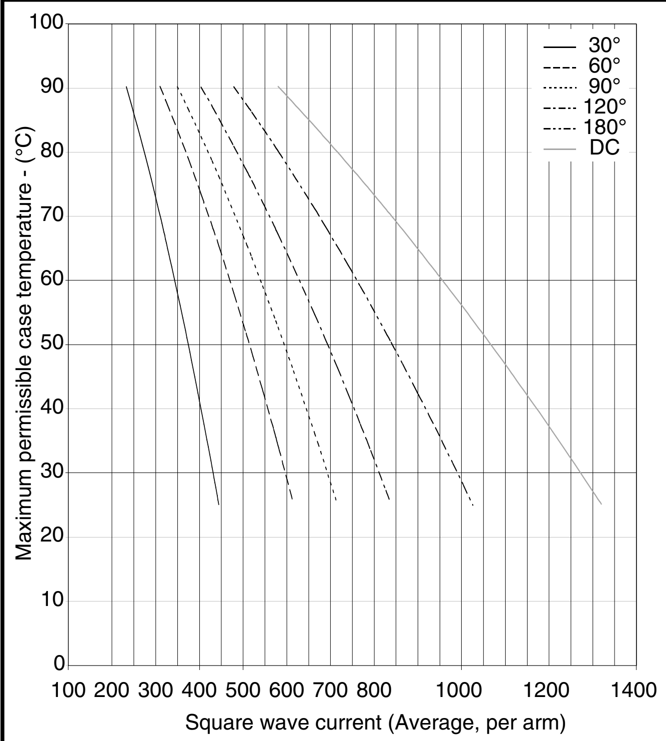

Fig. 10 Maximum permissible case temperature vs on-state current at specified conduction angles, square wave 50/60Hz

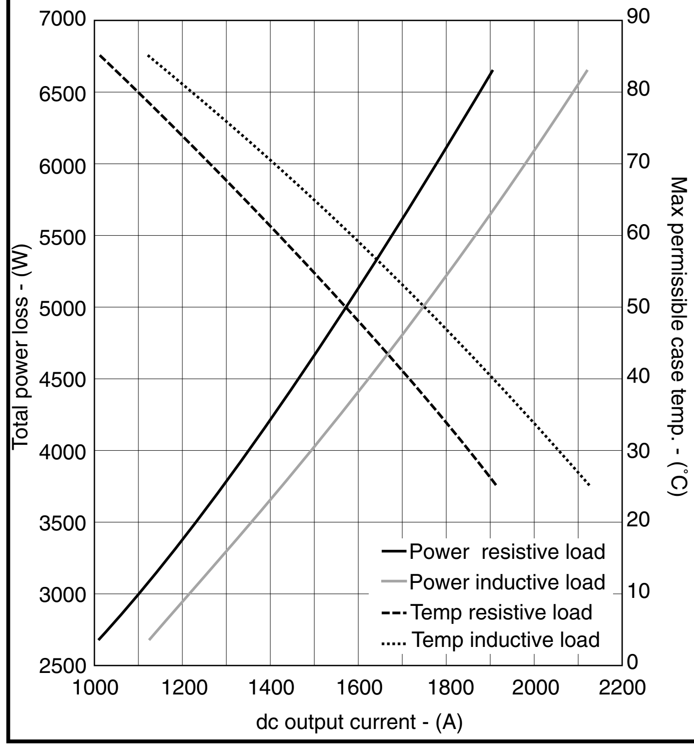

Fig. 11 50/60Hz single phase bridge DC output current vs power loss and maximum permissible case temperature

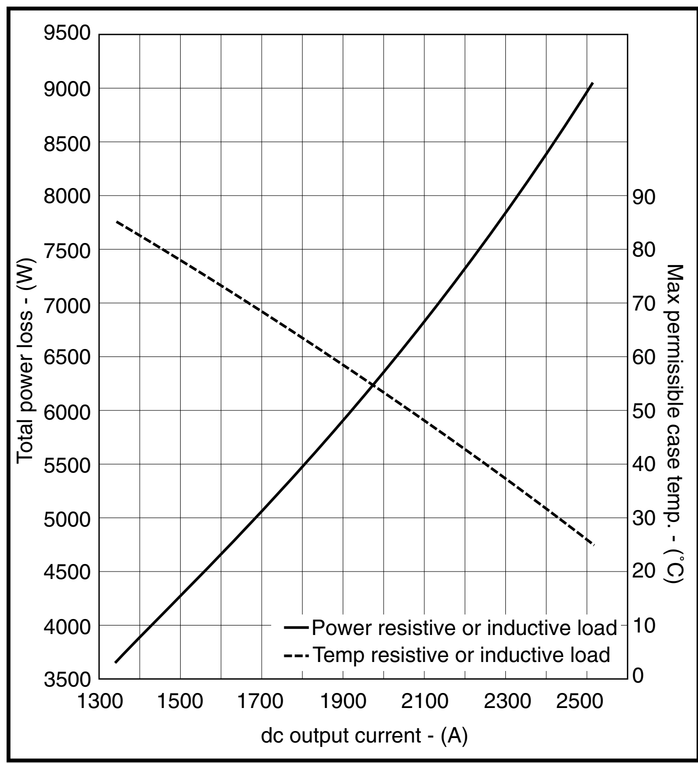

Fig. 12 50/60Hz Three phase bridge DC output current vs power loss and maximum permissible case temperature

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.

150
6
112
25.4
25.4
52
10
28
36
48
60
44
50
31
ø6.5(4PLCS)3
M10 THD
MAX 18 DP.
5(G1) 4(K1)
3(A) 2(A) 1(AK)
6(G2) 7(K2)

Nominal weight: 1580g
Auxiliary gate/cathode leads not supplied as standard, but maybe purchased separately.

Module outline type code: MP04

MOUNTING RECOMMENDATIONS

Adequate heatsinking is required to maintain the base temperature at 75°C if full rated current is to be achieved. Power dissipation may be calculated by use of $V_{T(TO)}$ and r_T information in accordance with standard formulae. We can provide assistance with calculations or choice of heatsink if required.

The heatsink surface must be smooth and flat; a surface finish of N6 (32µin) and a flatness within 0.05mm (0.002") are recommended.

Immediately prior to mounting, the heatsink surface should be lightly scrubbed with fine emery, Scotch Brite or a mild chemical etchant and then cleaned with a solvent to remove oxide build up and foreign material. Care should be taken to ensure no foreign particles remain.

An even coating of thermal compound (eg. Unial) should be applied to both the heatsink and module mounting surfaces. This should ideally be 0.05mm (0.002") per surface to ensure optimum thermal performance.

After application of thermal compound, place the module squarely over the mounting holes, (or 'T' slots) in the heatsink. Fit and finger tighten the recommended fixing bolts at each end. Using a torque wrench, continue to tighten the fixing bolts by rotating each bolt in turn no more than 1/4 of a revolution at a time, until the required torque of 6Nm (55lbs.ins) is reached on all bolts at both ends.

It is not acceptable to fully tighten one fixing bolt before starting to tighten the others. Such action may DAMAGE the module.

POWER ASSEMBLY CAPABILITY

The Power Assembly group provides support for those customers requiring more than the basic semiconductor switch. Using CAD design tools the group has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of Dynex semiconductors.

An extensive range of air and liquid cooled assemblies is available covering the range of circuit designs in general use today.

HEATSINKS

The Power Assembly group has a proprietary range of extruded aluminium heatsinks. These were designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or customer service office.

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We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

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