RJK1209JPE

120V - 80A - N Channel Power MOS FET
High Speed Power Switching

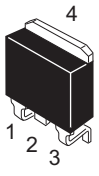
R07DS0691EJ0100
Rev.1.00
Mar 08, 2012

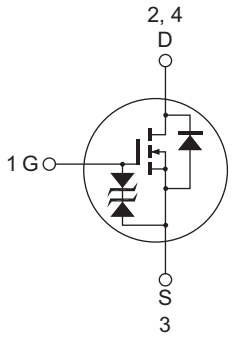
Features

- For Automotive application
- AEC-Q101 compliant
- Low on-resistance : $R_{DS(on)}$ = 14 mΩ typ.
- Low input capacitance: Ciss = 4600 pF typ

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK(S)-(1))





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	120	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	80	A
Drain peak current	I_D (pulse) Note1	320	A
Body-drain diode reverse drain current	I_{DR}	80	A
Avalanche current	I_{AP} Note2	45	A
Avalanche energy	E_{AR} Note2	173	mJ
Channel dissipation	Pch Note3	150	W
Channel temperature	Tch Note4	175	°C
Strage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10µs duty cycle ≤ 1%
2. Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C
4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θch-c: 1.0°C/W

Electrical Characteristics

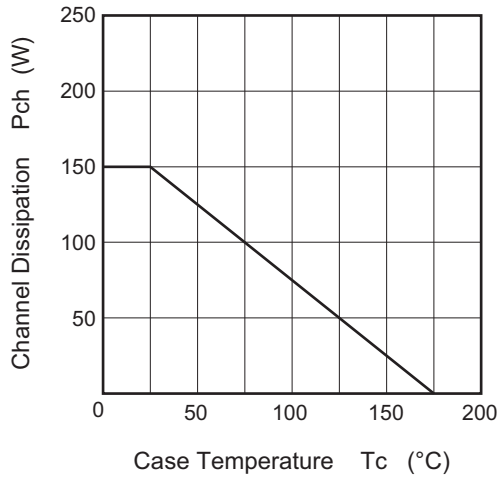
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 120 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.4	—	3.6	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	14	19	mΩ	I_D = 40 A, V_{GS} = 10 V Note5
Input capacitance	Ciss	—	4600	—	pF	V_{DS} = 10V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	570	—	pF	
Reverse transfer capacitance	Crss	—	190	—	pF	
Total gate charge	Qg	—	65	—	nC	V_{DD} = 50 V, V_{GS} = 10 V, I_D = 80 A
Gate to source charge	Qgs	—	18	—	nC	
Gate to drain charge	Qgd	—	12	—	nC	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 40 A, R_L = 0.75 Ω, V_{GS} = 10 V, R_G = 4.7 Ω
Rise time	t_r	—	13	—	ns	
Turn-off delay time	$t_{d(off)}$	—	75	—	ns	
Fall time	t_f	—	8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.96	1.25	V	I_F = 80 A, V_{GS} = 0 Note5
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 80 A, V_{GS} = 0 di_F/dt = 100 A/μs

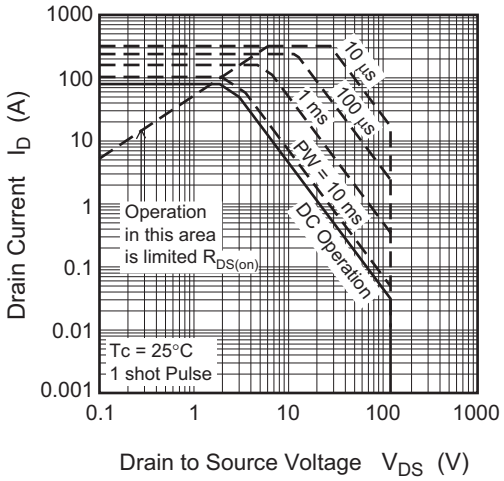
Note: 5. Pulse test

Main Characteristics

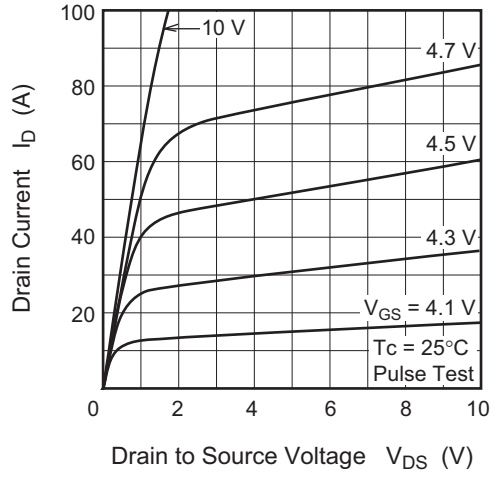
Power vs. Temperature Derating



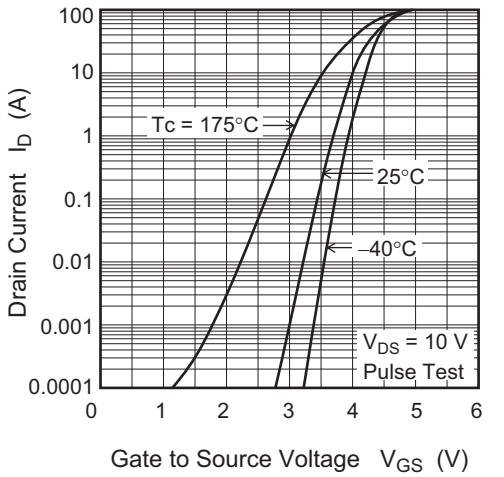
Maximum Safe Operation Area



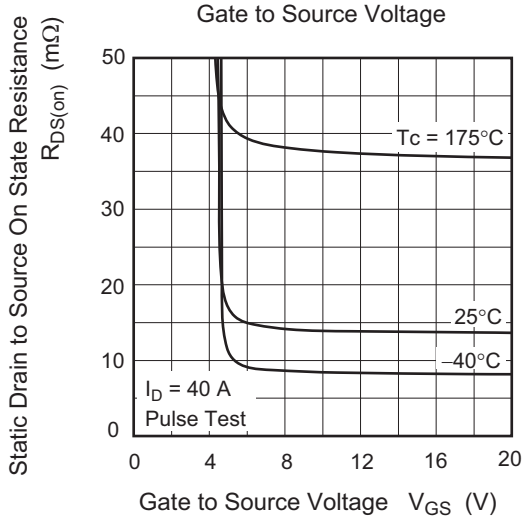
Typical Output Characteristics



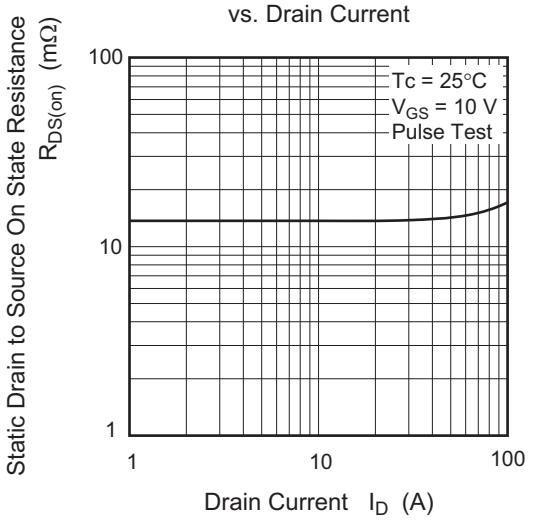
Typical Transfer Characteristics



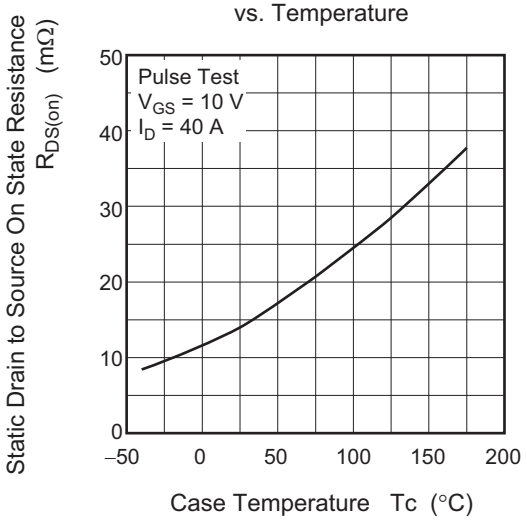
Static Drain to Source On State Resistance vs. Gate to Source Voltage



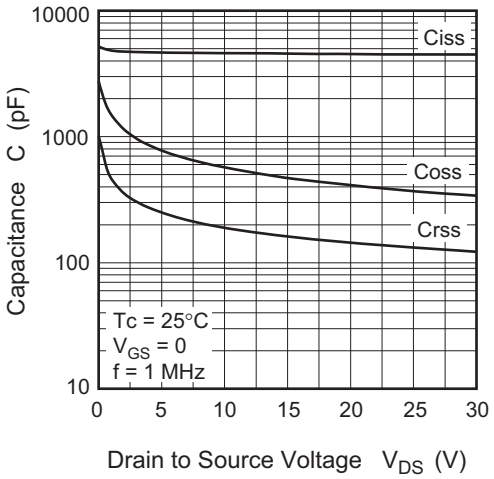
Static Drain to Source On State Resistance vs. Drain Current



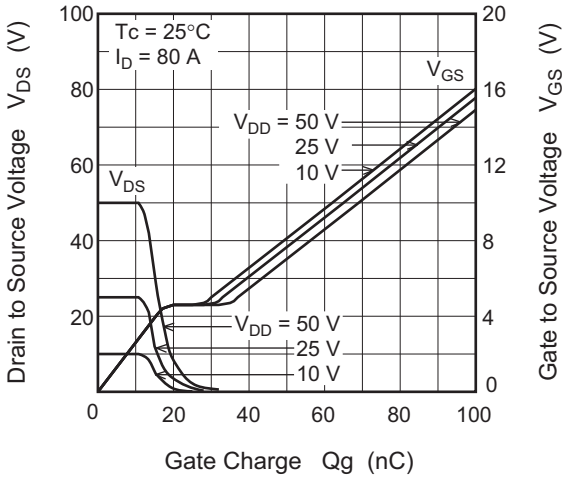
Static Drain to Source On State Resistance vs. Temperature



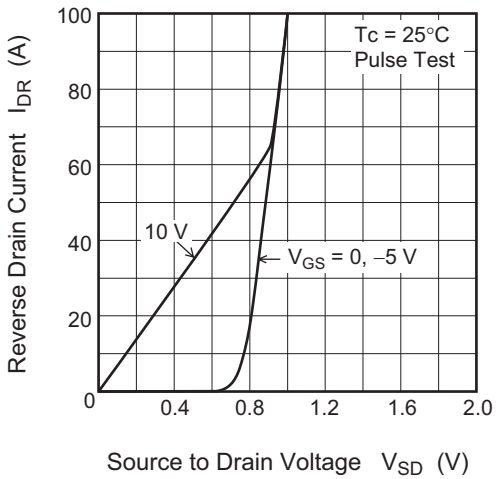
Typical Capacitance vs. Drain to Source Voltage



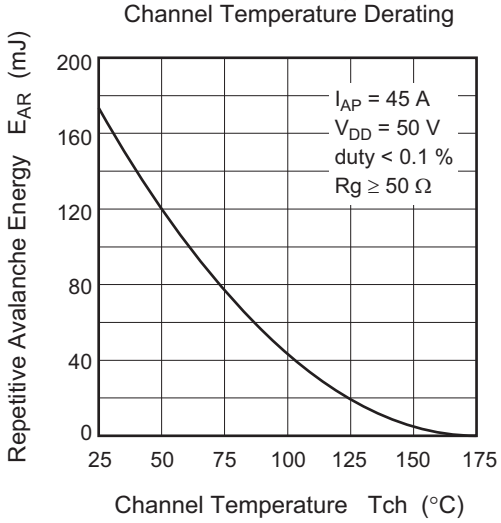
Dynamic Input Characteristics



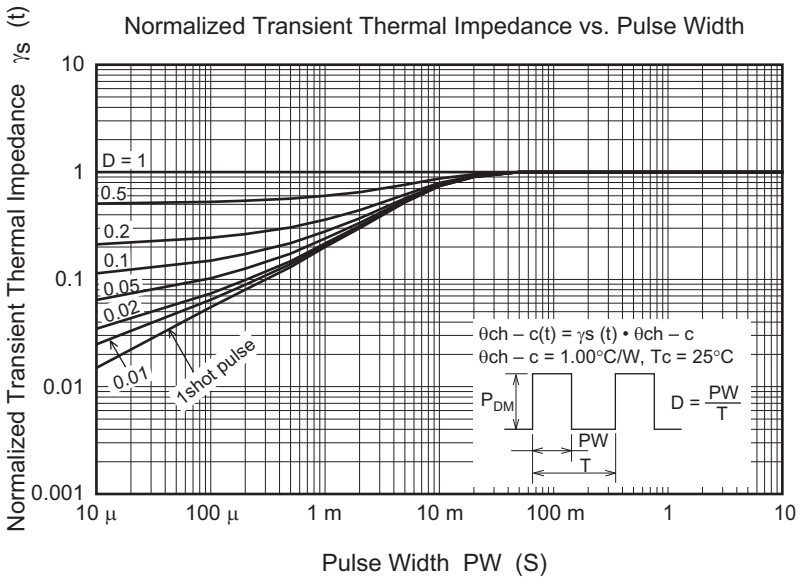
Reverse Drain Current vs. Source to Drain Voltage



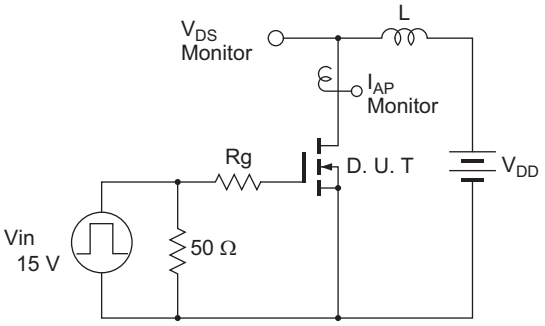
Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

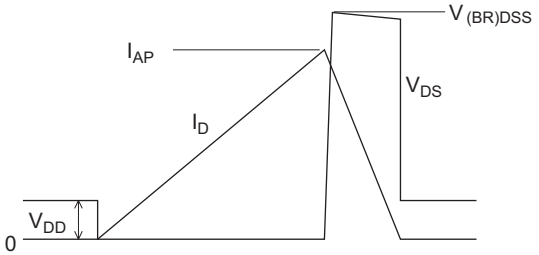


Avalanche Test Circuit

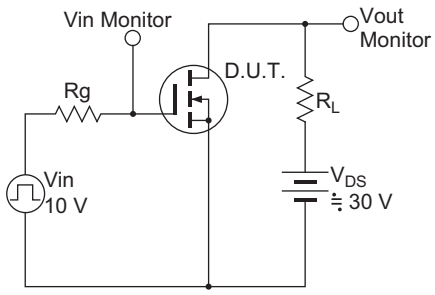


Avalanche Waveform

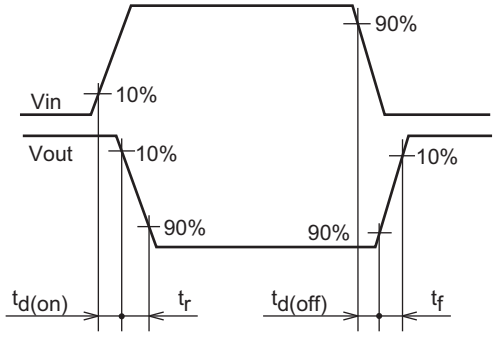
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



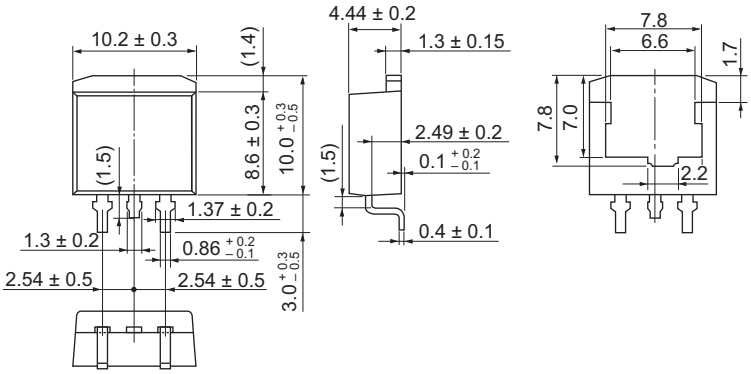
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(1)	SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK1209JPE-00-J3	1000 pcs	Taping (Sinistrorse)

Note: The symbol of 2nd "-" is occasionally presented as "#".

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