μPB100422
256 x 4-Bit
100K ECL RAM

Description

The μPB100422 is a very high-speed 100K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 or 10 ns maximum are available in 24-pin ceramic DIP or ceramic flatpack packaging.

Features

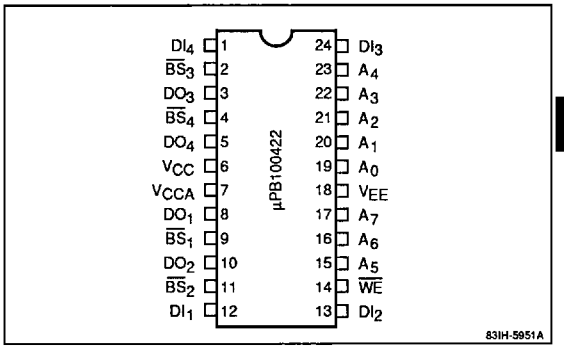
- 256-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin ceramic DIP or 24-pin ceramic flatpack packaging

Ordering Information

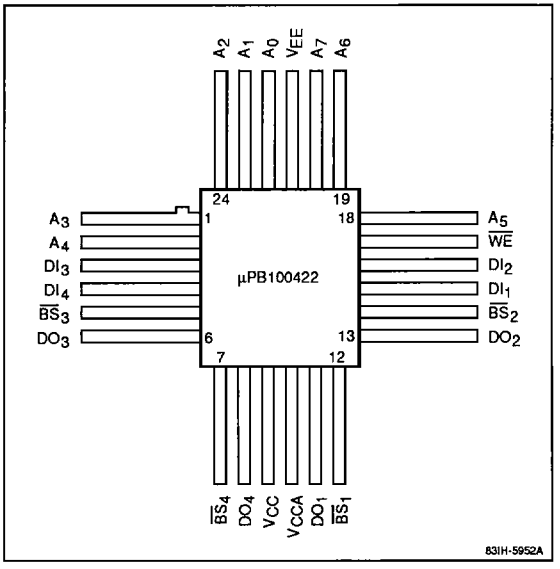
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100422D-7	7 ns	−220 mA	24-pin ceramic DIP
D-10	10 ns		
μPB100422B-7	7 ns	−220 mA	24-pin ceramic flatpack
B-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



24-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_7	Addresses
$\overline{BS}_1$ - $\overline{BS}_4$	Block select inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature, under bias, $T_{STG\ (bias)}$	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

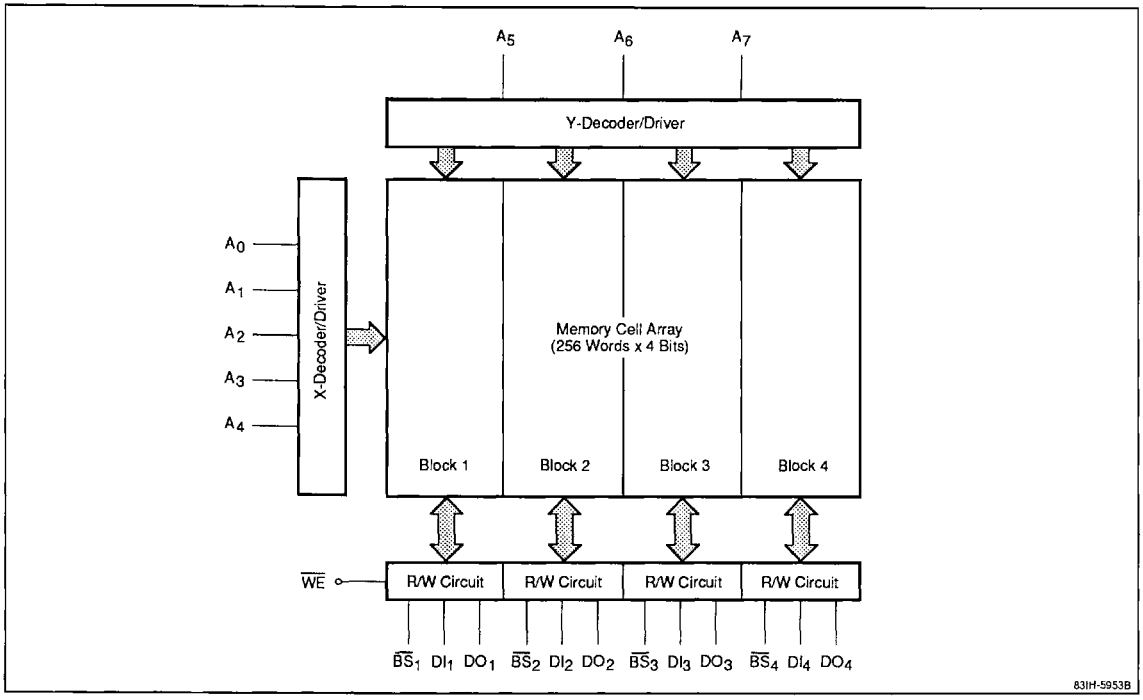
Truth Table

$\overline{BS}$	$\overline{WE}$	DI	DO	Function
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data Valid	Read

Notes:

(1) The Block Select input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



DC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{BS_1}$-$\overline{BS_4}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ± 5%

		μPB100422-7			μPB100422-10				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Block select access time	t_{ABS}			5			5	ns	
Block select recovery time	t_{RBS}			5			5	ns	
Address access time	t_{AA}			7			10	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	1			2			ns	
Address hold time	t_{WHA}	1			2			ns	
Block select setup time	t_{WSBS}	1			2			ns	
Block select hold time	t_{WHBS}	1			2			ns	
Write disable time	t_{WS}			5			5	ns	
Write recovery time	t_{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) The output load is shown in figure 1.

(4) Input transition times are shown in figure 2.

Figure 1. Loading Conditions Test Circuit

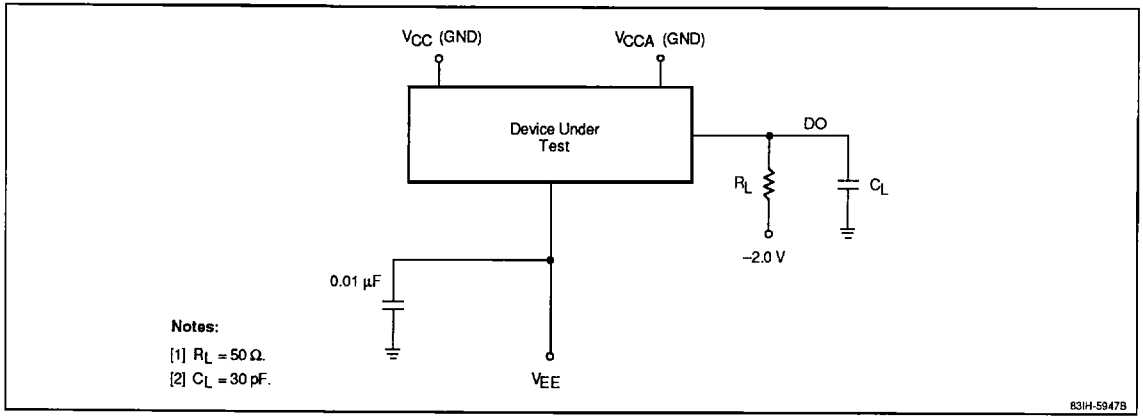
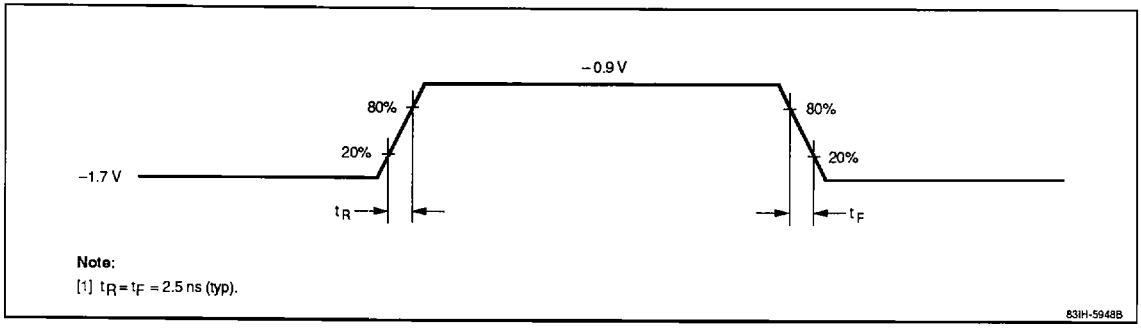
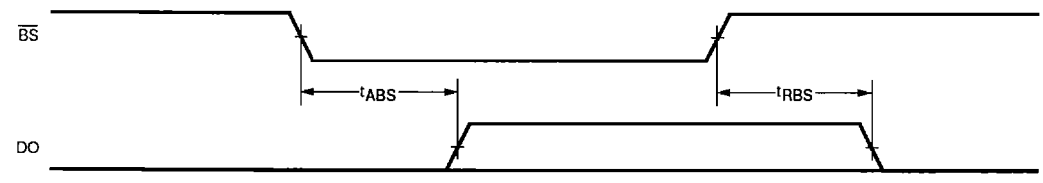


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access



Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{BS}$.

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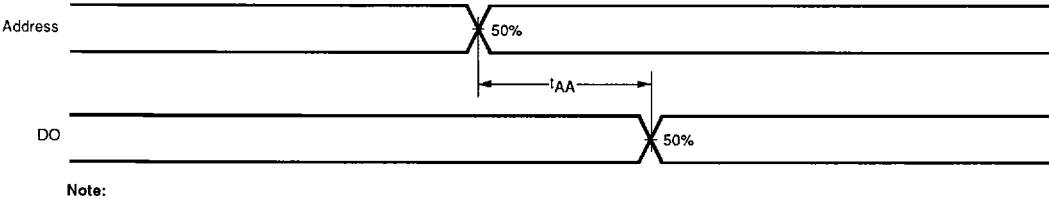
Address Access Cycle



Note:

[1] $\overline{BS} = V_{IL}$

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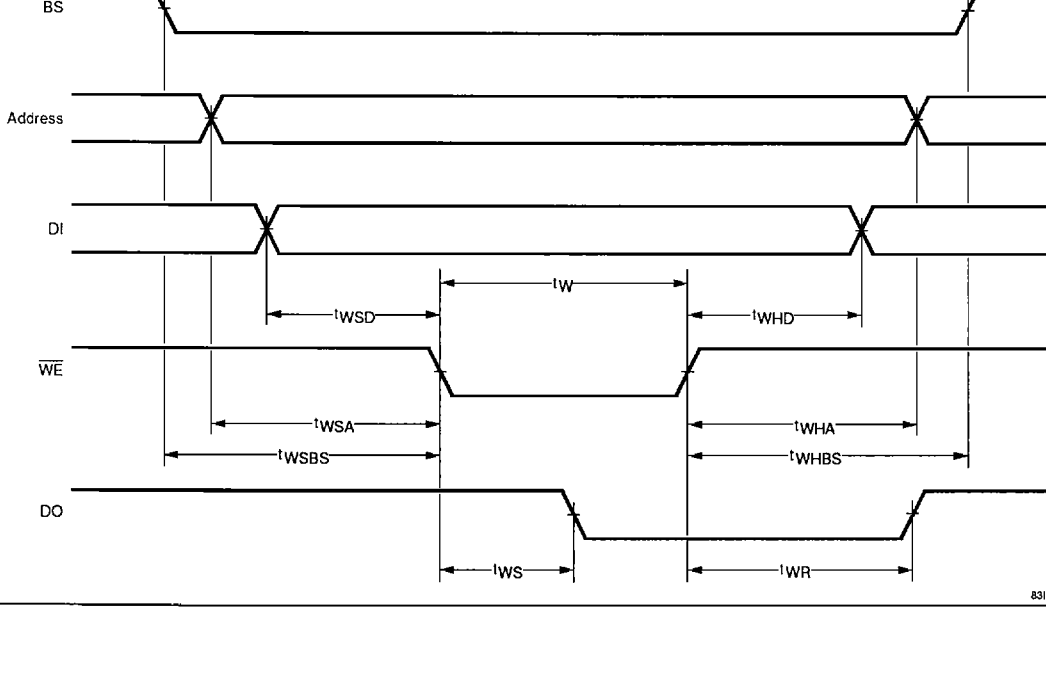
Write Cycle



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