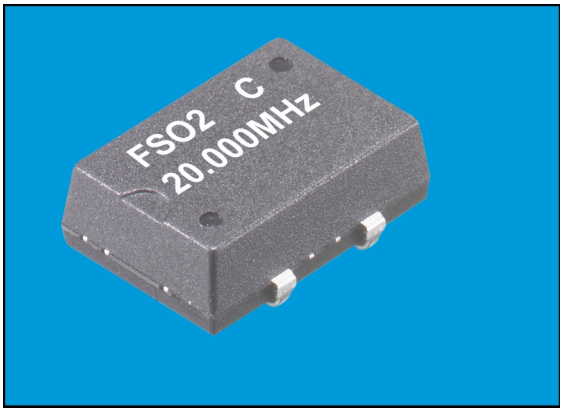
SURFACE MOUNT HCMOS CLOCK OSCILLATORS

FSO SERIES

The FSO series is compatible with both TTL and HCMOS technologies. The J-leaded configuration and high resistance to soldering temperature make it ideal for surface mount production processes. The FSO offers the low power consumption of HCMOS, but will drive a full 10 TTL Gates when used in a TTL application. This part is built to withstand vapor phase and other high temperature soldering operations and to give long term outstanding performance and reliability.



FEATURES

- Extended Temperature Range
- Solderable @ 260° for 10 sec.
- Tape and Reel (1,000 pcs. STD)

• MODEL NUMBER SELECTION (Stabilities & Temperature Ranges)

VDD (V)	Frequency Stability* (PPM)	Operating Temperature (°C)	Storage Temperature (°C)	Model Number
5.0 ± 0.5	±100	-20 ~ +70	-55 ~ +125	FSO-2
	±200	-40 ~ +85		
	±50	-20 ~ +70		FSO-25
3.3 ± 0.3	±100	-20 ~ +70		FSO-3
	±200	-40 ~ +85		
	±50	-20 ~ +70		FSO-35

*** Inclusive of 25°C tolerance, operating temperature range, input voltage change, and load change.**

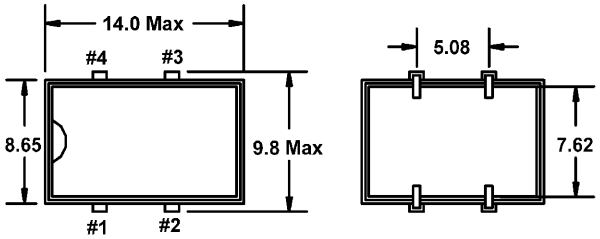
• ELECTRICAL CHARACTERISTICS (VDD = 5.0V (FSO-2/25), VDD = 3.3V (FSO-3/35)

PARAMETERS	FREQUENCY RANGE	CONDITIONS	FSO-2, FSO-25		FSO-3, FSO-35		UNITS
			MIN	MAX	MIN	MAX	
Frequency Range (FO)			1.000	66.6667	1.000	66.6667	MHz
Input Current	1.000 ~ 30.000	No Load		23		9	mA
	30.000+ ~ 66.6667			35		20	
Output Symmetry	1.000 ~ 66.6667	50% VDD	40	+60	40	60	%
		1.4V	45	+55			
Rise Time (TR)	1.000 ~ 30.000	20%VDD ~ 80%VDD		8		6	nS
		0.4V ~ 2.4V		8		---	
	30.000+ ~66.6667	20%VDD ~ 80%VDD		7		6	
		0.4V ~ 2.4V		5		---	
Fall Time (TF)	1.000 ~ 30.000	80%VDD ~ 20%VDD		8		6	nS
		0.4V ~ 2.4V		8		---	
	30.000+ ~66.6667	80%VDD ~ 20%VDD		7		6	
		0.4V ~ 2.4V		5		---	
Output Voltage (VOL)	1.000 ~ 66.6667	IOL = MAX		0.4		0.4	V
(VOH)		IOH = MAX	4.6		2.9		
Output Current (IOL)		VOL = MAX		16		4	mA
(IOH)		VOH = MIN		-16		-4	
Output Load		TTL		10		---	TTL
		HCMOS		50		30	pF
Start-up Time (TS)	1.000 ~ 30.000			4		4	mS
	30.000+ ~ 66.6667			10		10	
Enable/Disable Time		See Table**				100	nS

****ENABLE / DISABLE FUNCTION ****

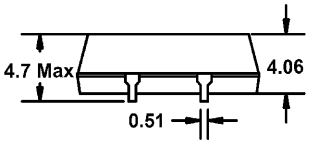
$\overline{INH}$ (Pin 1)	OUTPUT (Pin 3)
OPEN***	ACTIVE
'1' Level VIH ≥ 2.4 V	ACTIVE
'0' Level VIL ≤ 0.6 V	High Z

*** An internal pullup resistor from pin 1 to pin 4 allows active output if pin 1 is left open.
See page 44 for mechanical specifications, test circuits, and output waveform.
Note: A 0.01µF bypass capacitor should be placed between VDD (Pin 4) and GND (Pin 2) to minimize power supply line noise.
All specifications subject to change without notice. Rev. 03/02/00

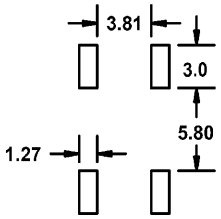


Pin Connections

#1 E/D** #3 Output
#2 GND #4 V DD



Recommended Solder Pad Layout



All dimensions are in millimeters.

See page 74 for tape and reel specifications.