REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add appendix A for device type 02 only. Make editorial changes throughout.	97-04-09	R. MONNIN
B	Make change to 1.4, 30.2.1, $I_{S(OFF)}$ overvoltage and $I_{D(OFF)}$ overvoltage tests. - ro	97-09-12	R. MONNIN
C	Make change to boilerplate and add device class T for device type 02. - ro	98-12-02	R. MONNIN
D	Add level P to table I. Make change to 1.5 and glassivation as specified under APPENDIX A. - ro	99-04-22	R. MONNIN
E	Make change to enable delay waveform as specified on figure 6. - ro	00-04-14	R. MONNIN
F	Make changes to supply voltage and V_{REF} to GND limits as specified under 1.3. Make clarification to paragraphs 4.4.4.2 and 4.4.4.3. - ro	04-06-25	R. MONNIN
G	Under 1.5, move footnote 3/ to the latch up parameter. Make correction to the R_L value under the $t_{ON(A)}$, $t_{OFF(A)}$ test as specified in table I. - ro	06-02-24	R. MONNIN
H	Add a junction temperature limit to paragraph 1.3 and make clarifications to the figure 3 logic diagram. - ro	09-06-17	J. RODENBECK
J	Add device type 03. Add paragraphs 2.2, 6.7, and Table IB. Under Table IIB, delete $+I_{S(OFF)}$, $-I_{S(OFF)}$, $-I_{D(OFF)}$, $+I_{D(OFF)}$, $+I_{D(ON)}$, $-I_{D(ON)}$ parameters. Under figure A-1, backside metallization, delete the word "none" and replace with "silicon". Update boilerplate paragraph to current MIL-PRF-38535 requirements. - ro	11-01-26	C. SAFFLE
K	Add device types 04 and 05. Make changes to paragraphs 1.2.2, 1.3, 1.4, 1.5, 4.4.4.2, A.1.2.2, A.1.2.4, Table IA, Table IB, Table IIA, Table IIB, and figure 1. Delete paragraph 4.4.4.2.1. - ro	11-06-28	C. SAFFLE
L	Add case outline Z. Make change to paragraph 3.2.5. Delete figure 4 radiation exposure circuit. Delete device class M requirements. - ro	13-05-02	C. SAFFLE
M	Add device types 04 and 05 to Table IIB. Delete LDR, HDR, and EDLRS references from paragraphs 1.2.2 and A.1.2.2. - ro	13-07-03	C. SAFFLE
N	Add device type 05 to the Analog input overvoltage range (power on/off) parameter as specified under paragraph 1.3. - ro	13-08-20	C. SAFFLE

REV																				
SHEET																				
REV	N	N	N	N	N	N	N	N	N	N	N									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	N	N	N	N	N	N	N	N	N	N	N	N	N
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
95-08-23

MICROCIRCUIT, DIGITAL-LINEAR, RADIATION HARDENED, SINGLE 16-CHANNEL ANALOG MUX / DEMUX WITH OVERVOLTAGE PROTECTION, MONOLITHIC SILICON

REVISION LEVEL
N

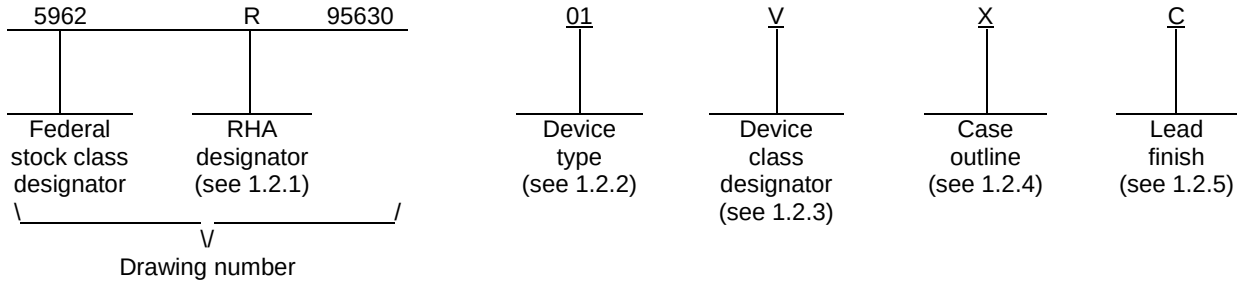
SIZE	CAGE CODE	
A	**67268**	**5962-95630**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-1840RH	Radiation hardened dielectrically isolated (DI) CMOS single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
02	HS-1840ARH	Radiation hardened DI BiCMOS single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
03	HS-1840BRH	Radiation hardened DI BiCMOS single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
04	HS-1840AEH	Radiation hardened DI BiCMOS single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection.
05	HS-1840BEH	Radiation hardened DI BiCMOS single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line
Y	CDFP3-F28	28	Flat pack
Z	CDFP3-F28	28	Flat pack with grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 1/

Supply voltage between V+ and V- :
- Device type 01 ..... +40 V
- Device types 02, 03, 04, and 05 ..... +33 V

Supply voltage between V+ and GND :
- Device type 01 ..... +20 V
- Device types 02, 03, 04, and 05 ..... +16.5 V

Supply voltage between V- and GND :
- Device type 01 ..... -20 V
- Device types 02, 03, 04, and 05 ..... -16.5 V

V_{REF} to GND :
- Device type 01 ..... +20 V
- Device types 02, 03, 04, and 05 ..... +16.5 V

Digital input overvoltage range ..... $((GND) - 4\ V) \leq V_A \leq ((V_{REF}) + 4\ V)$

Analog input overvoltage range (power on/off):
- Device type 01 ..... $-25\ V \leq V_S \leq +25\ V$
- Device types 02, 03, 04, and 05 ..... $-35\ V \leq V_S \leq +35\ V$

Storage temperature range ..... -65°C to +150°C

Junction temperature (T_J) ..... +175°C

Maximum package power dissipation (P_D): 2/
- Case X ..... 1600 mW
- Cases Y and Z ..... 1400 mW

Lead temperature (soldering, 10 seconds) ..... +275°C

Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

Thermal resistance, junction-to-ambient (θ_{JA}):
- Case X ..... 83.1°C/W
- Cases Y and Z ..... 49.1°C/W

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ The derating factor for case X shall be 20.4 mW/°C, above T_A = +95°C, and for cases Y and Z shall be 18.5 mW/°C above T_A = +95°C.

1.4 Recommended operating conditions.

Positive supply voltage (V+):
- Device types 01, 02, and 04 ..... +15 V
- Device types 03 and 05 ..... +12 V ±10%

Negative supply voltage (V-):
- Device types 01, 02, and 04 ..... -15 V
- Device types 03 and 05 ..... -12 V ±10%

V_{REF} ..... 5 V dc

V_{AH} ..... 4.0 V dc

V_{AL} ..... 0.8 V dc

V_{EN} ..... 0.8 V dc

Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available: high dose rate tests - dose rate = 50 – 300 rad(Si)/s
- Device classes Q and V:
  - Device type 01 ..... 200 krads(Si)
  - Device types 02, 03, 04 and 05 ..... 300 krads(Si)
- Device class T:
  - Device type 02 ..... 100 krads(Si)

ELDRS test (Low dose rate ≤ 10 mrad(Si)/s:
- Device class V:
- Device types 02 and 03 ..... Not production tested 3/
- Device types 04 and 05 ..... 50 krads(Si) 3/ 4/

Single event phenomena (SEP) :
- No SEL occurs at effective linear energy threshold (LET):
  - Device type 01 ..... ≤110 MeV/cm^2/mg 5/
  - Device types 02, 03, 04, and 05 ..... Latch up free 5/

Dose rate induced latch up:
- Device type 01 ..... None 6/
- Device types 02, 03, 04, and 05 ..... Not tested

Dose rate upset:
- Device type 01 ..... ≥1 x 10^8 rads(Si)/s
- Device types 02, 03, 04, and 05 ..... Not tested

For device types 02, 03, 04 and 05, the manufacturer supplying RHA parts on this drawing has performed characterization testing to a level of 150 krad(Si) that demonstrates the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) according to MIL-STD-883 method 1019 paragraph 3.13.1.1. Therefore, this part may be considered ELDRS free. Testing beyond 150 krads(Si) was not performed.

_____

3/ For device types 02, 03, 04 and 05, the manufacturer supplying RHA parts on this drawing has performed characterization testing to a level of 150 krad(Si) at low and high dose rate in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1. Therefore, this part may be considered ELDRS free. Testing beyond 150 krads(Si) was not performed.

4/ Devices 04 and 05 are production lot acceptance tested on a wafer by wafer basis to 50 krads(Si) at low dose rate (≤ 10 mrad(Si)/s).

5/ Device type 01 uses dielectrically isolated (DI) / CMOS technology and latch-up is physically not possible. Device types 02, 03, 04, and 05 use dielectrically isolated (DI) technology and latch-up is physically not possible.

6/ Guaranteed by process design, but not tested, unless specified in table IA herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input leakage current, 2/ address or enable pins	I_{AH}	Measure inputs sequentially, ground all used pins.		1,2,3	01,02, 03,04, 05	-1.0	1.0	µA
			M, D, P, L, R, F	1 3/		-1.0	1.0	
	I_{AL}			1,2,3		-1.0	1.0	µA
			M, D, P, L, R, F	1 3/		-1.0	1.0	
Leakage current into the source terminal of an off switch	$I_{S(OFF)}$	V_S = -10 V, all unused inputs and output		1	01,02, 03,04, 05	-10	+10	nA
		equal +10 V, see figure 4		2,3		-100	+100	
			M, D, P, L, R, F 4/	1 3/		-100	+100	
		V_S = +10 V, all unused inputs and output		1		-10	+10	nA
		equal -10 V, see figure 4		2,3		-100	+100	
			M, D, P, L, R, F 4/	1 3/		-100	+100	
Leakage current into the source terminal of an off switch with power off	$I_{S(OFF)}$ power off	V_S = +25 V, V_A = 0 V, V_{EN} = 0 V, V- = 0 V, V+ = 0 V, V_{REF} = 0 V,		1	01,02, 03,04, 05	-50	+50	nA
		all unused inputs tied to GND, see figure 4		2,3		-100	+100	
			M, D, P, L, R, F	1 3/		-100	+100	
Leakage current into the source terminal of an off switch with overvoltage applied	$I_{S(OFF)}$ over-voltage	V_D = 0 V, all unused inputs tied to GND, see figure 4		1,2,3	01,02, 03,04, 05	-1	+1	µA
		5/	M, D, P, L, R, F 4/	1 3/		-1.5	+1.5	
		V_D = 0 V, all unused inputs tied to GND, see figure 4		1,2,3		-1	+1	µA
		6/	M, D, P, L, R, F 4/	1 3/		-1.5	+1.5	
Leakage current into the drain terminal of an off switch with overvoltage applied	$I_{D(OFF)}$ over-voltage	V_D = 0 V, all unused inputs tied to GND, see figure 4		1,2,3	01,02, 03,04, 05	-1	+1	µA
		5/	M, D, P, L, R, F 4/	1 3/		-1	+1	
		V_D = 0 V, all unused inputs tied to GND, see figure 4		1,2,3		-1	+1	µA
		6/	M, D, P, L, R, F 4/	1 3/		-1	+1	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Leakage current into the drain terminal of an off switch	$I_{D(OFF)}$	V_D = -10 V, all unused inputs = +10 V, see figure 4	1	01,02, 03,04, 05	-10	+10	nA
			2,3		-100	+100	
		M, D, P, L, R, F 4/	1 3/		-100	+100	
Leakage current into the drain terminal of an off switch	$I_{D(OFF)}$	V_D = +10 V, all unused inputs = -10 V, see figure 4	1	01,02, 03,04, 05	-10	+10	nA
			2,3		-100	+100	
		M, D, P, L, R, F 4/	1 3/		-100	+100	
Leakage current from an on driver into the switch (drain and source)	$I_{D(ON)}$	V_S = +10 V, V_D = +10 V, V_{EN} = 0.8 V, all unused input = -10 V, see figure 4	1	01,02, 03,04, 05	-10	+10	nA
			2,3		-100	+100	
		M, D, P, L, R, F 7/	1 3/		-100	+100	
		V_S = -10 V, V_D = -10 V, V_{EN} = 0.8 V, all unused input = +10 V, see figure 4	1		-10	+10	nA
			2,3		-100	+100	
		M, D, P, L, R, F 7/	1 3/		-100	+100	
Positive supply current	I+	V_A = 0 V, V_{EN} = 0.8 V	1,2,3	01,02, 03,04, 05	0.05	0.5	mA
		M, D, P, L, R, F 7/	1 3/		0.05	0.5	
Negative power supply	I-	V_A = 0 V, V_{EN} = 0.8 V	1,2,3	01,02, 03,04, 05	0.05	0.5	mA
		M, D, P, L, R, F 7/	1 3/		0.05	0.5	
Positive standby supply current	$+I_{SBY}$	V_A = 0 V, V_{EN} = 4.0 V	1,2,3	01,02, 03,04, 05	0.05	0.5	mA
		M, D, P, L, R, F 4/	1 3/		0.05	0.5	
Negative standby power supply	$-I_{SBY}$	V_A = 0 V, V_{EN} = 4.0 V	1,2,3	01,02, 03,04, 05	0.05	0.5	mA
		M, D, P, L, R, F 4/	1 3/		0.05	0.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switch on resistance 8/	$R_{DS(ON)}$	V_S = V+, I_D = -1 mA, V_{EN} = 0.8 V, see figure 4	1,2,3	01	---	1.0	kΩ
				02,03, 04,05	0.5	3.0	
		M, D, P, L, R, F 7/	1 3/	01	---	1.0	
				02,03, 04,05	0.5	3.0	
		V_S = -5 V, I_D = +1 mA, V_{EN} = 0.8 V, see figure 4	1,2,3	01	---	4.0	
				02,03, 04,05	0.5	3.0	
		M, D, P, L, R, F 7/	1 3/	01	---	4.0	
				02,03, 04,05	0.5	3.0	
		V_S = +5 V, I_D = -1 mA, V_{EN} = 0.8 V, see figure 4	1,2,3	01	---	2.5	
				02,03, 04,05	0.5	3.0	
		M, D, P, L, R, F 7/	1 3/	01	---	2.5	
				02,03, 04,05	0.5	3.0	
Capacitance: digital input	C_A	V+ = V- = 0 V, f = 1 MHz, T_A = +25°C, see 4.4.1c	4	01,02, 03,04, 05		7	pF
Capacitance: channel input	$C_{S(OFF)}$	V+ = V- = 0 V, f = 1 MHz, T_A = +25°C, see 4.4.1c	4	01,02, 03,04, 05		5	pF
Capacitance: channel output	$C_{D(OFF)}$	V+ = V- = 0 V, f = 1 MHz, T_A = +25°C, see 4.4.1c	4	01,02, 03,04, 05		50	pF
Off isolation input or output	V_{ISO}	V_{EN} = 4.0 V, f = 200 kHz, C_L = 7 pF, R_L = 1 kΩ, V_S = 3 V_{RMS}, T_A = +25°C, see 4.4.1c	4	01,02, 03,04, 05	-45		dB
Functional test		See 4.4.1d	7,8A,8B	01,02, 03,04, 05			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Break-before-make 8/ time delay	t_D	C_L = 50 pF, R_L = 1 kΩ, see figure 5	9	01,02, 03,04, 05	25		ns
			10,11		5		
		M, D, P, L, R, F 4/ 7/ 9/	9 3/		5		
Propagation delay 8/ time address inputs to I/O channels	$t_{ON(A)}$, $t_{OFF(A)}$	C_L = 50 pF, R_L = 10 kΩ, see figure 5	9	01		0.6	µs
				02,03, 04,05		1.25	
			10,11	01		1.0	
				02,03, 04,05		1.5	
		M, D, P, L, R, F 4/ 7/ 9/	9 3/	01		3.0	
				02,03, 04,05		1.5	
Propagation delay 8/ time enable to I/O channels	$t_{ON(EN)}$, $t_{OFF(EN)}$	C_L = 50 pF, R_L = 1 kΩ, see figure 5	9	01		0.6	µs
				02,03, 04,05		1.25	
			10,11	01		1.0	
				02,03, 04,05		1.5	
		M, D, P, L, R, F 4/ 7/ 9/	9 3/	01		3.0	
				02,03, 04,05		1.5	

1/ Unless otherwise specified, V_{AH} (logic level high) = 4.0 V dc, V_{AL} (logic level low) = 0.8 V dc, V_{EN} = 4.0 V, and V_{REF} = 5.0 V dc. For device types 01, 02, and 04, V+ = +15 V dc, V- = -15 V dc. For device types 03 and 05, tested over tolerance range of +10%, V+ = +13.2 V dc, V- = -13.2 V dc.

2/ Input current of one node.

3/ RHA device type 01 (device classes Q and V) supplied to this drawing will meet all RHA levels M, D, P, L, R. However, device type 01 is irradiated and tested only "R" level in accordance with MIL-STD-883 method 1019 condition A.

RHA device types 02, 03, 04, and 05 (device classes Q or V) supplied to this drawing will meet all RHA levels M, D, P, L, R and F. However, device types 02, 03, 04 and 05 are irradiated and tested only at the "F" level in accordance with MIL-STD-883 method 1019 condition A (high dose rate).

RHA device types 02, 03, 04 and 05 supplied on this drawing have had characterization testing performed to a level of 150 krads(Si) that demonstrates the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) according to MIL-STD-883 method 1019 paragraph 3.13.1.1. (see paragraph 1.5 herein). In addition, device types 04 and 05 (device class V) supplied to this drawing are production lot acceptance tested on a wafer by wafer basis to the "L" level (50 krads(Si)) in accordance with MIL-STD-883 method 1019 condition D (low dose rate).

RHA device type 02 (device class T) supplied to this drawing will meet all RHA levels M, D, P, L, R. However device type 02 is irradiated and tested only "R" level in accordance with MIL-STD-883 method 1019 condition A.

Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

TABLE IA. Electrical performance characteristics - Continued.

4/ V_{EN} = 4.5 V.

5/ For device type 01, V_S = +25 V. For device types 02, 03, 04, and 05, V_S = +35 V.

6/ For device type 01, V_S = -25 V. For device types 02, 03, 04, and 05, V_S = -35 V.

7/ V_{EN} = 0.5 V.

8/ For device types 03 and 05, tested over tolerance range of ±10%, V+ = +10.8 V dc, V- = -10.8 V dc and V+ = +13.2 V dc, V- = -13.2 V dc.

9/ V_{AH} = 4.5 V and V_{AL} = 0.5 V.

TABLE IB. SEP test limits. 1/ 2/

Device types	SEP	Temperature (T_C)	Effective linear energy transfer (LET) for no SEL, bias for SEL, V_S = 15 V
01	SEL	+125°C	≤ 110 MeV-cm^2/mg
02, 03, 04, 05	SEL	+125°C	Latch up free 3/

1/ For SEP test conditions, see 4.4.4.5 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ Device types 02, 03, 04, and 05 use dielectrically isolated (DI) technology and latch up is physically not possible.

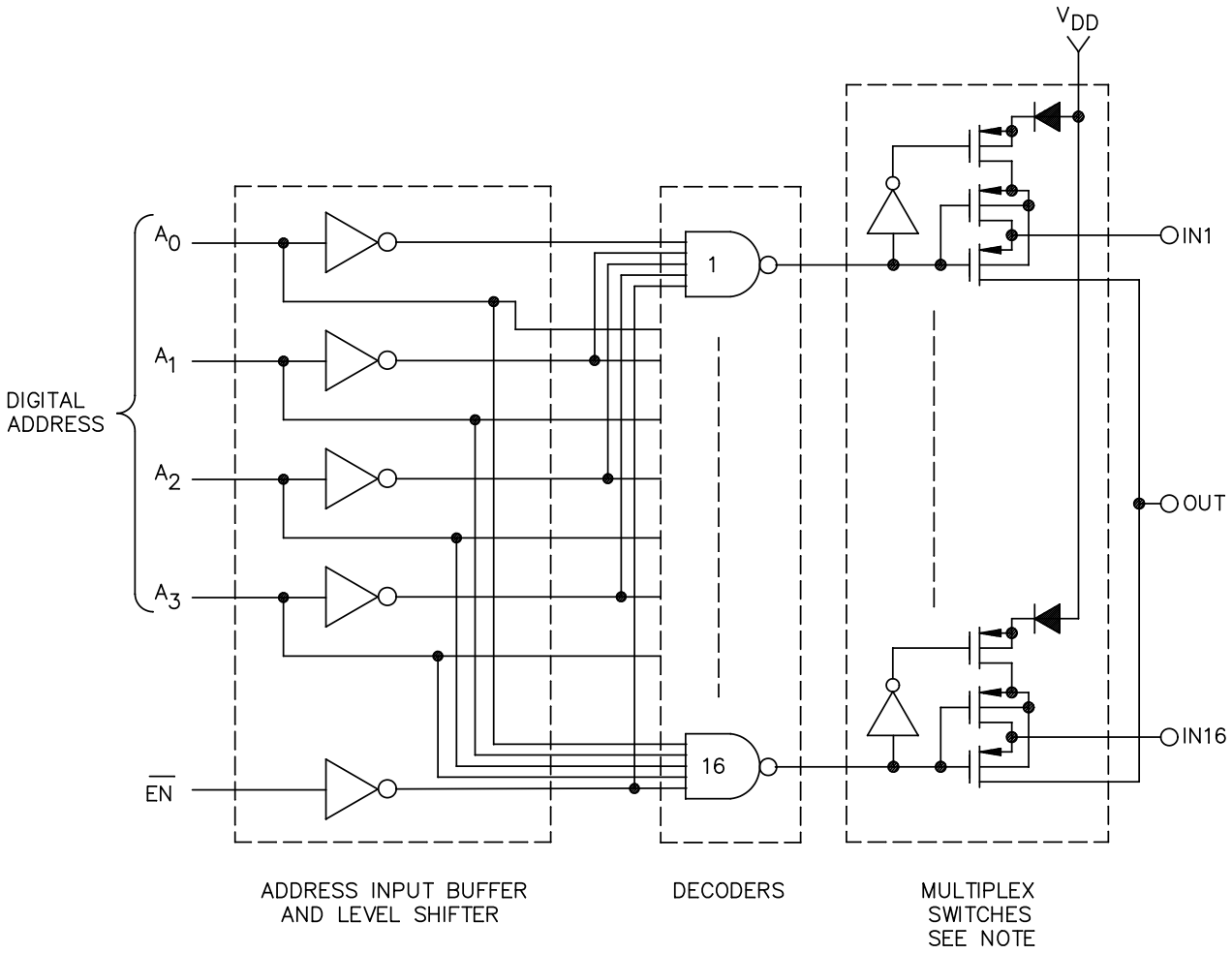
Device types	01, 02, 03, 04 and 05
Case outlines	X, Y and Z
Terminal number	Terminal symbol
1	V+
2	NC
3	NC
4	IN 16
5	IN 15
6	IN 14
7	IN 13
8	IN 12
9	IN 11
10	IN 10
11	IN 9
12	GND
13	V_{REF}
14	A3
15	A2
16	A1
17	A0
18	$\overline{EN}$
19	IN 1
20	IN 2
21	IN 3
22	IN 4
23	IN 5
24	IN 6
25	IN 7
26	IN 8
27	V-
28	OUT

NC = No connection

FIGURE 1. Terminal connections.

Truth table					
A_3	A_2	A_1	A_0	$\overline{EN}$	On channel
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

FIGURE 2. Truth table.



NOTE: Main switch INXX: Switch on, body tied to source.
Switch off, body tied to V_{CC} – 0.7 V.

FIGURE 3. Logic diagram.

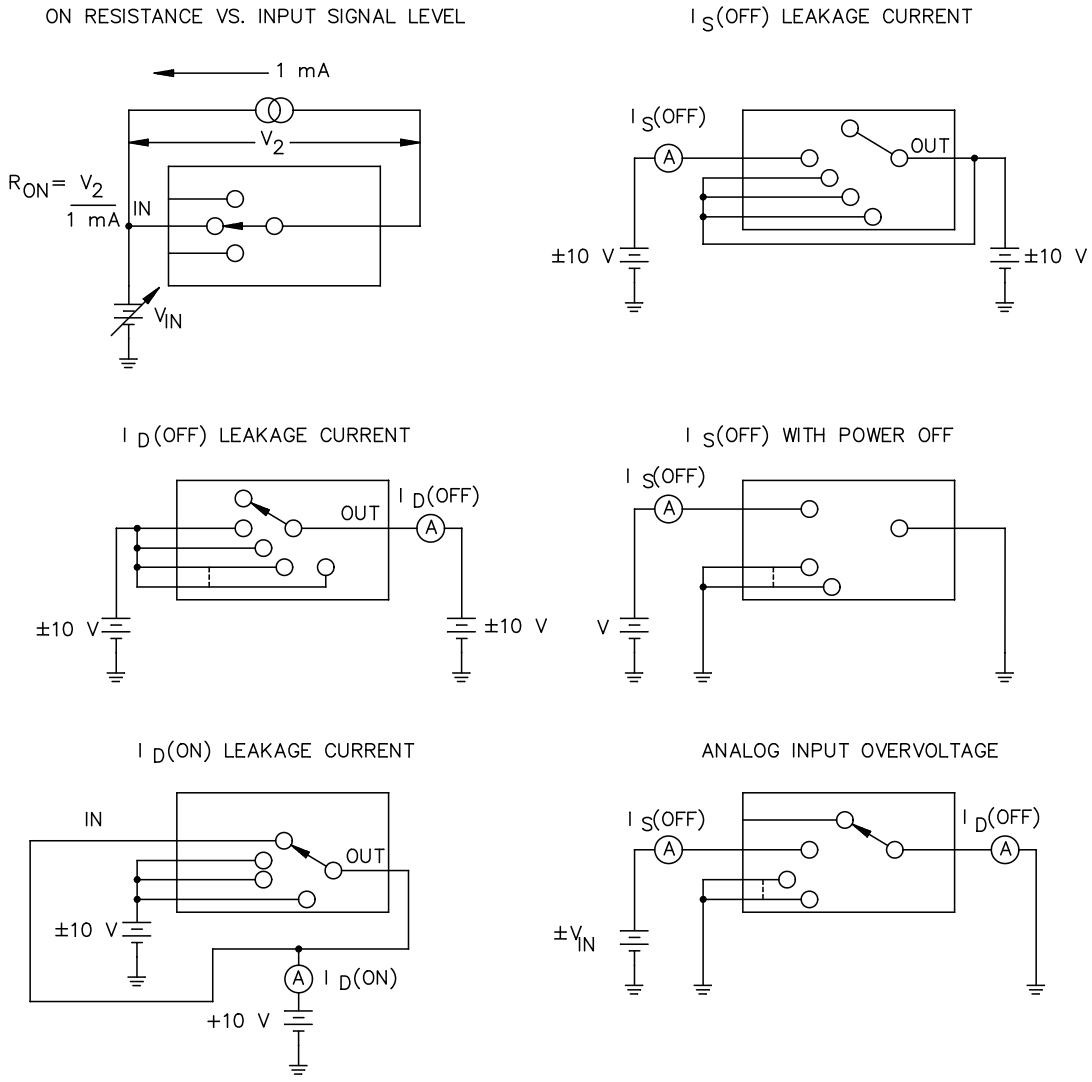
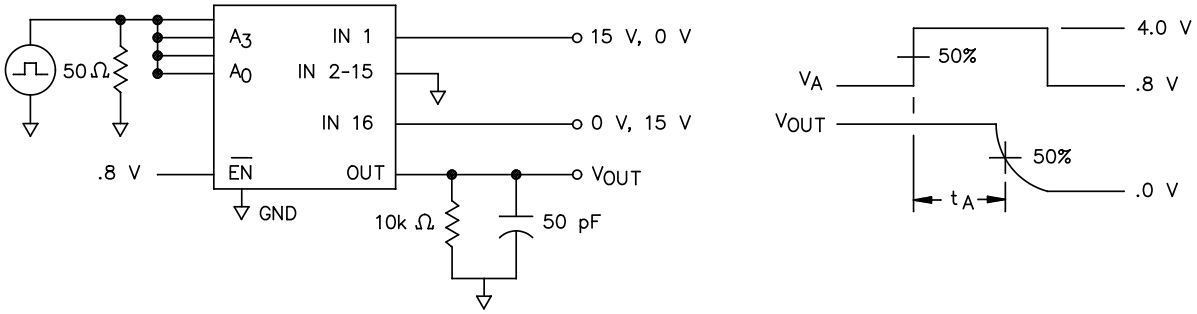
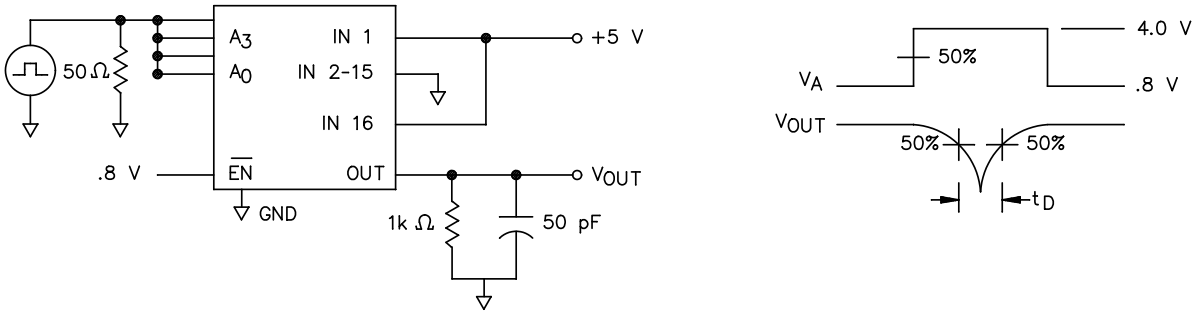


FIGURE 4. Test circuits for dc levels.

ADDRESS TIME, LOGIC LEVEL HIGH



BREAK BEFORE MAKE DELAY



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

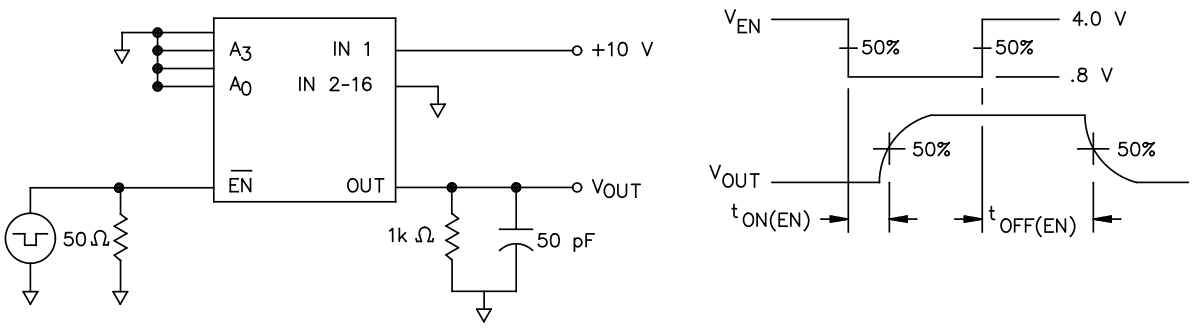


FIGURE 5. Test circuits and waveforms for ac levels.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_A, C_S, C_D, and V_{ISO} measurements) should be measured for initial qualification and after any process or design changes which may affect input or output capacitance.

d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,7,8A, 1/ 8B,9,10,11	1,2,3, 1/ 2/ 7,8A,8B,9, 10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,4,7,8A, 8B,9,10,11	1,2,3,4,7, 8A,8B,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8A,8B, 9,10,11	1,2,3,7,8A, 2/ 8B,9,10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	As specified in QM plan

1/ PDA applies to subgroup 1. For device class V, 1, 7, and Δ.
2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limits
Input leakage current, address, or enable pins	I_{AH}	Measure inputs sequentially, ground all unbiased pins	±100 nA
Switch on resistance	$R_{DS(ON)}$	For devices 01, 02, and 04, V_S = +15 V, For devices 03 and 05, V_S = +13.2 V, I_D = -1 mA, V_{EN} = 0.8 V	±150 Ω
		V_S = -5 V, I_D = +1 mA, V_{EN} = 0.8 V	±250 Ω
Positive supply current	I+	V_{EN} = 0.8 V	±50 μA
Negative supply current	I-	V_{EN} = 0.8 V	±50 μA
Positive standby supply current	$+I_{SBY}$	V_{EN} = 4.0 V	±50 μA
Negative standby supply current	$-I_{SBY}$	V_{EN} = 4.0 V	±50 μA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing high dose rate (HDR) shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, 03, 04 and 05. Total dose irradiation testing (ELDRS – low dose rate) shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein for device types 04 and 05. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535.

4.4.4.3 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When specified in the purchase order or contract, dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm$10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

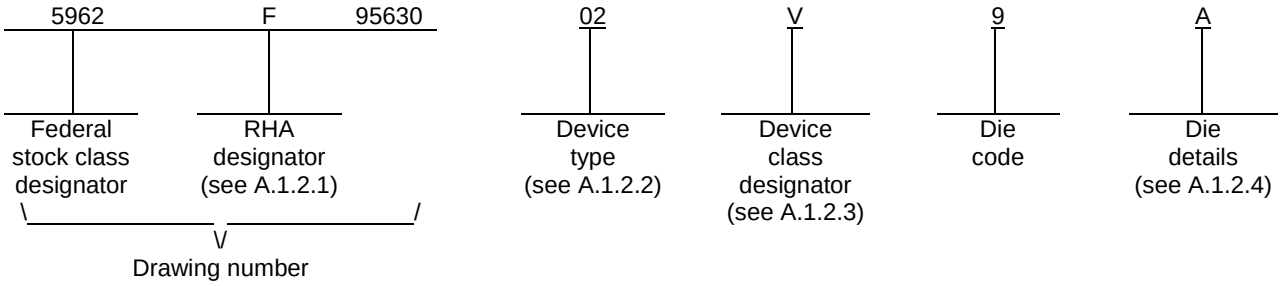
c. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-95630

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
02	HS-1840ARH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
03	HS-1840BRH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
04	HS-1840AEH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
05	HS-1840BEH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
02, 03, 04, 05	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02, 03, 04, 05	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
02, 03, 04, 05	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
02, 03, 04, 05	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.3, 4.4.4.4, and 4.4.4.5 herein..

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

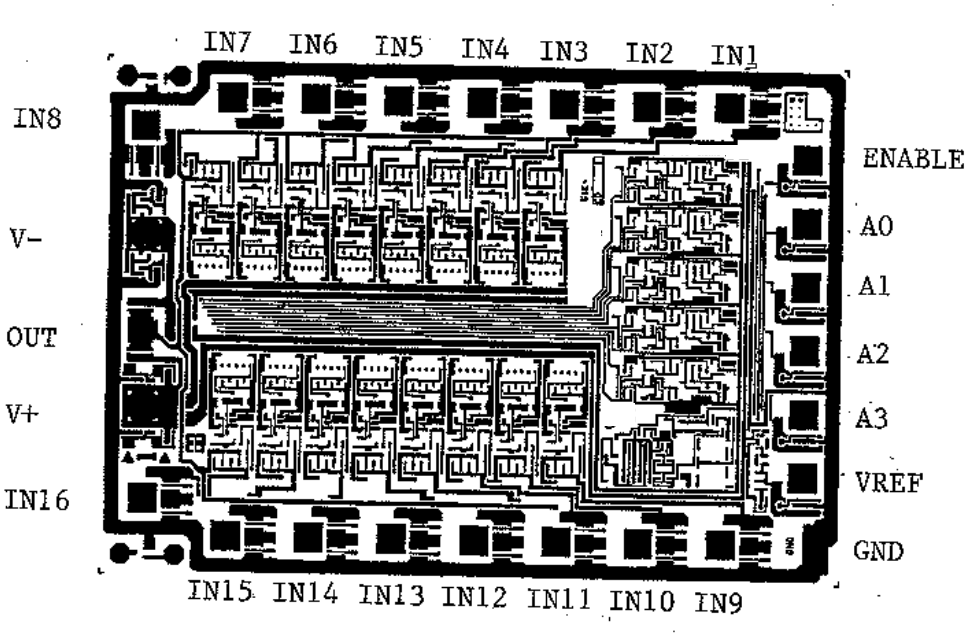
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

NOTE: Pad numbers reflect terminal numbers when placed in case outlines X, Y, and Z (see figure 1).



Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 4080 microns x 2820 microns.
Die thickness: 483 microns ± 25.4 microns.

Interface materials.
Top metallization: Al Si Cu
Thickness: 16.0 kÅ ±2 kÅ
Backside metallization: Silicon

Glassivation.
Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0 kÅ ±1.0 kÅ

Substrate: DI (dielectric isolation)

Assembly related information.
Substrate potential: Unbiased
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-08-20

Approved sources of supply for SMD 5962-95630 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9563001VXC	3/	HS1-1840RH-Q
5962R9563001VYC	3/	HS9-1840RH-Q
5962R9563001QXC	3/	HS1-1840RH-8
5962R9563001QYC	3/	HS9-1840RH-8
5962F9563002VXC	34371	HS1-1840ARH-Q
5962F9563002VYC	34371	HS9-1840ARH-Q
5962F9563002QXC	34371	HS1-1840ARH-8
5962F9563002QYC	34371	HS9-1840ARH-8
5962F9563002V9A	34371	HS0-1840ARH-Q
5962R9563002TXC	34371	HS1-1840ARH-T
5962R9563002TYC	3/	HS9-1840ARH-T
5962F9563002VZC	34371	HS9G-1840ARH-Q
5962F9563003VXC	34371	HS1-1840BRH-Q
5962F9563003VYC	34371	HS9-1840BRH-Q
5962F9563003QXC	34371	HS1-1840BRH-8
5962F9563003QYC	34371	HS9-1840BRH-8
5962F9563003V9A	34371	HS0-1840BRH-Q
5962F9563004VXC	34371	HS1-1840AEH-Q
5962F9563004VYC	34371	HS9-1840AEH-Q
5962F9563004V9A	34371	HS0-1840AEH-Q
5962F9563005VXC	34371	HS1-1840BEH-Q
5962F9563005VYC	34371	HS9-1840BEH-Q
5962F9563005V9A	34371	HS0-1840BEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803