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LB11620T

Monolithic Digital IC Brushless Motor Driver

Overview

The LB11620T is a direct PWM drive predriver IC that is optimal for three-phase power brushless motors. A motor driver circuit with the desired output capability (voltage and current) can be implemented by adding discrete transistors or other power devices to the outputs of this IC. Since the LB11620T is provided in a miniature package, it is also appropriate for use with miniature motors as well.

Features

- Three-phase bipolar drive
- Direct PWM drive (input of either a control voltage or a variable-duty PWM signal)
- Built-in forward/reverse switching circuit
- Full complement of protection circuits (current limiter, low-voltage, and automatic recovery lock (motor constraint) protection circuits)
- Selectable Hall sensor signal pulse output

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|------------------------------|-------------|------------------|
| Supply voltage 1 | V_{CC} max | V_{CC} pin | 18 | V |
| Output current | I_O max | UL, VL, WL, UH, VH, WH pins | 30 | mA |
| Allowable power dissipation | P_d max | *Mounted on a circuit board. | 0.8 | W |
| Operating temperature | T_{opr} | | -20 to +100 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

* Mounted on a circuit board : 114.3mm×76.1mm×1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LB11620T

Recommended Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------------|-------------|---|------------|------|
| Supply voltage range 1-1 | V_{CC1-1} | V_{CC} pin | 8 to 17 | V |
| Supply voltage range 1-2 | V_{CC1-2} | V_{CC} pin, with V_{CC} shorted to VREG | 4.5 to 5.5 | V |
| Output current | I_O | UL, VL, WL, UH, VH, WH pins | 25 | mA |
| 5 V constant voltage output current | IREG | | -30 | mA |
| HP pin voltage | VHP | | 0 to 17 | V |
| HP pin output current | IHP | | 0 to 15 | mA |
| RD pin voltage | VRD | | 0 to 17 | V |
| RD pin output current | IRD | | 0 to 15 | mA |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|----------------------|---|--------------|--------------|--------------|----------------------------|
| | | | min | typ | max | |
| Supply voltage 1 | I_{CC1} | | | 12 | 16 | mA |
| 5V constant voltage output (VREG pin) | | | | | | |
| Output voltage | VREG | | 4.7 | 5.0 | 5.3 | V |
| Line regulation | ΔV_{REG1} | $V_{CC} = 8$ to 17V | | 40 | 100 | mV |
| Load regulation | ΔV_{REG2} | $I_O = -5$ to -20mA | | 10 | 30 | mV |
| Temperature coefficient | ΔV_{REG3} | Design target | | 0 | | $\text{mV}/^\circ\text{C}$ |
| Low-voltage protection circuit (VREG pin) | | | | | | |
| Operating voltage | VSDL | | 3.5 | 3.7 | 3.9 | V |
| Clear voltage | VSDH | | 3.95 | 4.15 | 4.35 | V |
| Hysteresis | ΔV_{SD} | | 0.3 | 0.45 | 0.6 | V |
| Output Block | | | | | | |
| Output voltage 1-1 | V_{OUT1-1} | Low level $I_O = 400\mu\text{A}$ | | 0.2 | 0.5 | V |
| Output voltage 1-2 | V_{OUT1-2} | Low level $I_O = 10\text{mA}$ | | 0.9 | 1.2 | V |
| Output voltage 2 | V_{OUT2} | High level $I_O = -20\text{mA}$ | $V_{CC-1.1}$ | $V_{CC-0.9}$ | | V |
| Output leakage current | I_{Oleak} | | | | 10 | μA |
| Hall Amplifier Block | | | | | | |
| Input bias current | IHB (HA) | | -2 | -0.5 | | μA |
| Common-mode input voltage range 1 | VICM1 | When a Hall effect sensor is used | 0.5 | | $V_{CC-2.0}$ | V |
| Common-mode input voltage range 2 | VICM2 | For single-sided input bias (Hall IC application) | 0 | | V_{CC} | V |
| Hall input sensitivity | | | 80 | | | mVp-p |
| Hysteresis | ΔV_{IN} (HA) | | 15 | 24 | 40 | mV |
| Input voltage low \rightarrow high | VSLH (HA) | | 5 | 12 | 20 | mV |
| Input voltage high \rightarrow low | VSHL (HA) | | -20 | -12 | -5 | mV |
| PWM Oscillator (PWM pin) | | | | | | |
| High-level output voltage | V_{OH} (PWM) | | 2.75 | 3.0 | 3.25 | V |
| Low-level output voltage | V_{OL} (PWM) | | 1.2 | 1.35 | 1.5 | V |
| External capacitor charge current | ICHG | $V_{PWM} = 2.1\text{V}$ | -120 | -90 | -65 | μA |
| Oscillator frequency | f (PWM) | $C = 2000\text{pF}$ | | 22 | | kHz |
| Amplitude | V (PWM) | | 1.4 | 1.6 | 1.9 | Vp-p |

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LB11620T

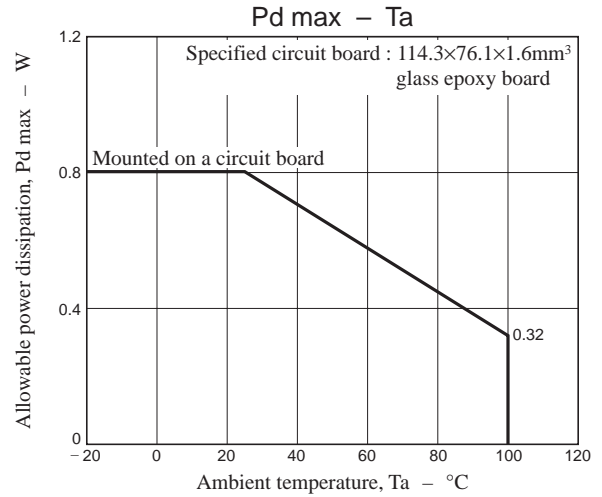
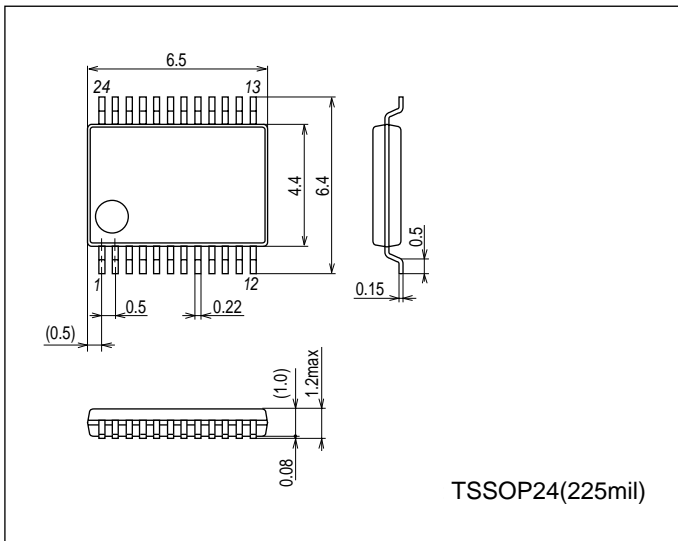
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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|-----------------------|--|----------|------|----------|-------|
| | | | min | typ | max | |
| EI+ pin | | | | | | |
| Input bias current | IB (CTL) | | -1 | | 1 | μA |
| Common-mode input voltage range | VICM | | 0 | | VREG-1.7 | V |
| Input voltage 1 | VCTL1 | Output duty 100% | | 3.0 | | V |
| Input voltage 2 | VCTL2 | Output duty 0% | | 1.35 | | V |
| Input voltage 1L | VCTL1L | Design target value. When VREG = 4.7V, 100% | | 2.82 | | V |
| Input voltage 2L | VCTL2L | Design target value. When VREG = 4.7V, 0% | | 1.29 | | V |
| Input voltage 1H | VCTL1H | Design target value. When VREG = 5.3V, 100% | | 3.18 | | V |
| Input voltage 2H | VCTL2H | Design target value. When VREG = 5.3V, 0% | | 1.44 | | V |
| HP pin | | | | | | |
| Output saturation voltage | VHPL | I _O = 10mA | | 0.2 | 0.5 | V |
| Output leakage current | IHPleak | V _O = 18V | | | 10 | μA |
| CSD oscillator (CSD pin) | | | | | | |
| High-level output voltage | V _{OH} (CSD) | | 2.7 | 3.0 | 3.3 | V |
| Low-level output voltage | V _{OL} (CSD) | | 0.7 | 1.0 | 1.3 | V |
| External capacitor charge current | ICHG1 | VCSD = 2V | -3.15 | -2.5 | -1.85 | μA |
| External capacitor discharge current | ICHG2 | VCSD = 2V | 0.1 | 0.14 | 0.18 | μA |
| Charge/discharge current ratio | RCSD | Charge current /discharge current | 15 | 18 | 21 | Times |
| RD pin | | | | | | |
| Low-level output voltage | VRDL | I _O = 10mA | | 0.2 | 0.5 | V |
| Output leakage current | IL (RD) | V _O = 18V | | | 10 | μA |
| Current limiter circuit (RF pin) | | | | | | |
| Limiter voltage | VRF | RF-GND | 0.225 | 0.25 | 0.275 | V |
| PWMIN pin | | | | | | |
| Input frequency | f (PI) | | | | 50 | kHz |
| High-level input voltage | V _{IH} (PI) | | 2.0 | | VREG | V |
| Low-level input voltage | V _{IL} (PI) | | 0 | | 1.0 | V |
| Input open voltage | V _{IO} (PI) | | VREG-0.5 | | VREG | V |
| Hysteresis | V _{IS} (PI) | | 0.2 | 0.25 | 0.4 | V |
| High-level input current | I _{IH} (PI) | VPWMIN = VREG | -10 | 0 | 10 | μA |
| Low-level input current | I _{IL} (PI) | VPWMIN = 0V | -130 | -90 | | μA |
| F/R pin | | | | | | |
| High-level input voltage | V _{IH} (FR) | | 2.0 | | VREG | V |
| Low-level input voltage | V _{IL} (FR) | | 0 | | 1.0 | V |
| Input open voltage | V _{IO} (FR) | | VREG-0.5 | | VREG | V |
| Hysteresis | V _{IS} (FR) | | 0.2 | 0.25 | 0.4 | V |
| High-level input current | I _{IH} (FR) | | -10 | 0 | 10 | μA |
| Low-level input current | I _{IL} (FR) | | -130 | -90 | | μA |
| N1 pin | | | | | | |
| High-level input voltage | V _{IH} (N1) | | 2.0 | | VREG | V |
| Low-level input voltage | V _{IL} (N1) | | 0 | | 1.0 | V |
| Input open voltage | V _{IO} (N1) | | VREG-0.5 | | VREG | V |
| High-level input current | I _{IH} (N1) | VN1 = VREG | -10 | 0 | 10 | μA |
| Low-level input current | I _{IL} (N1) | VN1 = 0V | -130 | -100 | | μA |

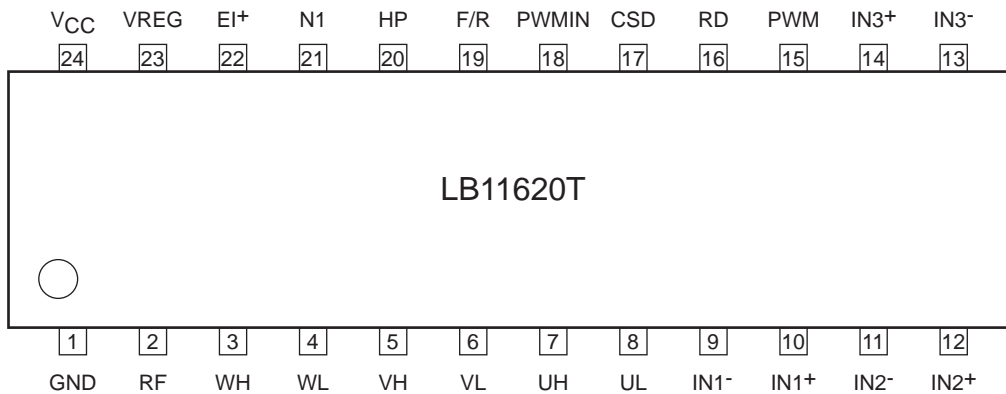
LB11620T

Package Dimensions

unit : mm (typ)
3260A



Pin Assignment



• Three-Phase Logic Truth Table (IN = "H" indicates the state where IN⁺ > IN⁻)

| | F/R = "L" | | | F/R = "H" | | | Output | |
|---|-----------|-----|-----|-----------|-----|-----|--------|----|
| | IN1 | IN2 | IN3 | IN1 | IN2 | IN3 | PWM | |
| 1 | H | L | H | L | H | L | VH | UL |
| 2 | H | L | L | L | H | H | WH | UL |
| 3 | H | H | L | L | L | H | WH | VL |
| 4 | L | H | L | H | L | H | UH | VL |
| 5 | L | H | H | H | L | L | UH | WL |
| 6 | L | L | H | H | H | L | VH | WL |

• PWMIN pin

| Input state | State |
|--------------|------------|
| High or open | Output off |
| Low | Output on |

If the PWM pin is not used, the input must be held at the low level.

• N1 pin

| Input state | HP output |
|--------------|--------------------------------------|
| High or open | Three Hall sensor synthesized output |
| Low | Single Hall sensor output |

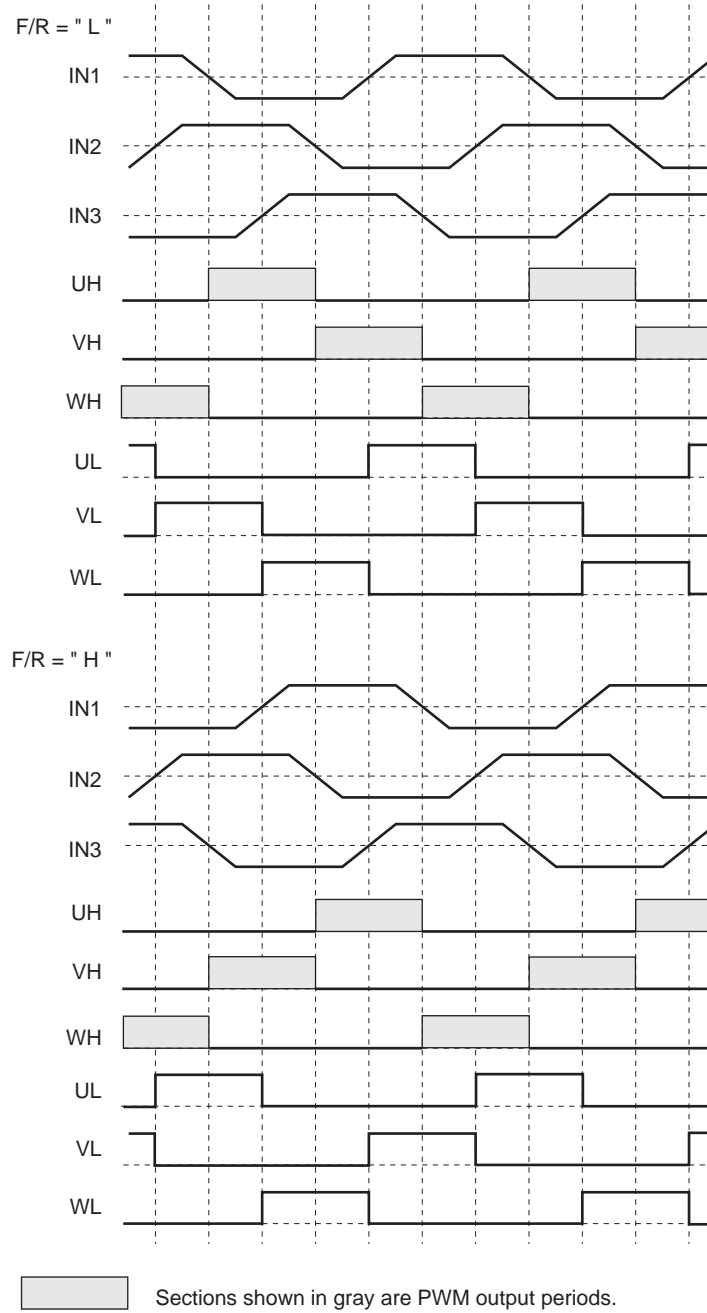
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Pin Functions

| Pin No. | Pin | Description |
|---------------------------|--|---|
| 1 | GND | Ground |
| 2 | RF | Output current detection. The current detection resistor (Rf) voltage is sensed by the RF pin to implement current detection. The maximum output current is set by RF to be $I_{OUT} = 0.25/R_f$. |
| 7 5 3 | UH VH WH | Outputs (PWM outputs). These are push-pull outputs. |
| 8 6 4 | UL VL WL | Outputs These are push-pull outputs. |
| 10, 9 12, 11 14, 13 | IN1+, IN1- IN2+, IN2- IN3+, IN3- | Hall sensor inputs from each motor phase. The logic high state indicates that $IN^+ > IN^-$. If inputs are provided by a Hall effect sensor IC, the common-mode input range is expanded by biasing either the + or - input. |
| 15 | PWM | Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor between this pin and ground. |
| 16 | RD | Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects that the motor has been stopped. This is an open collector output. |
| 17 | CSD | Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used. |
| 18 | PWMIN | PWM pulse signal input. The output goes to the drive state when this pin is low, and to the off state when this pin is high or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state must be provided. |
| 19 | F/R | Forward/reverse control input |
| 20 | HP | Hall signal output (HP output). This provides either a single Hall sensor output or a synthesized 3-sensor output. |
| 21 | N1 | Hall signal output (HP output) selection |
| 22 | EI+ | CTL amplifier + (noninverting) input. The PWMIN pin must be held at the low level to use this input for motor control |
| 23 | VREG | 5V regulator output (Used as the control circuit power supply. A low-voltage protection circuit is built in.) Connect a capacitor between this pin and ground for stabilization. |
| 24 | VCC | Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting this IC. |

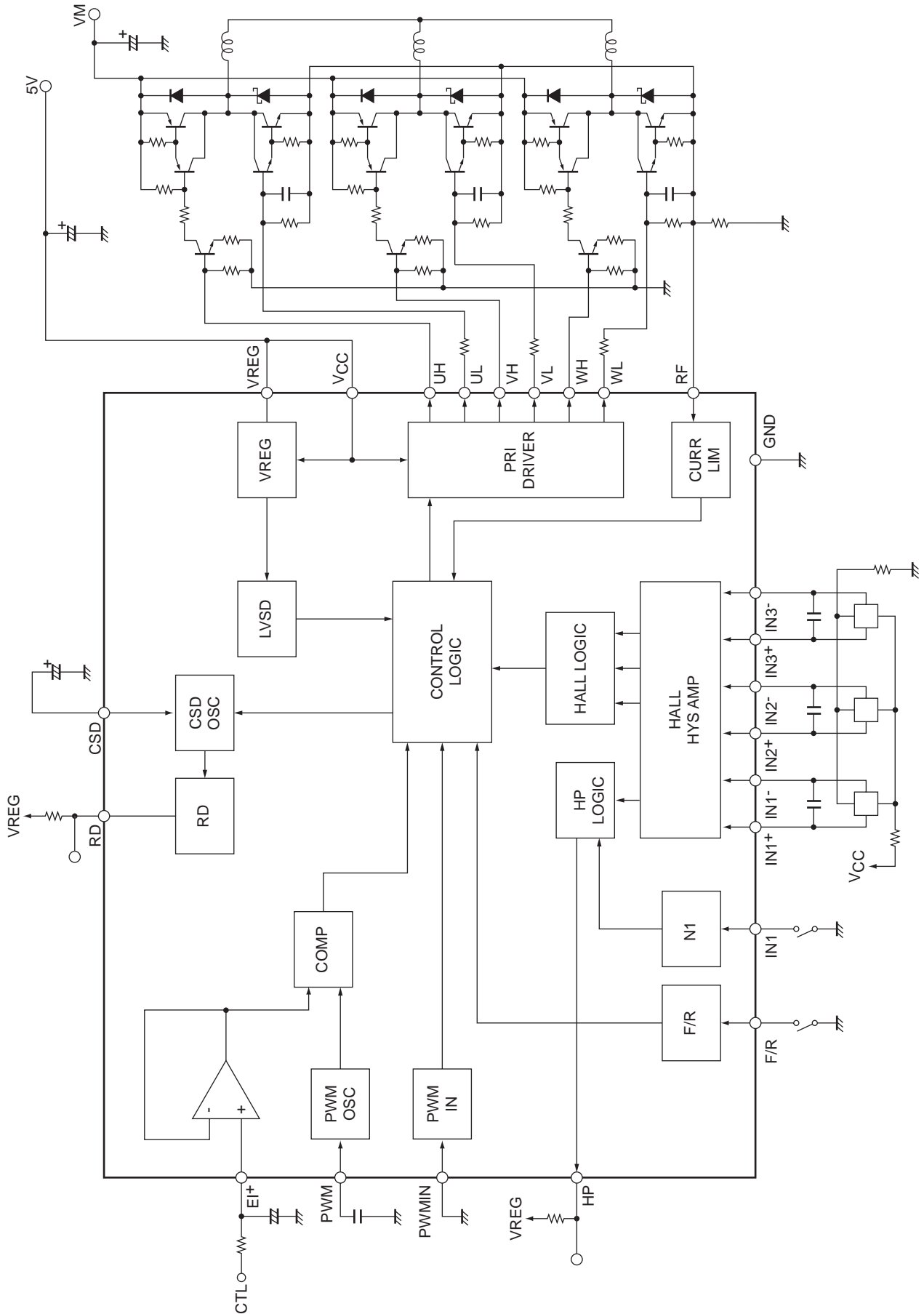
LB11620T

Hall Sensor Signal Input/Output Timing Chart



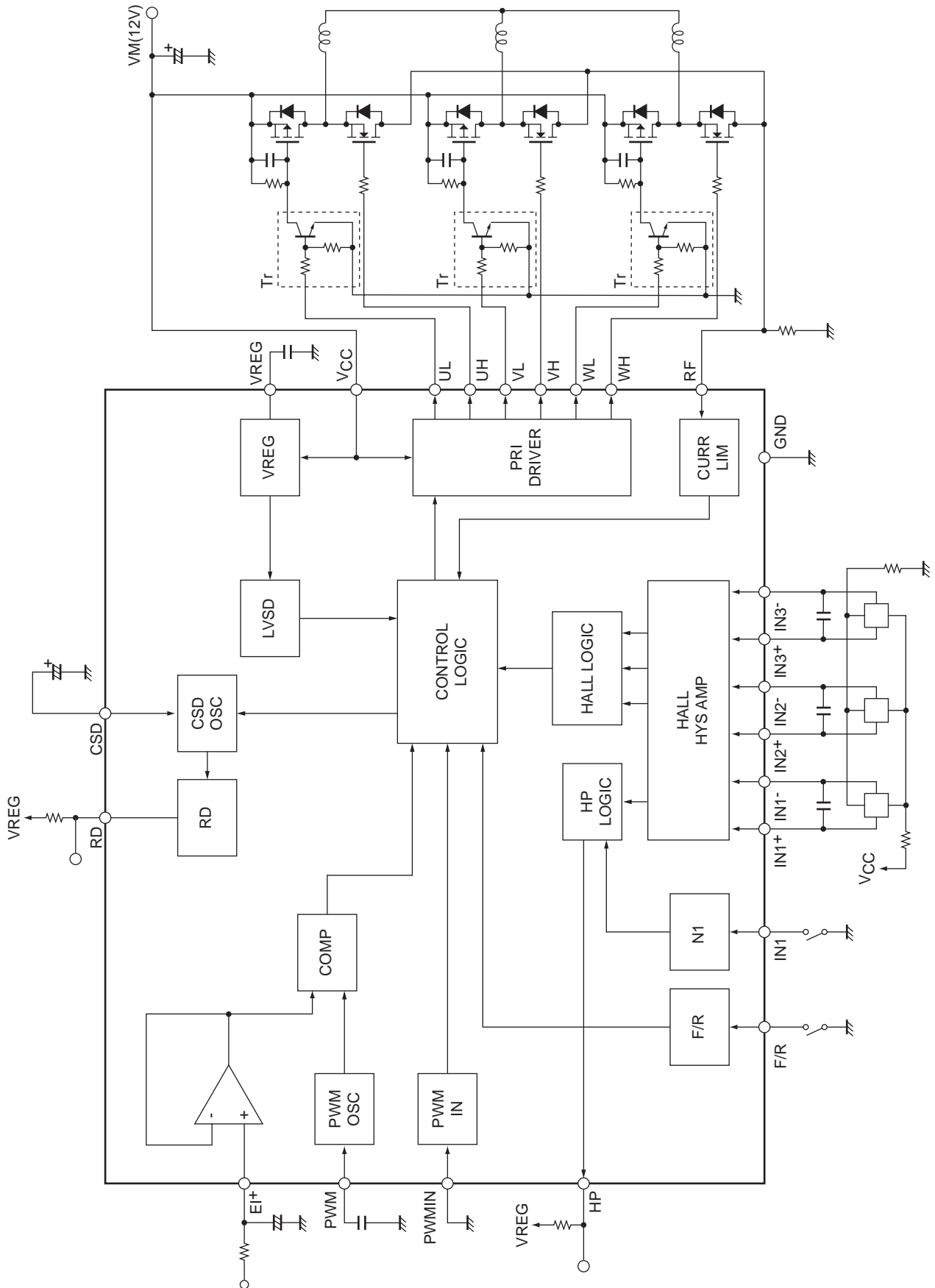
Block Diagram and Application Example 1

Bipolar transistor drive (high side PWM)
using a 5V power supply



Application Example 2

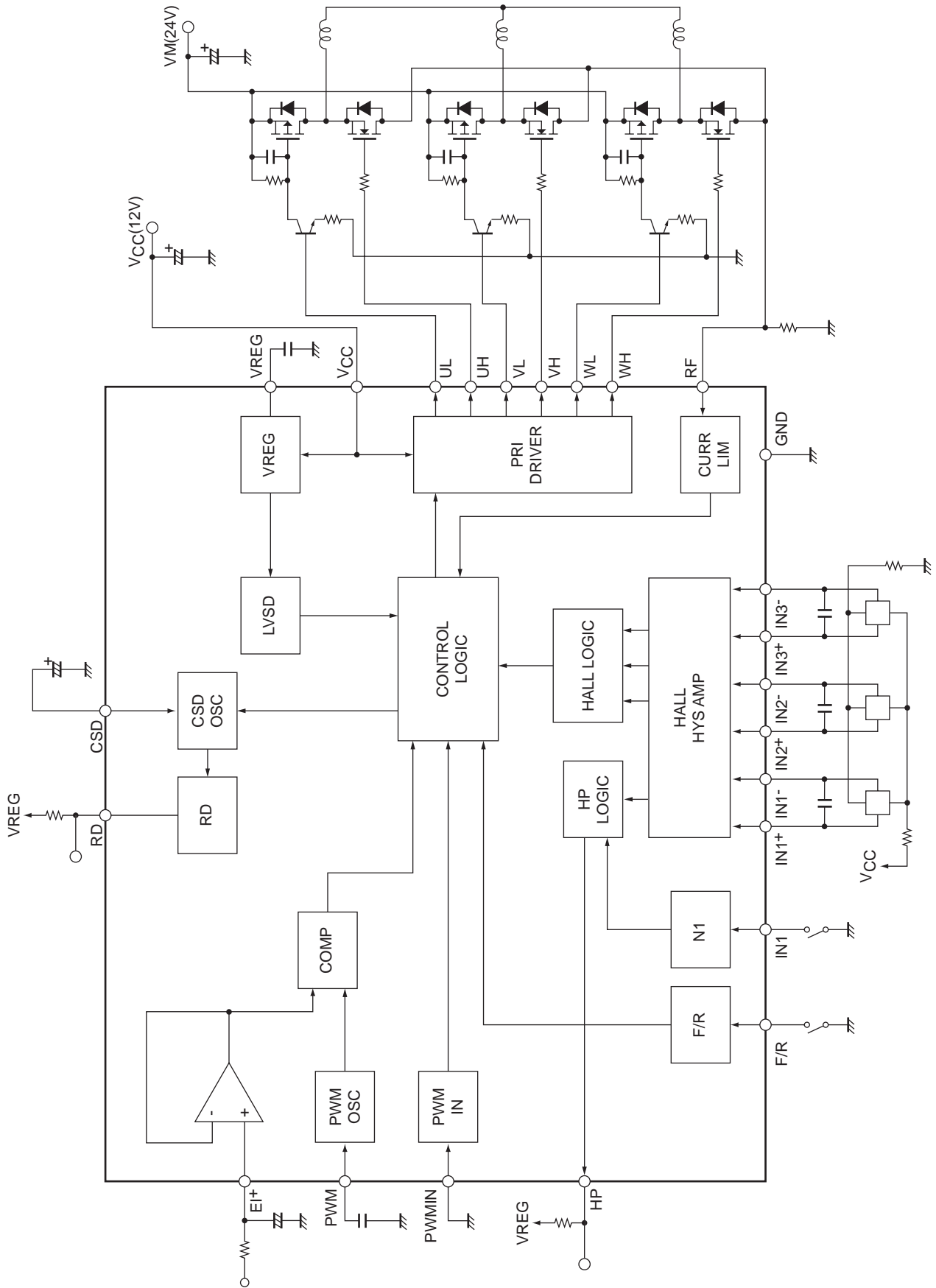
54 MOS transistor drive (low side PWM)
using a 12V single-voltage power supply



Application Example 3

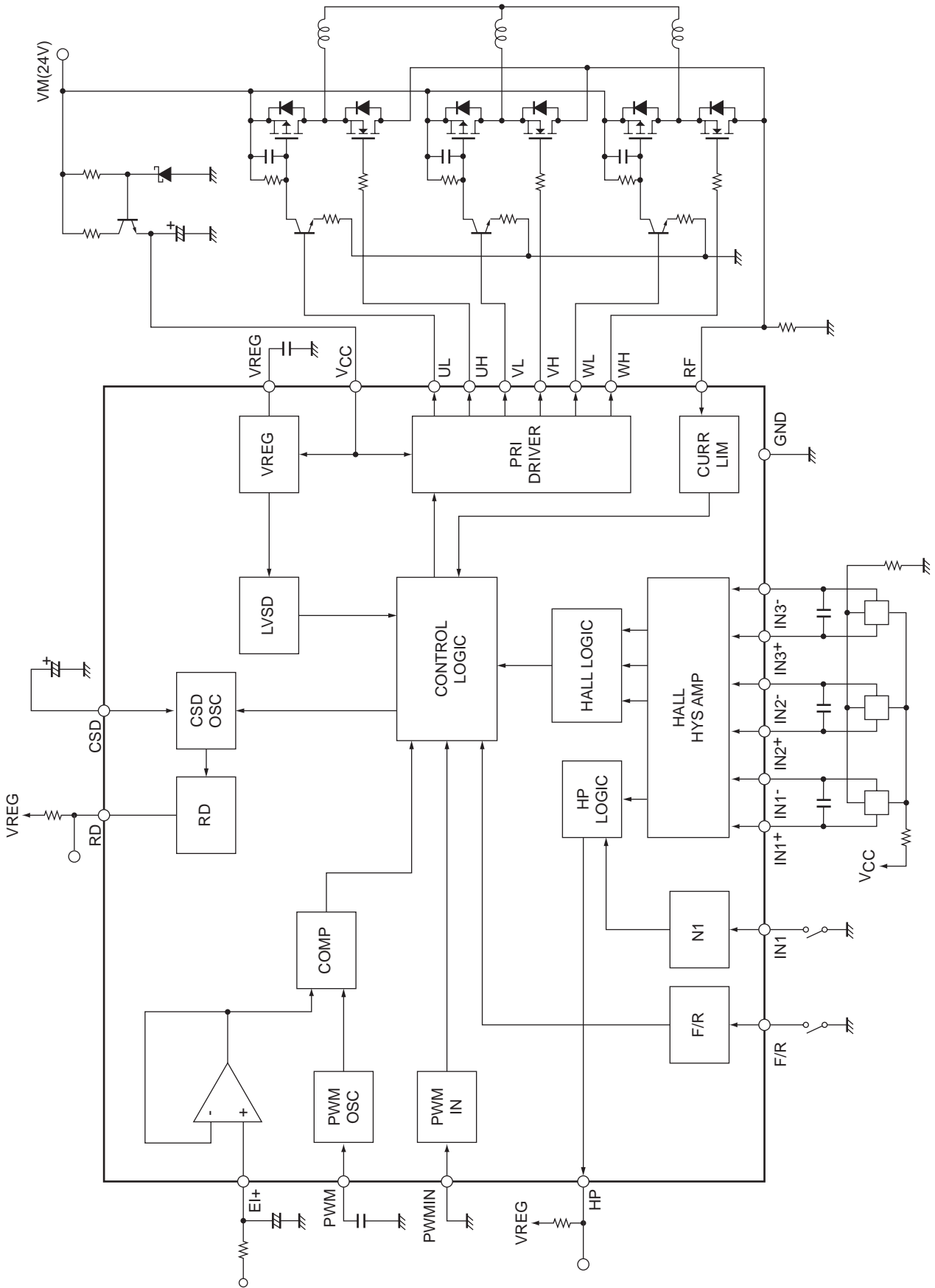
MOS transistor drive (low side PWM)

using a $V_{CC} = 12V$, $V_M = 24V$ power supply system



Application Example 4

MOS transistor drive (low side PWM)
using a 24V single-voltage power supply



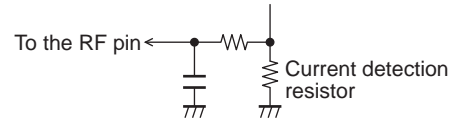
LB11620T Functional Description

1. Output Drive Circuit

The LB11620T adopts direct PWM drive to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH outputs. Since the UL to WL and UH to WH outputs have the same output form, applications can select either low side PWM or high side PWM drive by changing the way the external output transistors are connected. Since the reverse recovery time of the diodes connected to the non-PWM side of the outputs is a problem, these devices must be selected with care. (This is because through currents will flow at the instant the PWM side transistors turn on if diodes with a short reverse recovery time are not used.)

2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation $I = VFR/R_f$ ($VFR = 0.25V$ typical, R_f : current detection resistor). This circuit suppresses the output current by reducing the output on duty.



The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode reverse recovery current flows for longer than 1μs).

3. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$f_{PWM} \approx 1/(22500 \times C)$$

If a 2000pF capacitor is used, the circuit will oscillate at about 22kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it is too high, the output power loss will increase. Thus a frequency in the range 15k to 50kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

4. Control Methods

The output duty can be controlled by either of the following methods

- Control based on comparing the EI+ pin voltage to the PWM oscillator waveform

The low side output transistor duty is determined according to the result of comparing the EI+ pin voltage to the PWM oscillator waveform. When the EI+ pin voltage is 1.35V or lower, the duty will be 0%, and when it is 3.0V or higher, the duty will be 100%.

When EI+ pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to ground.

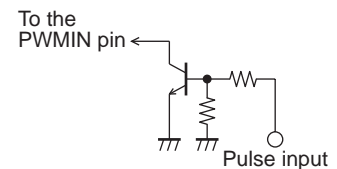
- Pulse Control Using the PWMIN Pin

A pulse signal can be input to the PWMIN pin, and the output can be controlled based on the duty of that signal.

Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the PWMIN pin is open it goes to the high level and the output is turned off. If inverted input logic is required, this can be implemented with an external transistor (npn).

When controlling motor operation from the PWMIN pin, the EI+ pin must be connected to the VREG pin.

Note that since the PWM oscillator is also used as the clock for internal circuits, a capacitor (about 2000pF) must be connected to the PWM pin even if the PWMIN pin is used for motor control.



5. Hall Input Signals

A signal input with an amplitude in excess of the hysteresis (80mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.

If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors across the inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.

If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all go to the low level).

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0V to V_{CC} range.

6. Under-voltage Protection Circuit

The under-voltage protection circuit turns one side of the outputs (UH, VH, and WH) off when the VREG pin voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output will not recover until the operating voltage rises 0.5V (typical).

7. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0 V) by a constant current of about 2.25μA and is then discharged (to about 1.0V) by a constant current of about 0.15μA.

This process is repeated, generating a saw-tooth waveform. The constraint protection circuit turns motor drive on and off repeatedly based on this saw-tooth waveform. (The UH, VH, and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0V to about 3.0V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0V to about 1.0V.

The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.

The motor drive on and off times are determined by the value of the connected capacitor C (in μF).

$$TCSD1 \text{ (drive on period)} \approx 0.89 \times C \text{ (seconds)}$$

$$TCSD2 \text{ (drive off period)} \approx 13.3 \times C \text{ (seconds)}$$

When a 0.47μF capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of about 0.4 seconds and a drive off period of about 6.3 seconds.

While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.

When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated. As a result, the CSD pin external capacitor is charged by a constant current of 2.5μA to about 3.0V, at which point the constraint protection circuit operates. When the constraint on the motor is released, the constraint protection function is released.

Connect the CSD pin to ground if the constraint protection circuit is not used.

8. Forward/Reverse Direction Switching

This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is turning. However, if the direction is switched when the motor is turning, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those current levels or only switching directions after the speed has fallen below a certain speed.

9. Handling Different Power Supply Types

When this IC is operated from an externally supplied 5V power supply (4.5 to 5.5V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.

When this IC is operated from an externally supplied 12V power supply (8 to 17 V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5V level to function as the control circuit power supply.)

11. Power Supply Stabilization

Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground.

If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required.

If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

12. VREG Stabilization

To stabilize the VREG voltage, which is the control circuit power supply, a $0.1\mu\text{F}$ or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must be connected to the IC ground pin with a line that is as short as possible.

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