MA9564

HIGH TRANSIENT/RADIATION HARD 8192 x 8 BIT STATIC RAM

The MA9564 64k Static RAM is configured as 8192x8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology. The device has been designed specifically for high transient gamma applications and is pin compatible with the Honeywell MC6364 device.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

Operation Mode	$\overline{CS}$	CE	$\overline{OE}$	$\overline{WE}$	$\overline{AS}$	I/O	Power
Read	L	H	L	H	X	D OUT	
Write	L	H	X	L	X	D IN	ISB1
Output Disable	L	H	H	H	X	High Z	
Standby	H	X	X	X	X	High Z	ISB2
	X	L	X	X	X		

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 45ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{12} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Optional Capacitors on Package and Lid to Hold Up Power Rail
- Multiple 5V Supply Pins
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation

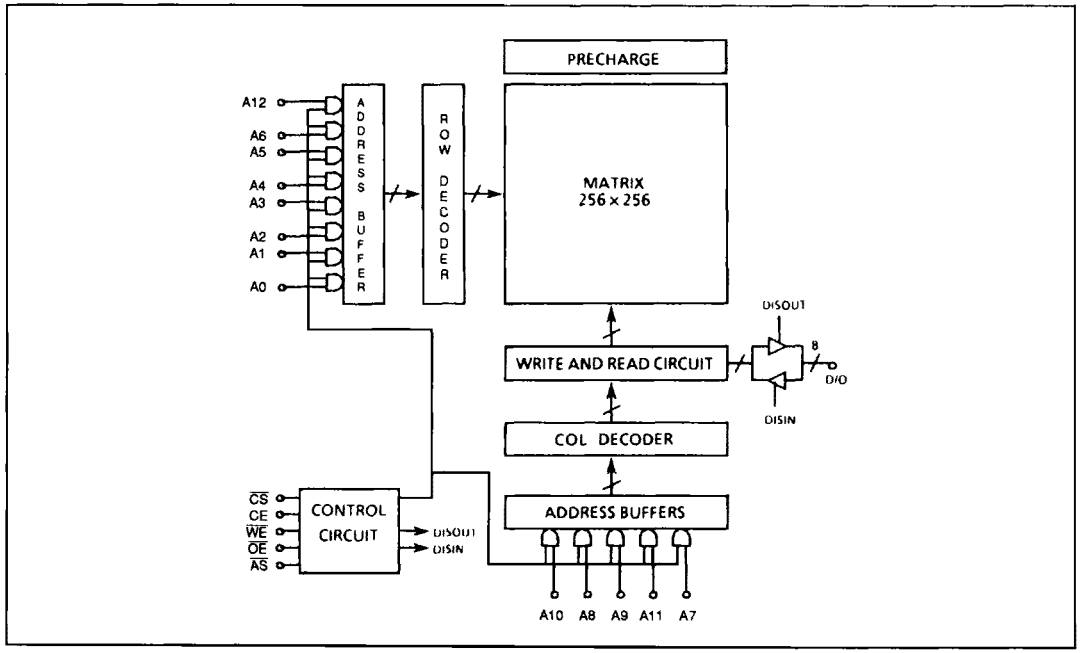


Figure 2: Block Diagram

SIGNAL DEFINITIONS

A0-12
Address input pins which select a particular eight bit word within the memory array.

D0-7
Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{CS}$
Chip Select, which, at low level, activates a read or write operation. When at a high level it defaults the SRAM to a prechargencondition and holds the data output drivers in a high impedance state.

$\overline{WE}$
Write Enable which when at a low level enables a write and holds data output drivers in a high impedance state. When at a high level, it enables a read.

$\overline{OE}$
Output Enable which when at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by $\overline{CS}$, $\overline{WE}$ and CE. If this signal is not used it must be connected to VSS.

$\overline{AS}$
Address Strobe which when at a low level maintains on chip address latches in a transparent state allowing the loading of address inputs. When at a high level, it latches the loaded address state. If this signal is not used it must be connected to VSS,($\overline{AS}$ can be connected to VSS in the package as a pinout option). $\overline{AS}$ can be connected to $\overline{CS}$ during normal operation.

CE
Chip Enable which when at a high level allows normal operation. When at a low level it defaults the SRAM to a precharge condition, disables the input circuits on all input pins and holds the data output drivers in a high impedance state. If this signal is not used it must be connected to VDD, (CE can be connected to VDD in the package as a pinout option).

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	2.0 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	-	0.1	15	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	8	23	mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V CE = V_{SS} +0.2V	-	0.1	15	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}, CE = V_{SS}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V CE = V_{SS}	-	0.05	6	mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V (TTL) and V_{SS} to 4.0V (CMOS).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9564X70 Min	MAX9564X70 Max	MAX9564X90 Min	MAX9564X90 Max	Units
T_{AVAVR}	Read Cycle Time	70	-	90	-	ns
T_{AVQV}	Address Access Time	-	65	-	85	ns
T_{EHQV}	Chip Select Access Time	-	70	-	90	ns
T_{SLQV}	Chip Enable Access Time	-	70	-	90	ns
T_{EHQX} (5,6)	Chip Selection to Output in Low Z	15	-	15	-	ns
T_{SLQX} (5,6)	Chip Enable to Output in Low Z	15	-	15	-	ns
T_{ELQZ} (5,6)	Chip Deselection to Output in High Z	0	20	0	20	ns
T_{SHQZ} (5,6)	Chip Disable to Output in High Z	0	20	0	20	ns
T_{AXQX}	Output Hold from Address Change	30	-	40	-	ns
T_{GLQV}	Output Enable Access Time	-	25	-	30	ns
T_{GLQX} (5,6)	Output Enable to Output in Low Z	15	-	15	-	ns
T_{GHQZ} (5,6)	Output Enable to Output in High Z	0	20	0	20	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9564X70 Min	MAX9564X70 Max	MAX9564X90 Min	MAX9564X90 Max	Units
T_{AVAVW}	Write Cycle Time	45	-	55	-	ns
T_{EHWH}	Chip Selection to End of Write	45	-	55	-	ns
T_{SLWH}	Chip Enable to End of Write	45	-	55	-	ns
T_{AVWH}	Address Valid to End of Write	45	-	55	-	ns
T_{AVWL}	Address Set Up Time	0	-	0	-	ns
T_{WLWH}	Write Pulse Width	35	-	40	-	ns
T_{WHAV}	Write Recovery Time	0	-	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	0	20	ns
T_{DVWH}	Data to Write Time Overlap	25	-	30	-	ns
T_{WHDX}	Data Hold from Write	0	-	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

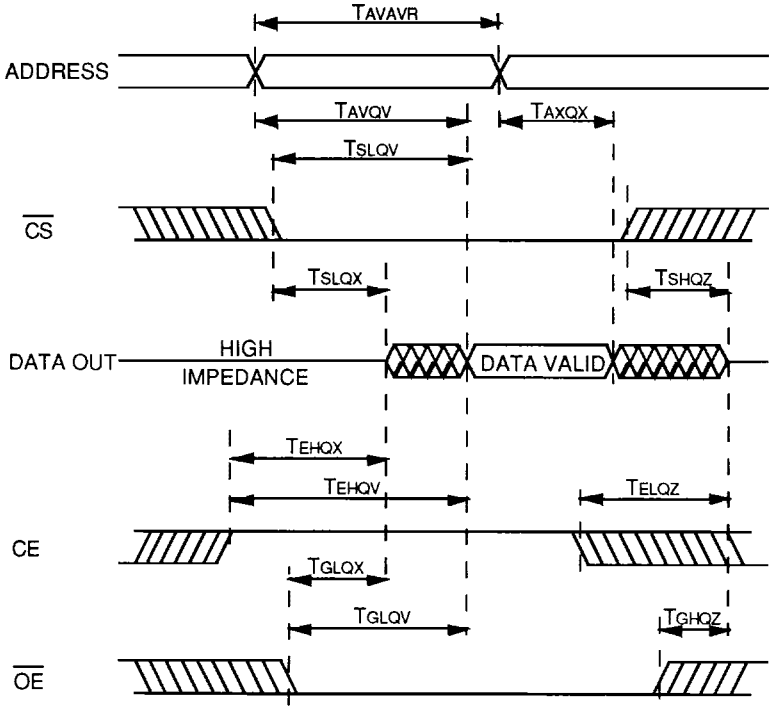
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

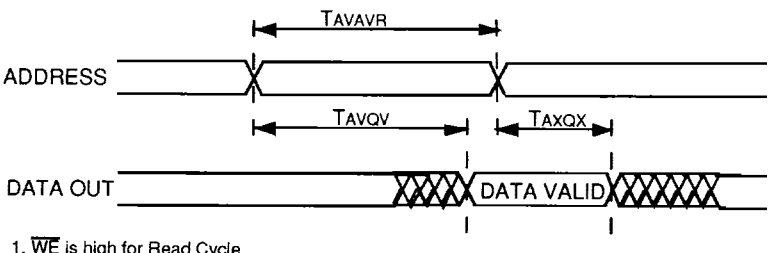
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



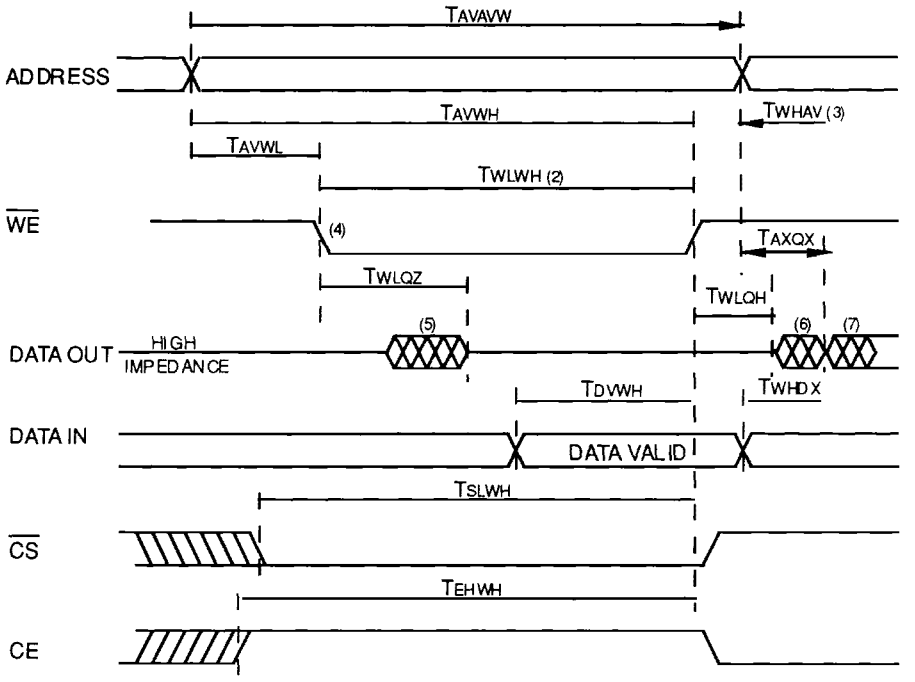
1. $\overline{WE}$ is high for Read Cycle.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low or CE transition high.
3. $\overline{AS}$ is low.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$,$\overline{AS}$,$\overline{OE}$ low,CE high.

Figure 11b: Read Cycle 2

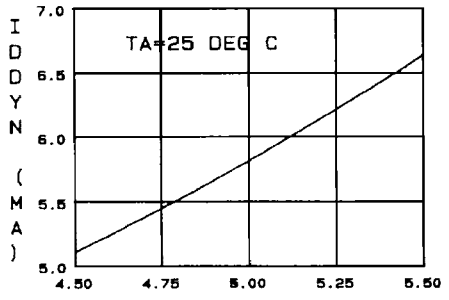


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$, a high CE and a low WE.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high or CE going low, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low or CE high transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address, if selected.
8. $\overline{AS}$ is low, $\overline{OE}$ is low. (If $\overline{OE}$ is high the DATA OUT remains in a high impedance state throughout the cycle).

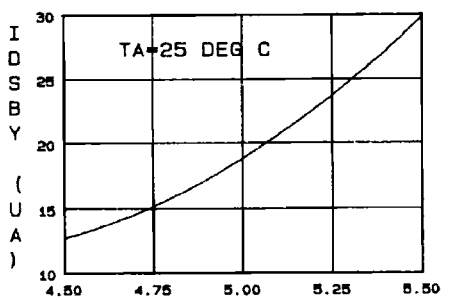
Figure 12: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9564x90

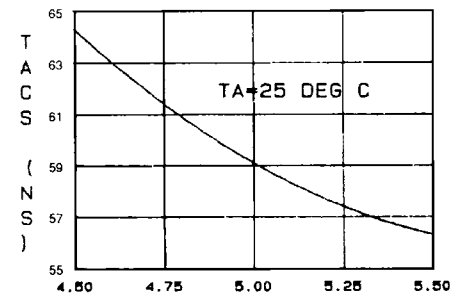
DYNAMIC CURRENT VS SUPPLY VOLTAGE



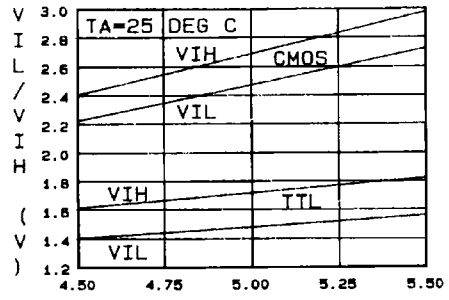
STANDBY CURRENT VS SUPPLY VOLTAGE



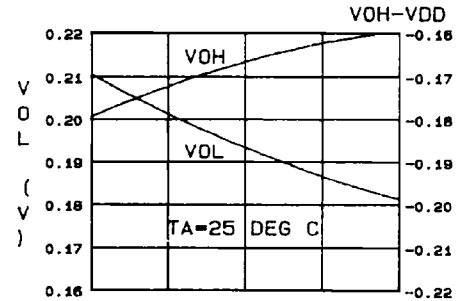
CS ACCESS TIME VS SUPPLY VOLTAGE



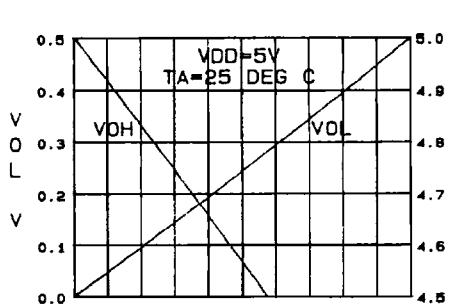
INPUT LEVELS VS SUPPLY VOLTAGE



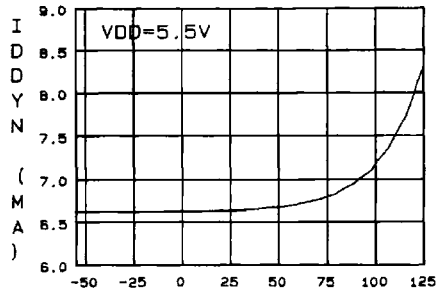
OUTPUT LEVELS VS SUPPLY VOLTAGE



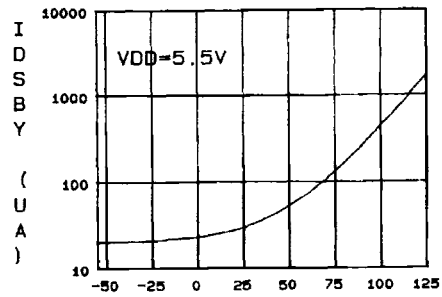
OUTPUT VOLTAGE VS CURRENT



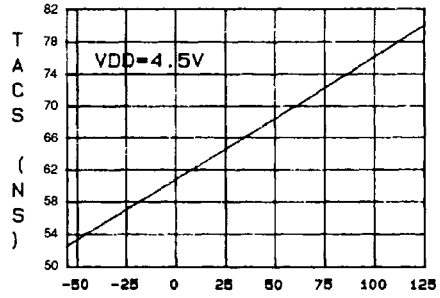
DYNAMIC CURRENT VS TEMPERATURE



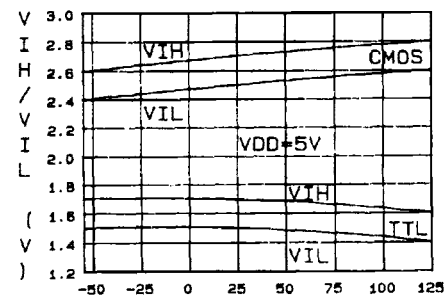
STANDBY CURRENT VS TEMPERATURE



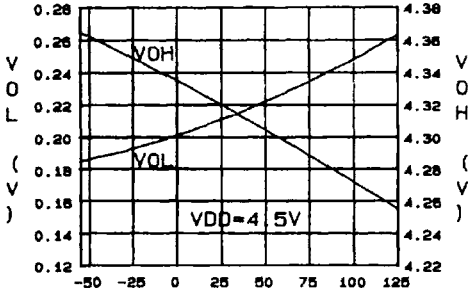
CS ACCESS TIME VS TEMPERATURE



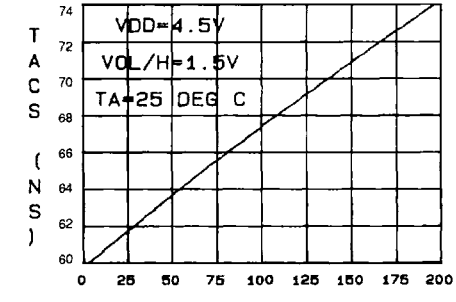
INPUT LEVELS VS TEMPERATURE



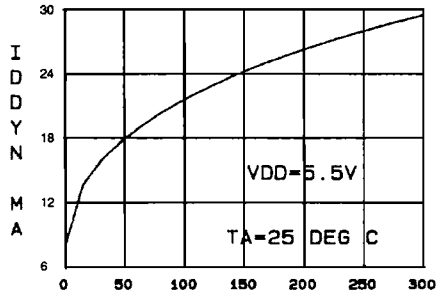
OUTPUT LEVELS VS TEMPERATURE



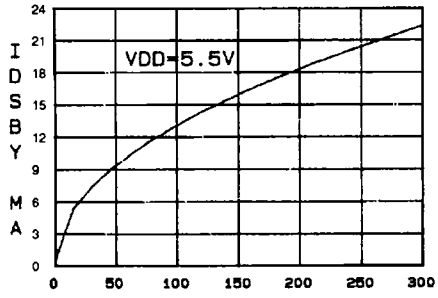
CS ACCESS TIME VS OUTPUT LOAD



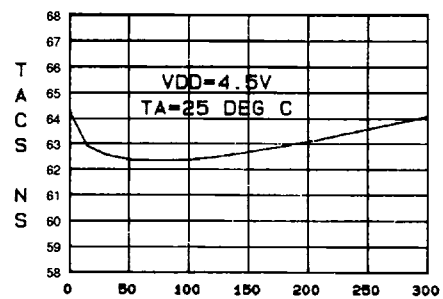
DYNAMIC CURRENT VS RADIATION



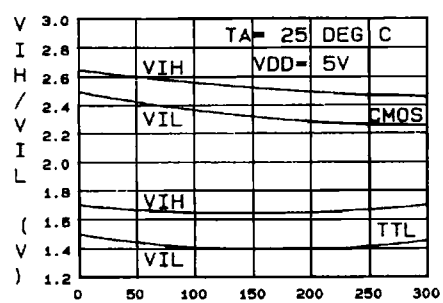
STANDBY CURRENT VS RADIATION



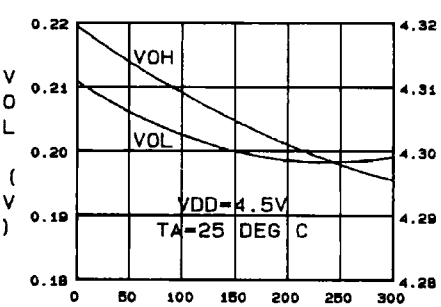
CS ACCESS TIME VS RADIATION



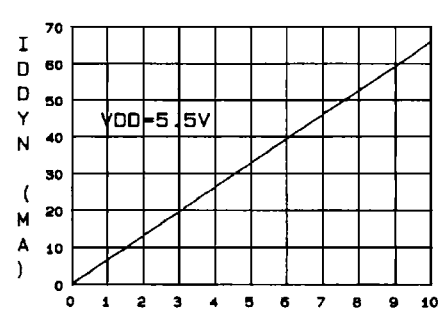
INPUT LEVELS VS RADIATION



OUTPUT LEVELS VS RADIATION



DYNAMIC CURRENT VS FREQUENCY



PIN ASSIGNMENT

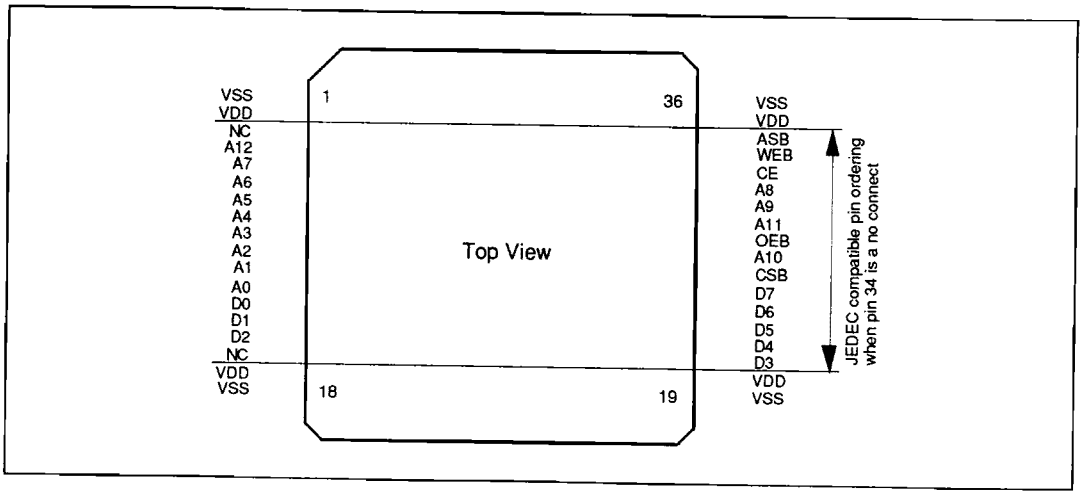


Figure 13: 36 Lead Ceramic Flatpack (Solder Seal) - Package Style F

OUTLINE

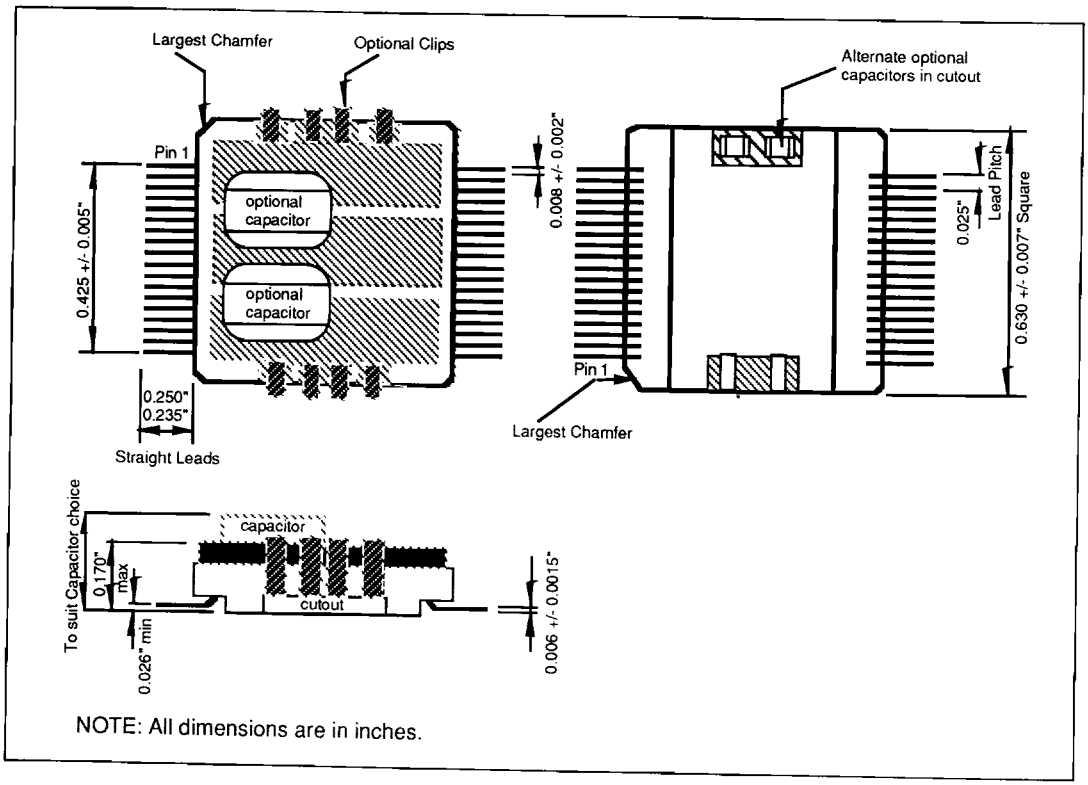


Figure 14: 36 Lead Ceramic Flatpack (Solder Seal) - Package Style F

Pin No.	Function	Connection	Static 1	Static 2	Dynamic	Radiation
1	VSS	DIRECT	0V	0V	0V	0V
2	VDD	DIRECT	5V	5V	5V	5V
4	A12	R	5V	0V	F2	5V
5	A7	R	5V	0V	F3	5V
6	A6	R	5V	0V	F14	5V
7	A5	R	5V	0V	F13	5V
8	A4	R	5V	0V	F12	5V
9	A3	R	5V	0V	F11	5V
10	A2	R	5V	0V	F10	5V
11	A1	R	5V	0V	F9	5V
12	A0	R	5V	0V	F8	5V
13	D0	R	5V	0V	F1	5V
14	D1	R	5V	0V	F1	5V
15	D2	R	5V	0V	F1	5V
17	VDD	DIRECT	5V	5V	5V	5V
18	VSS	DIRECT	0V	0V	0V	0V
19	VSS	DIRECT	0V	0V	0V	0V
20	VDD	DIRECT	5V	5V	5V	5V
21	D3	R	5V	0V	F1	5V
22	D4	R	5V	0V	F1	5V
23	D5	R	5V	0V	F1	5V
24	D6	R	5V	0V	F1	5V
25	D7	R	5V	0V	F1	5V
26	CSB	R	5V	0V	F15	5V
27	A10	R	5V	0V	F4	5V
28	0EB	R	5V	0V	F15	5V
29	A11	R	5V	0V	F7	5V
30	A9	R	5V	0V	F6	5V
31	A8	R	5V	0V	F5	5V
32	CE	R	5V	0V	F15B	5V
33	WEB	R	5V	0V	F0	5V
34	ASB	R	5V	0V	F15	5V
35	VDD	DIRECT	5V	5V	5V	5V
36	VSS	DIRECT	0V	0V	0V	0V

1. F0 = 150 KHz, F1 = F0/2, F2 = F0/4, F3 = F0/8 etc.
2. Static 1, Static 2 and Dynamic; R = 4k7.
3. Radiation; R = 10k.

Figure 15: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Basic function)	$1x10^6$ Rad(Si)
Total Dose (Function to specification)	$1x10^5$ Rad(Si)
Transient Upset	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Figure 16: Typical Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

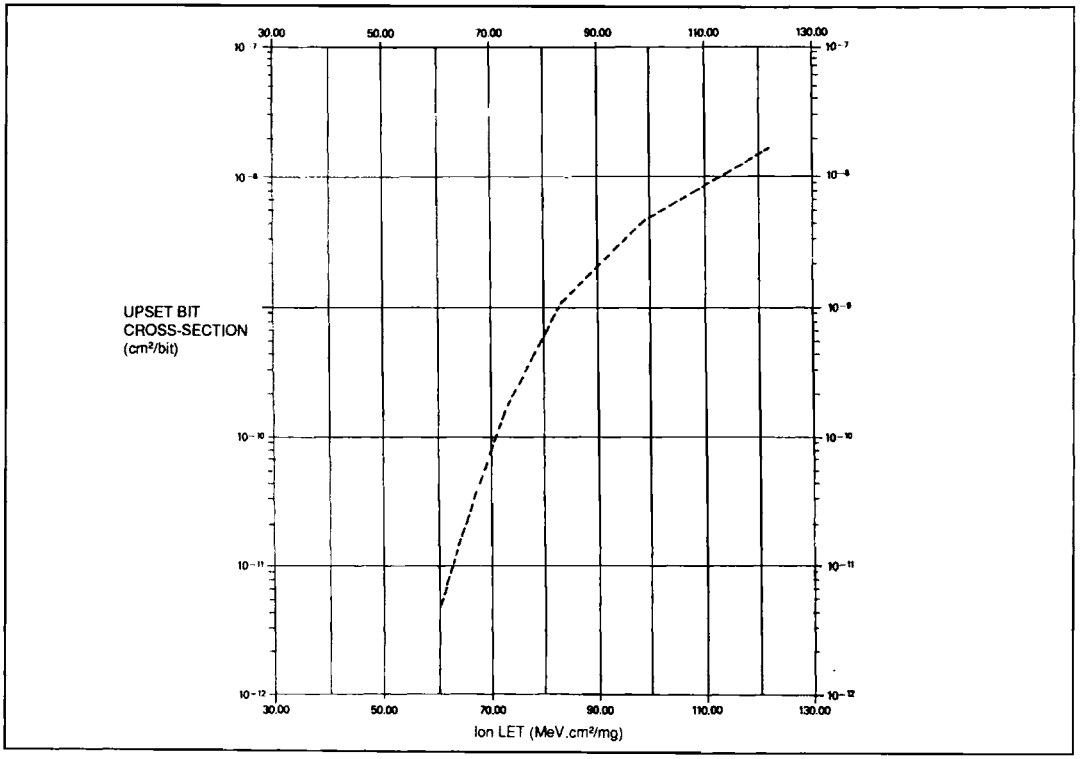
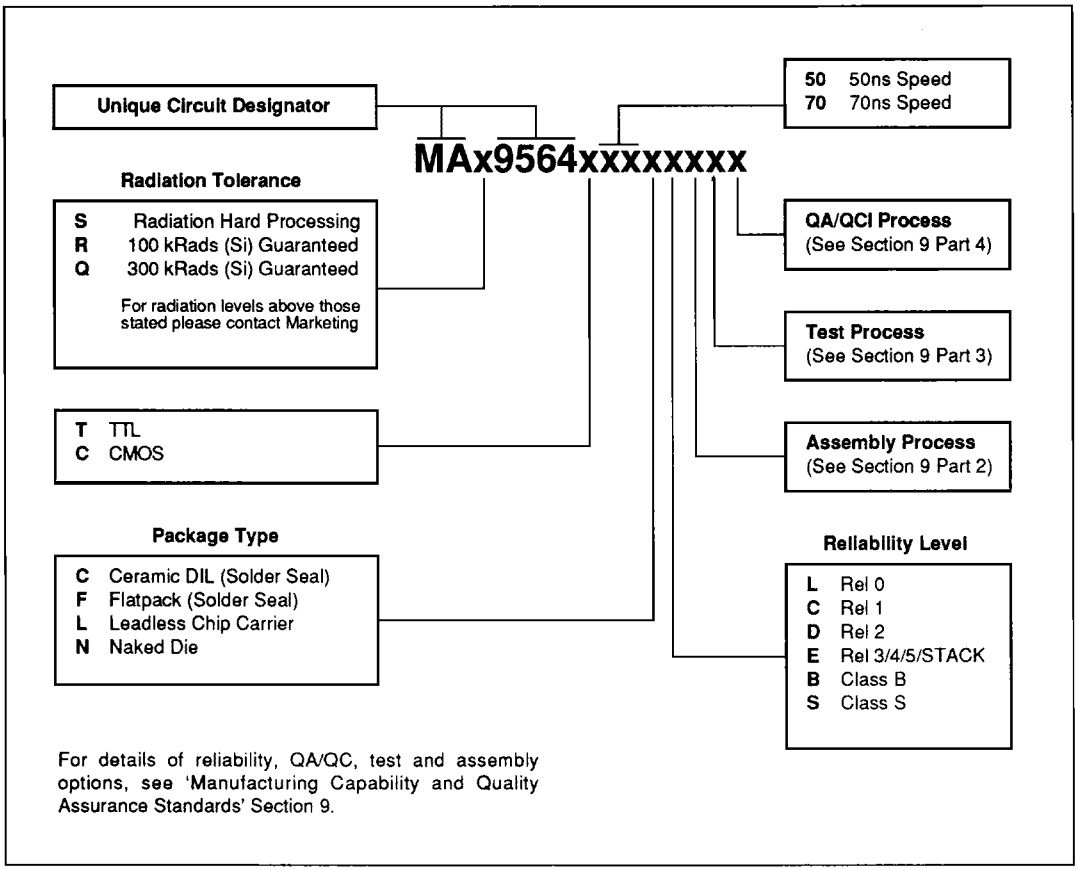


Figure 17: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.