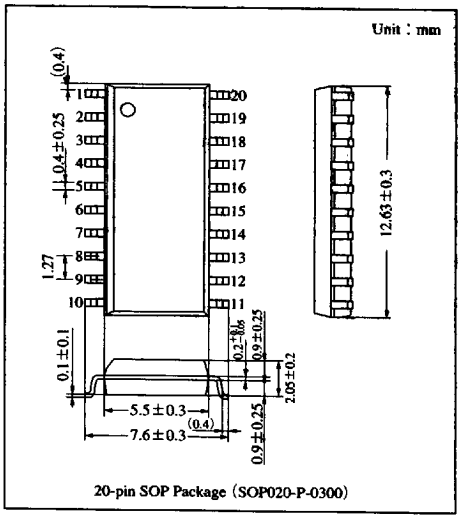
DN8665S

8-Bit Shift Register Latch Constant Current Driver IC

■ Overview

The DN8665S is a semiconductor integrated circuit which incorporates a 8-bit shift register, a latch driver and a constant current driver to satisfy the demand for equalization of LED panel brightness. It also incorporates the serial-in and serial-out/parallel-out functions. It employs the Bi-CMOS process : The 8-step shift register block and latch block consist of CMOS while the 8-step parallel driver block is bipolar.



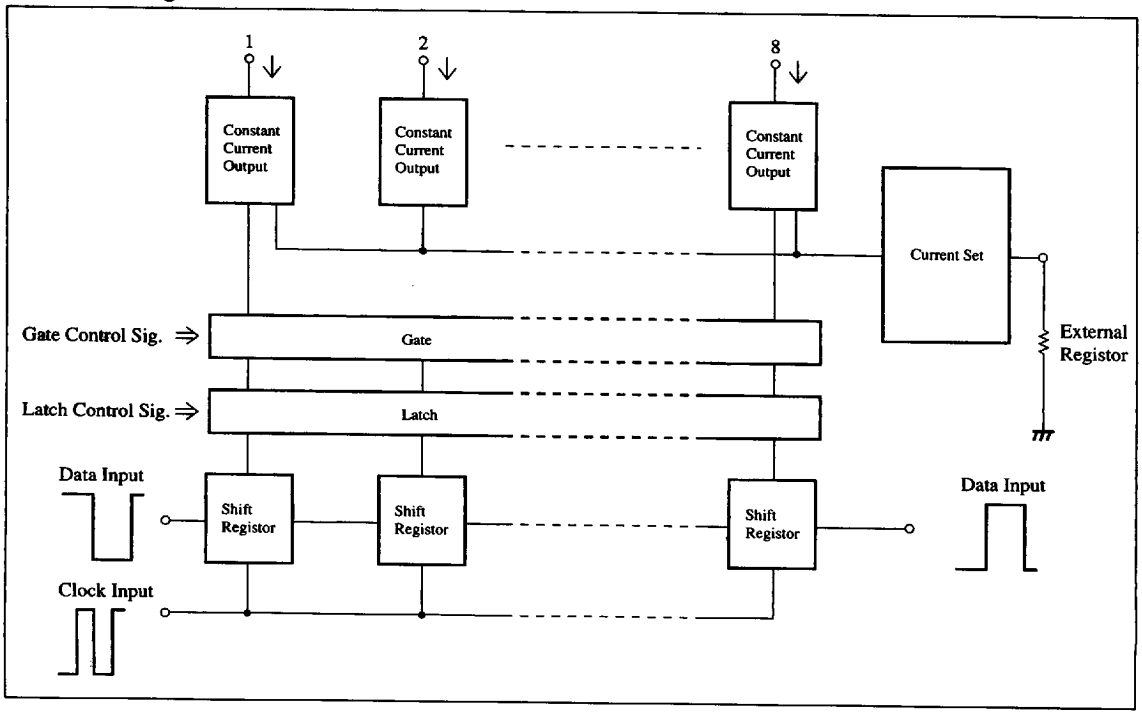
■ Features

- Serial-in, serial-out/parallel-out
- Cascade connection possible
- Constant current output (0 to 60 mA able to be set by one external resistor)
- Output-forced ON/OFF pin provided (EN)
- Input/Output CMOS compatible

■ Application

- LED panel drive

■ Block Diagram



■ Absolute Maximum Rating (Ta=25 ℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	0 to +7.0	V
Input voltage	V_I	−0.4 to V_{CC}+0.4	V
Output voltage Note 1)	V_O	0 to +30	V
Output current	I_O	80	mA
Single unit IC power dissipation Note 2)	P_D	0.718	W
Reference printed board mounting power dissipation Note 2)		1.374	
Operating ambient temperature	T_{opr}	−20 to +85	℃
Storage temperature	T_{stg}	−55 to +150	℃

Note 1) When output is off
Note 2) It is specified for reference printed board SM (glass epoxy printed board : 50×50×0.8mm).
It decreases with rate of 11.0 mW/℃ from Ta=25 ℃.

■ Recommended Operation Range (Ta=25 ℃)

Parameter	Symbol	Range
Operating supply voltage	V_{CC}	4.5V to 5.5V

■ Electrical Characteristics (V_{CC}=5V, Ta=25 ± 2℃)

Parameter		Symbol	Condition	min	typ	max	Unit
Input voltage	Positive direction	V_{T+}	V_{SOUT}=0.1, V_{CC}−0.1V I_{SOUT}=20 μA	0.35V_{CC}	—	0.7V_{CC}	V
	Negative direction	V_{T-}	I_O ($\overline{Qn}$) =10 μ, 22mA V_O ($\overline{Qn}$) =1.0V I_{ref}=−12mA	0.2V_{CC}	—	0.55V_{CC}	V
Input current		I_{IH}	V_{IH}=5.0V	—	—	25	μA
		I_{IL}	V_{IL}=0V	−25	—	—	μA
Output voltage (SOUT)		V_{OH}	V_{CC}=5.0V, I_{OH}=−0.4mA	4.0	—	—	V
		V_{OL}	V_{CC}=5.0V, I_{OL}=1.6mA	—	—	0.5	V
Output current		I_O	V_O ($\overline{Qn}$) =0.8V	—	—	60	mA
Output current error between bits		ΔI_O	V_{CC}=5.0V, I_{ref}=−12mA V_O ($\overline{Qn}$) =1.0V	—	—	±6	%
Output leak current		I_{OLK}	V_O=30V (Output OFF)	—	—	50	μA
		I_{OLK}	V_O=15V (Output OFF)	—	—	25	μA
Supply current		I_{CC1}	Total Driver Output OFF, V_{CC}=5.5V, I_{ref}=0mA	—	—	6	mA
		I_{CC2}	Total Driver Output OFF, V_{CC}=5.5V, I_{ref}=−12mA	—	—	45	mA
		I_{CC3}	Total Driver Output ON, V_{CC}=5.5V, I_{ref}=−12mA	—	—	55	mA
Maximum clock frequency		f_{max}	CLK	12	—	—	MHz
Transmission delay time		t_{PLH}	CLK → SOUT, V_{CC}=5.0V, R_L=50Ω, C_L=15pF	—	—	100	ns
		t_{PHL}		—	—	100	ns
		t_{PLH}	CLK → $\overline{Qn}$	—	—	350	ns
		t_{PHL}		—	—	350	ns
		t_{PLH}	EN → $\overline{Qn}$	—	—	350	ns
		t_{PHL}		—	—	350	ns
		t_{PLH}	STB → $\overline{Qn}$	—	—	350	ns
		t_{PHL}		—	—	350	ns

■ Recommended Operation Conditions (Ta = −20 ~ +85℃)

Parameter		Symbol	Condition	min	typ	max	Unit
Supply voltage		V_{CC}		4.5	5.0	5.5	V
Output voltage		V_O		—	—	30	V
Input voltage		V_I		0	—	V_{CC}	V
Clock frequency		f_{CLK}	Input Duty 40 to 60%	—	—	12	MHz
Input pulse width	CLK	t_w		33	—	—	ns
	STB			33	—	—	ns
Setting-up time	SIN	t_{su}		25	—	—	ns
	STB			33	—	—	ns
Holding time	SIN	t_h		20	—	—	ns
	STB			10	—	—	ns
Clock pulse rise time		t_r		—	—	500	ns
Clock pulse fall time		tf		—	—	500	ns
Output current Note)	$\overline{Qn}$	I_{OUT}		—	—	60	mA
	SOUT	I_{OH}		—	—	−0.4	mA
		I_{OL}		—	—	1.6	mA

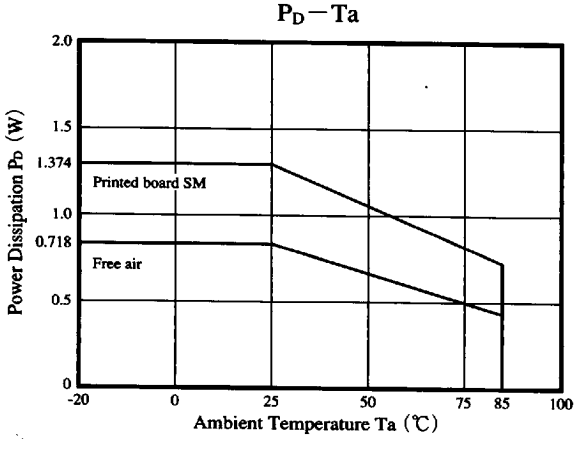
Note) Allowable value is changed,depending on the number of simultaneous ON circuits and duty.
The power dissipation should be reviewed enough for use of DN8665S.

■ Function Table (Note)

Input				Output			
CLK	STB	EN	SIN	$\overline{Q_0}$	$\overline{Q_m}$	$\overline{Q_7}$	SOUT
↑	H	L	Q_n	$\overline{Q_n}$	$\overline{Q_{m-1}}$	$\overline{Q_6}$	Q_6
↑	L	L	Q_n	nc	nc	nc	Q_6
↑	×	H	Q_n	H	H	H	Q_6
↓	×	×	Q_n	nc	nc	nc	nc

(Note)
H : High level,
L : Low level,
× : H or L
Q_m,Q_n : H or L.
However, for $\overline{Q_n}$, "H" =OFF, "L" =ON.
↑ : Shift from L to H,
↓ : Shift from H to L
nc : No change

■ Package Power Dissipation



Note) For SM to printed board (glass epoxy printed board : 50×50×0.8mm).
it decreases with rate of 11.0mW/℃ from Ta=25 ℃.
For free air, it decreases with rate of 5.74mW/℃ from Ta=25 ℃.

■ Pin Descriptions

Pin No.	Symbol	Pin name	Description
1	DGND	Digital ground	Digital ground
2	SIN	Serial data input	It is the serial data input terminal for shift register.
3	CLK	Clock input	The value of shift register shifts at the rising edge of clock input.
4	STB	Strobe input	Setting the STB input to "H" forwards the data of shift register to the latch. When the STB input is set to "L", even if the value of shift register changes, the value of latch is not changed.
5, 7, 8, 10, 11, 13 14, 16	$\overline{Qn}$	Driver output	It outputs signals by using the polarity opposite to that of data taken into the latch. For example, when the value of serial input is "H", the output becomes "L" level and the output is turned on. The output takes open collector form of NPN transistor.
6, 9 12, 15	PGND	Output ground	Output ground
17	EN	Enabling input	When the EN input is set to "H", all the outputs are turned off, independent of condition of shift register and latch driver.
18	SOUT	Serial data output	It is the terminal which performs the serial-output of data inputted from the SIN.
19	RC	Constant current setting input	It connects the external resistor between RC and GND and sets the current of output block. * Output current calculation : $I_O\ (\overline{Qn})\ (A) \fallingdotseq \frac{5 \times V_{CC}\ (V)}{2 \times R_{RC}\ (\Omega) + 50}$ ** RC terminal setting calculation : $I_{RC}\ (A) \fallingdotseq \frac{V_{CC}\ (V)}{2 \times R_{RC}\ (\Omega) + 50}$ or $R_{RC}\ (\Omega) \fallingdotseq \frac{1}{2}\left(\frac{V_{CC}\ (V)}{I_{RC}\ (A)} - 50\right)$
20	Vcc	Vcc	Supply terminal

* Calculation example

$V_{CC}=5V \quad I_O\ (\overline{Qn}) \fallingdotseq \frac{5 \times 5}{2 \times 183 + 50} \fallingdotseq 60mA$

$R_{RC}=183\,\Omega$

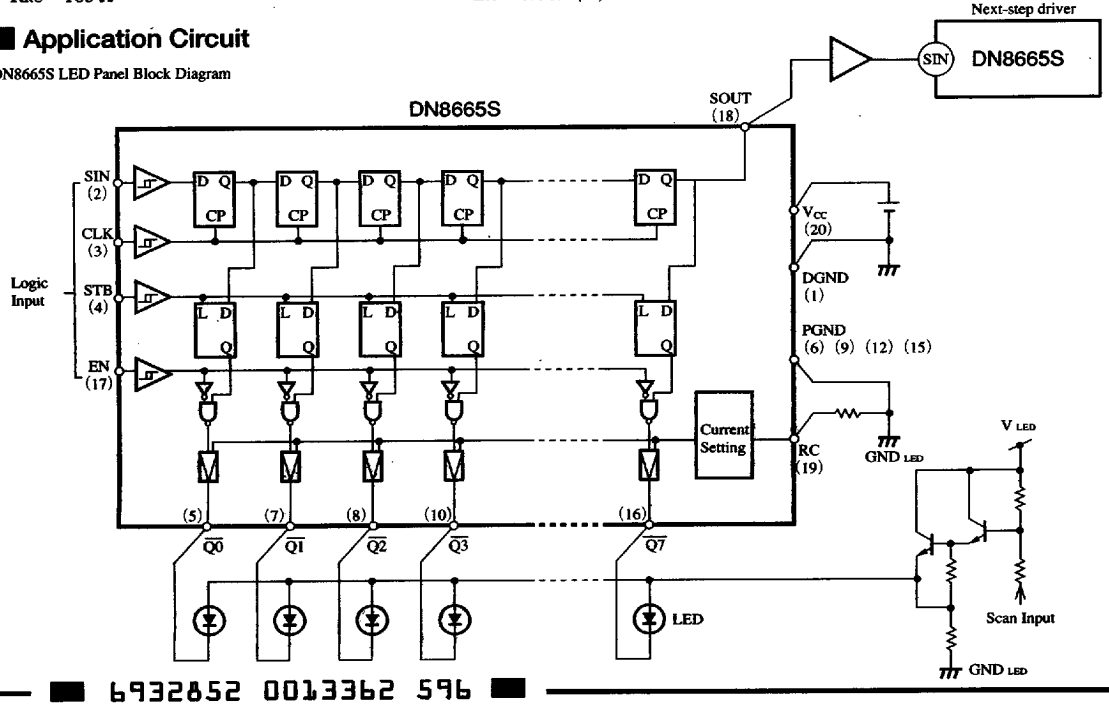
** Calculation example

$V_{CC}=5V \quad R_{RC} \fallingdotseq \frac{1}{2}\left(\frac{5}{0.012} - 50\right) \fallingdotseq 183\ (\Omega)$

$I_{RC}=0.012\ (A)$

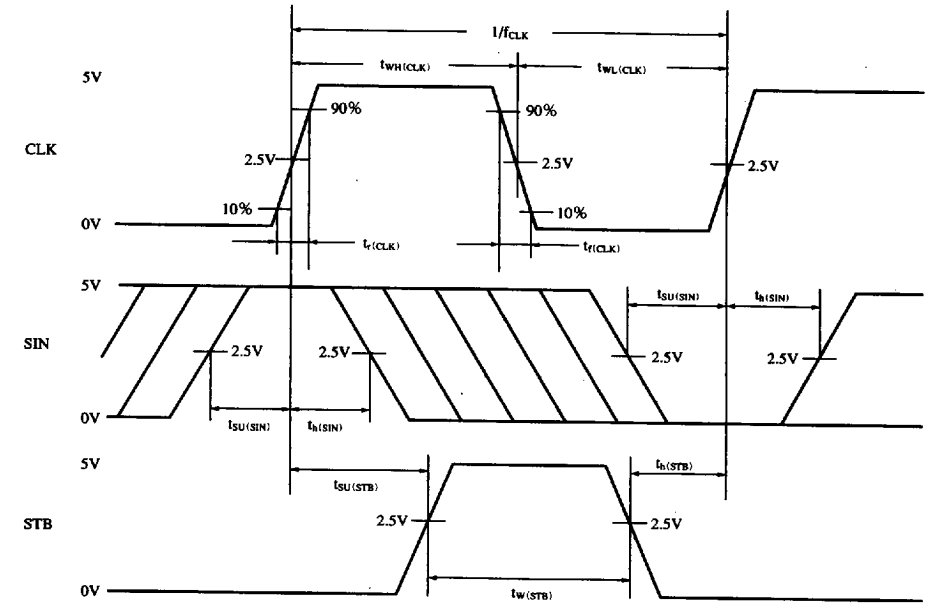
■ Application Circuit

DN8665S LED Panel Block Diagram

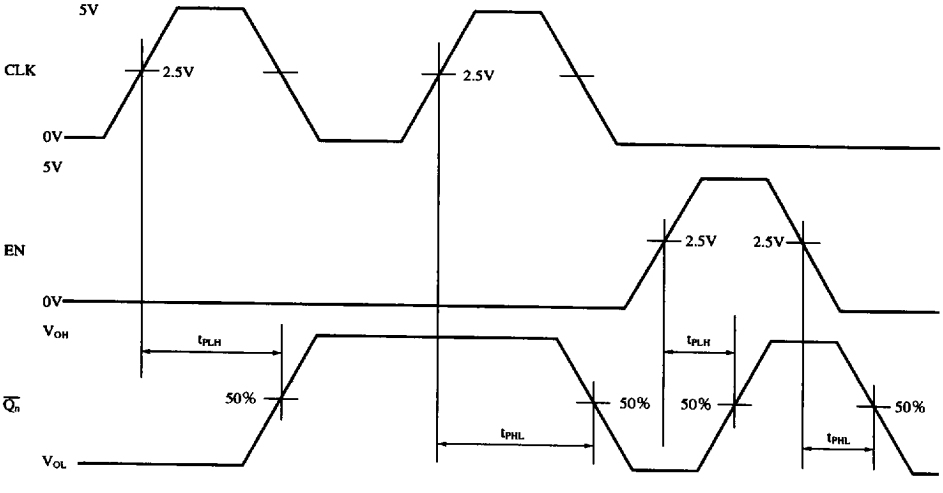


■ Timing Chart

1. Input timing (V_{IL}=0V,V_{IH}=5.0V)



2. Transmission delay time (V_{IL}=0V,V_{IH}=5.0V)



Others